Algorithm and implementation of muon trigger and data transmission system for barrel-endcap overlap region of the CMS detector

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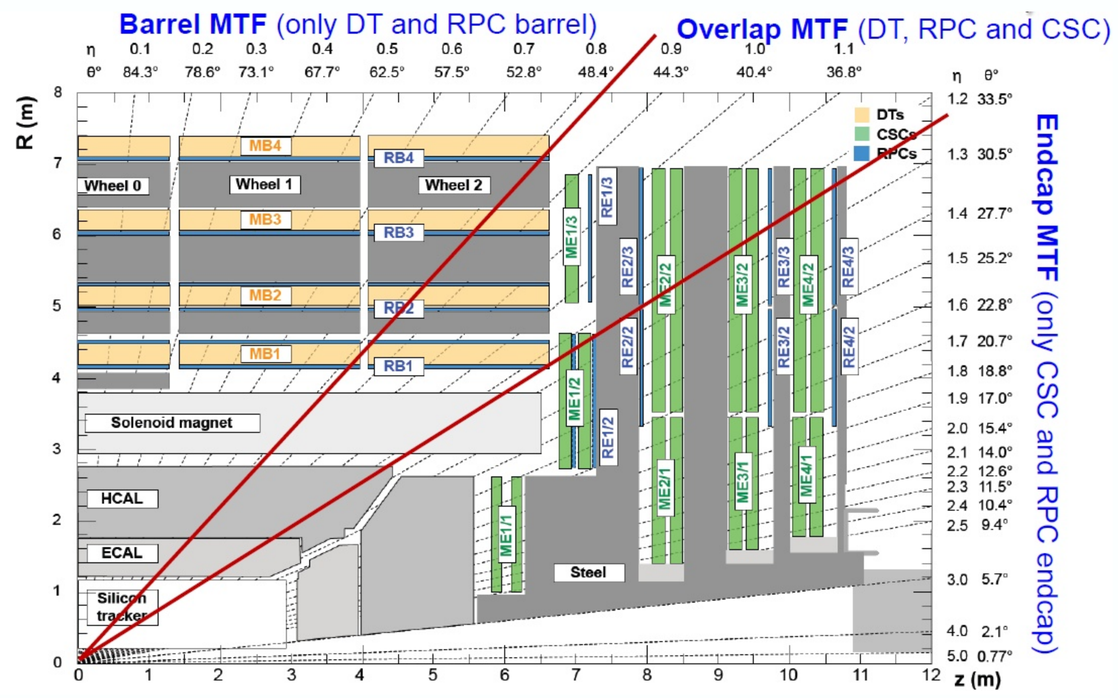
Introduction

Compact Muon Solenoid (CMS) is one of experiments at the Large Hadron Collider (LHC) at CERN.
After successfull operation in years 2010-2012, which resulted in discovery of Higgs boson, it is currently undergoing **upgrade of its trigger, including the Level-1 muon trigger [1]**. In the barrel-endcap transition region (see the Figure below) it is possible to combine signals from 3 types of muon detectors - RPC, DT and CSC. **The Overlap Muon Track Finder (OMTF)** is a dedicated electronic system analyzing the data received from those detectors and finding trigger muon candidates.
The result of the OMTF processing is transferred to the CMS Level-1 Global Muon Trigger.

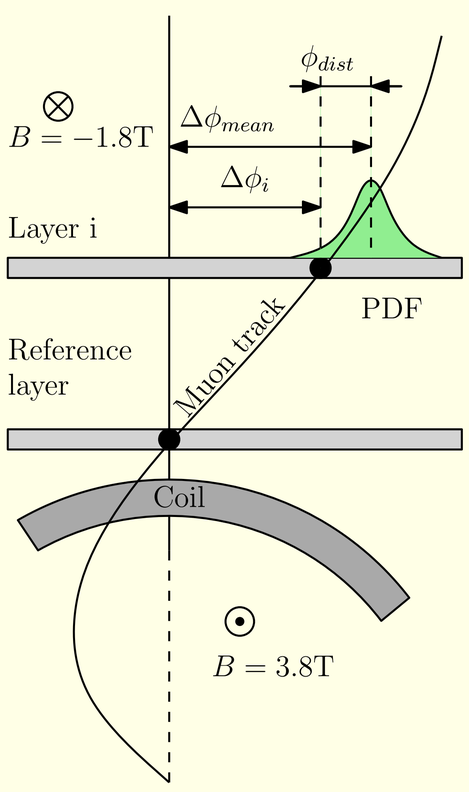


Algorithm of the trigger

The complex detector geometry in the overlap region and possible large number of available signals in the event motivated us to develop **an algorithm based on comparison of reconstructed signals from detectors (hits) with a set of precomputed patterns, called Golden Patterns (GPs).** Each GP is an object intended to represent a muon tracks with defined transverse momentum range and sign. It contains information about average track bending in the CMS magnetic field between consecutive detector layers and possible track deviations (due to stochastic effects), represented in associated probablity density functions (PDF).

From the large number of available detector layers a subset of reference ones is choosen. To provide analysis of multi-muon events, up to 4 hits in these layers (reference hits) are selected to start the muon reconstruction within OMTF.
For each hit in the event, the difference of the angular azimuthal positions ($\Delta\Phi$) between this hit and the particular reference hit is computed. Then taking into account bending of the average track ($\Delta\Phi_{mean}$) kept in GPs, the distance of a hit from the average position in that layer is calculated (Φ_{dist}). Then the PDF value for particular hit position in the layer is extracted from each GP. Using all available data, the GP best matched to event data (in terms of sum of PDFs and number of hit layers) is selected.

Thus up to 4 muon candidates (given by GP), associated with the reference hits, can be reconstructed. Within these candidates duplicates (one physical muon may result in several candidates) are removed and best candidates in terms of reconstruction quality are selected as a result of algorithm reconstruction.



Hardware Platform

Due to high number of possible detector signal inputs and high consumption of logic resources the OMTF trigger has been splited into smaller OMTF processors, each covering the 70˚ range of Φ (with 10˚ overlap between neighbouring processors). Each OMTF processor is implemented in the MTF7 board [2].
The MTF7 board is an MTCA double width AMC board equipped with two FPGA chips XC7VX690T and XC7K70 and with optional memory daughterboard. The OMTF processor occupies the bigger XC7VX690T chip.

Data transmission and preprocessing

The OMTF trigger has been implemented in FPGA chips.
The input RPC, CSC and DT data are transmitted via optical links at different rates (1.6 Gbps, 3.2 Gbps or 10 Gbps) using different transmission modes (synchronous or asynchronous).
Before those data are processed by the OMTF trigger it is necessary to deserialize them and combine them in the data sets corresponding to particular event.
To ensure that each data source is independently synchronised with the LHC clocking system, synchronization circuits are controlled via IPbus software and specific delay coefficients are determined (and tuned) at runtime.
To allow uniform further processing, those data must be converted into a unified format, containing the azimuthal angle (Φ) of each hit.
Conversion parameters (specific to data source) can also be controlled with IPbus.
Finally the data from various detectors must be aligned in time before passing to the OMTF algorithm.

Implementation of the algorithm

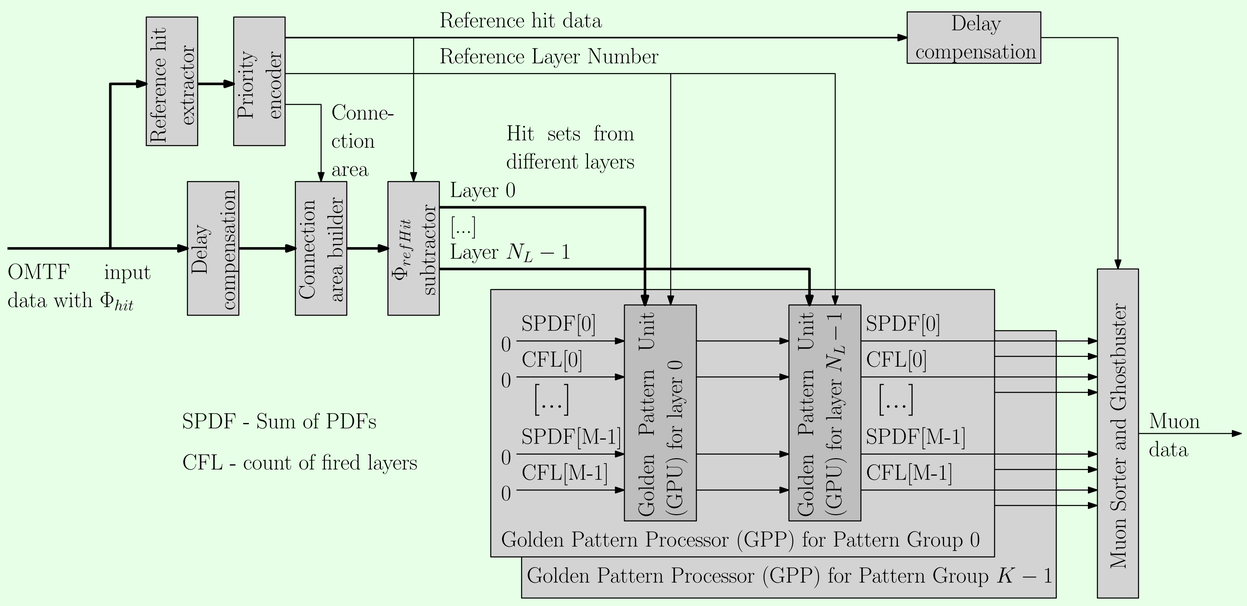
The OMTF processor has been implemented in the pipelined architecture. To allow checking of the multiple reference hits in a single event, the internal clock frequency of the OMTF processor is a multiple of the LHC clock frequency. The multiplication factor is parametrized and may be changed before compilation. The current implementation of the OMTF is able to operate with multiplication factor of 4, i.e. with internal clock frequency of ca. 160 MHz, allowing to check up to 4 reference hits in each event.

The OMTF processor must be implemented in a flexible and easy to maintain way in order to fullfill High Energy Particle Physics requirements to allow further development, optimization and adaptation to running operating conditions of LHC.

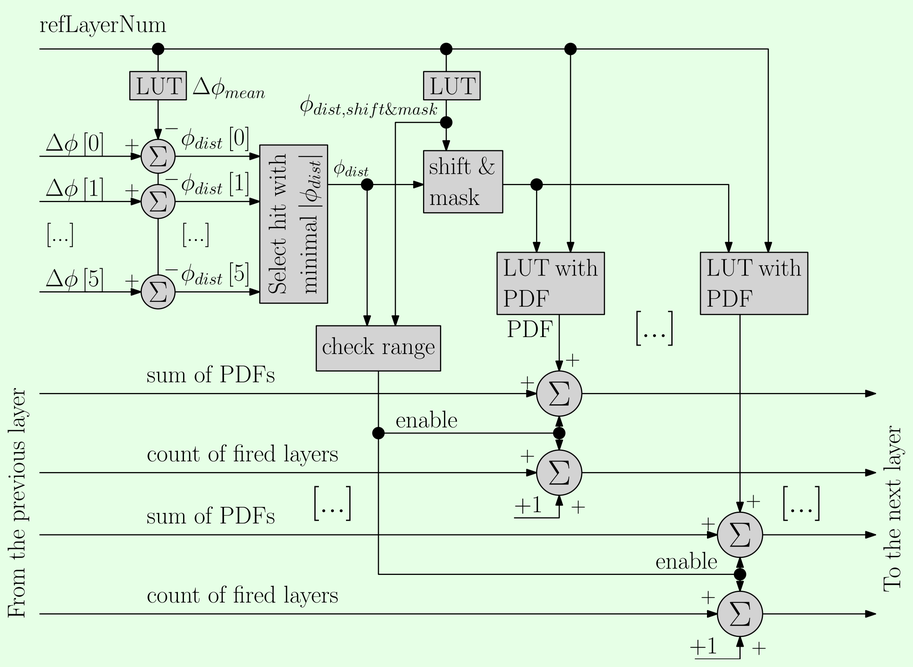
Therefore a special high level, parametrized VHDL description was used. Various parameters, like: number of reference hits, length of the word on different stages and number of patterns may be adjusted before synthesis. Most data structures are described using the hierarchy of VHDL record types, which allows to minimize code changes during optimization of the algorithm [3].

The GPs resulting from physical Monte Carlo simulations are stored in the XML file. Therefore a special tool written in Python is used to automatically generate VHDL files and memory initialization files describing other parameters of the algorithm including GPs and values of their PDFs.

Block diagrams of the OMTF Processor are shown in figures below.



Block diagram of the OMTF trigger processor firmware



Block diagram of the Golden Pattern Unit (GPU) calculating the PDF values for the group of patterns

Results

Currently the algorithm implemention is still under development but reaches already its functional state.
The OMTF Processor was successfully synthesized for the XC7VX690T chip available in the MTF7 board.
The chip occupancy is as follows:

- Slices used: 94.48% (102319 from 108300 available)
- Slice LUTs: 64.88% (281040 from 433200 available)
- Slice Registers: 32.87 % (284752 from 866400 available)
- Block RAM tiles: 51.22% (753 from 1470 available)

Due to the fact, that synthesis of the OMTF firmware is a time consuming process (typically ca. 8 hours on 8 cores 64GB Xeon machine), it is important, that correctness of the algorithm after any modification may be done in simulation. Therefore a dedicated environment for generation of input data end expected results from simulation XML files has been created.
Full verification of design, including timing has been also performed in a real hardware.
The tests - both in simulations and in hardware have confirmed correct operation of the OMTF trigger.

References

[1] CMS Collaboration, CMS Technical Design Report for the Level-1 Trigger Upgrade, no. CERN-LHCC-2013-011. CMS-TDR-12 in Technical Design Report CMS (Jun 2013).
[2] D. Acosta et al.; The CMS Modular Track Finder boards, MTF6 and MTF7, 2013 JINST 8 C12034 (Dec. 2013), doi:10.1088/1748-0221/8/12/C12034
[3] W.M. Zabołotny et al., FPGA implementation of overlap MTF trigger: preliminary study, Proc. SPIE 9290, 929025 (Nov, 2014); doi:10.1117/12.2073380.