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Algorithm and implementation of muon trigger and data transmission system for barrel-endcap overlap region of the CMS detector

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The CMS experiment is currently undergoing upgrade of its trigger, including the Level-1 muon trigger. In the barrel-endcap transition region it is necessary to merge data from 3 types of detectors - RPC, DT and CSC. The Overlap Muon Track Finder (OMTF) uses the novelty approach to concentrate and process those data in an uniform manner. The paper presents the algorithm and FPGA firmware implementation of the OMTF and its data transmission system in CMS. The OMTF is subject to significant changes during optimizations based on physical simulations. Therefore a special, high level, parametrized HDL implementation is necessary.

Summary

The CMS experiment is currently undergoing upgrade of its trigger, including the Level-1 muon trigger. In the barrel-endcap transition region it is necessary to merge signals from 3 types of detectors - RPC, DT and CSC. The Overlap Muon Track Finder (OMTF) is a dedicated system analyzing the data received from those detectors and finding muon candidates.

The data acquired from different detectors are transferred via links operating at various speeds (1.6, 3.2 or 10 Gb/s) and in different modes (synchronous or asynchronous).
Therefore, dedicated blocks for time alignment of acquired data are needed.
The system is controlled with IPbus protocol via 1 Gb/s Ethernet link.

To allow uniform processing of the acquired data, hit data from each detector are converted into azimuthal angles and compared with the track patterns, prepared basing on physical simulations. Benefiting from the cylindrical symmetry of detector it was possible to minimize number of track patterns.

The single OMTF processor receives data from 70 degrees range of azimuthal angle (with 10 degrees overlap between neighbouring processors). Therefore 6 OMTF processors are used to form the whole OMTF system.

Dedicated pipelined architecture is implemented in VHDL to allow simultaneous parallel comparison of detected hits with multiple patterns and to select the best matching pattern.

Due to the fact that the pattern definitions and details of the detection algorithm are adjusted in the development process, a special flexible implementation is needed. Additionally to fully utilize logic resources offered by the FPGA chip, it is necessary to allow synthesis tools to optimize the pattern comparing units basing on regularities of the patterns. Resulting high level, parametrized description of the algorithm is an attempt to satisfy both mentioned requirements.

In order to find multiple muon candidates in each bunch crossing, the system has to operate at the multiplied LHC clock frequency. To ensure high speed operation in the modern, complex Virtex 7 FPGA device, the low level details of implementation have been thoroughly adjusted. In current state, the operation at 160 MHz clock is achieved, allowing each OMTF processor to find up to 4 muon candidates every bunch crossing.

To speed up development and testing, a dedicated environment was created allowing to verify the algorithm and track patterns in behavioral simulation, (which allows quick verification), and in real hardware.

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