Ongoing studies for the control system of a serially powered ATLAS pixel detector at the HL-LHC

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In terms of the Phase-2 Upgrade of the ATLAS detector, the entire inner tracker (ITK) of ATLAS will be replaced. This includes the pixel detector and the corresponding detector control system (DCS). The current baseline is a serial powering scheme of the detector modules. Therefore a new detector control system for ATLAS pixel is being developed with emphasis on the supervision of serially powered modules and radiation tolerance. The concept of the DCS for ATLAS pixel after the Phase-2 upgrade is presented, as well as the status of development including tests with the prototype ASIC.

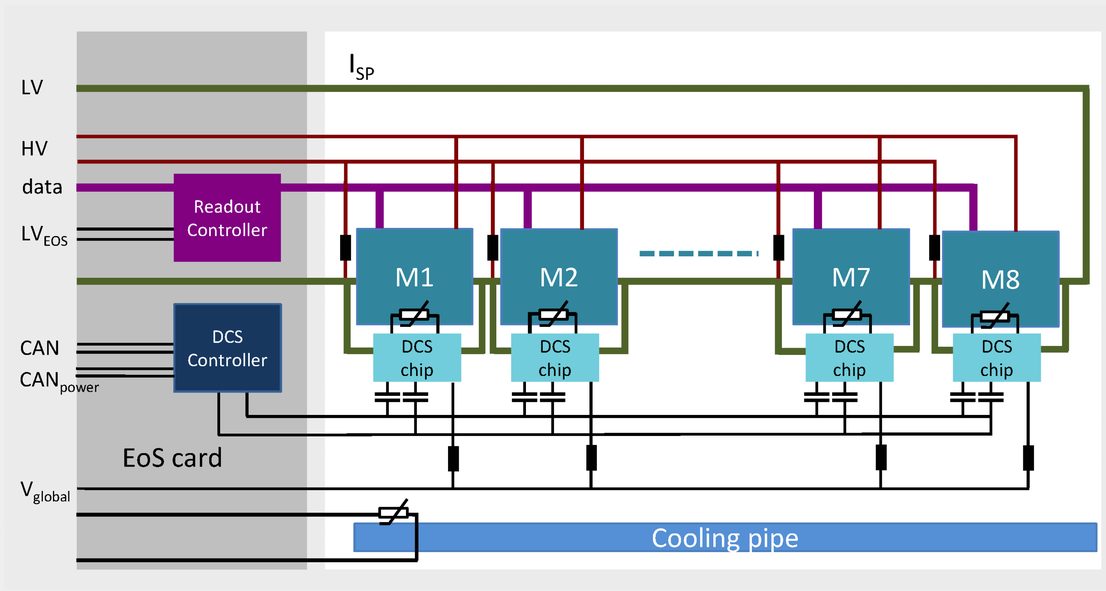
TWEPP 2015 Topical Workshop on Electronics for Particle Physics
28 September – 02 October 2015
IST Lisbon, Portugal

Requirements

- Support serial powering concept
  - protects against over-voltage
  - allows to turn on/off individual module
  - operated at different voltage potentials
  - (AC coupled)
- independent operation
- local monitoring
- as few cables as possible
- small material budget
- low power consumption
  - operation without cooling
- robust communication interface
- radiation hard
  - as the innermost layer of the pixel detector

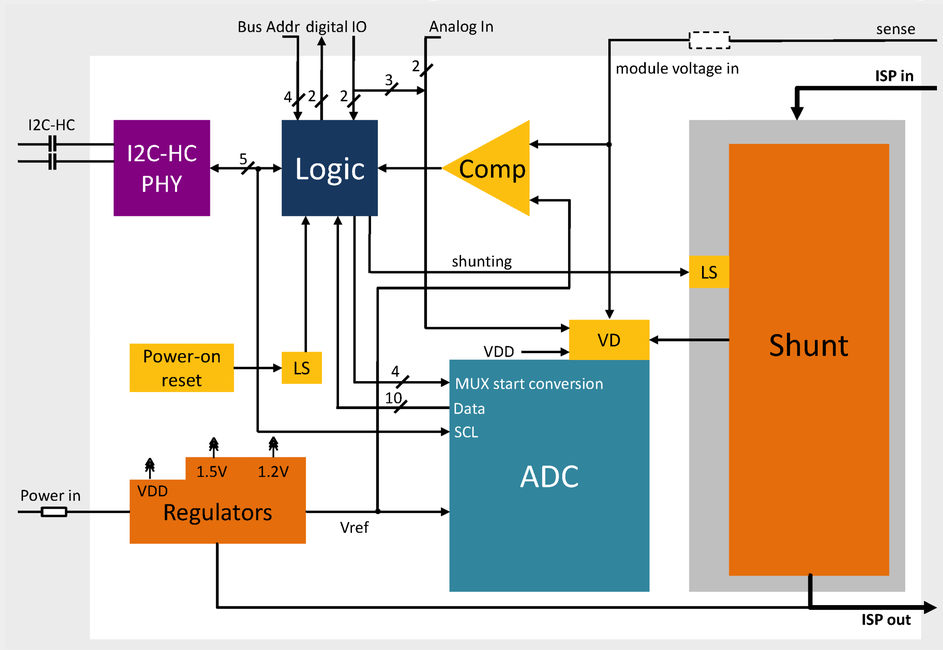
Serially powered stave

- all services are routed through End of Sub-structure card
- all modules of a half stave share one LV current source
- LV distributed serially
- challenge for DCS: all modules on different potential
- 3 connecting lines along the support structure for DCS



DCS Chip: Pixel Serial Powering Protection chip

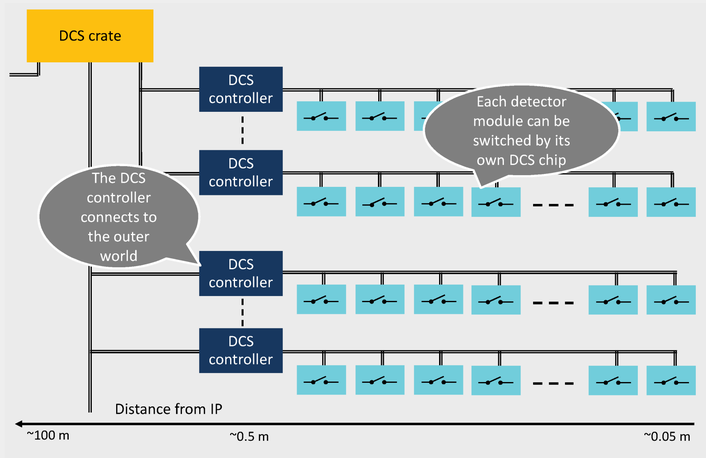
- Voltage regulators
- Over voltage comparator
- Power-on reset
- Shunt transistor (@ 0 to 2.4 A)
- 2 ADC channels 10 bit
  - 5 voltage deviders (VD)
- 2 digital Inputs, 2 digital Outputs
- logic block
  - modified I2C slave
  - Hemming code for error detection
  - not permanently clocked
- AC coupled I2C-HC physical layer
- 130 nm CMOS technology
- Level shifters (LS)
- size of PSPPv2: (1.75 x 1,27) mm²



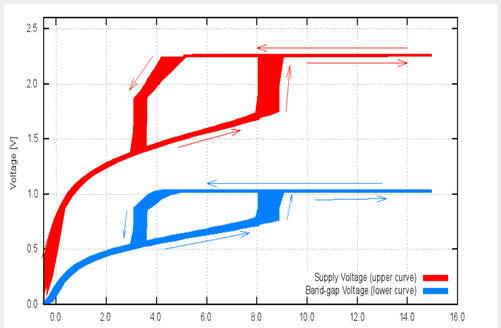
Inherited components from SPP and FEI4 chips, see proceedings for details

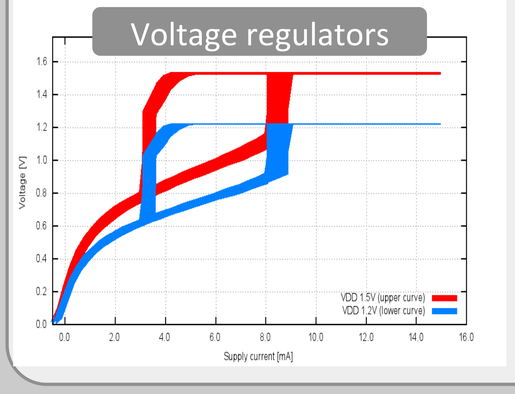
DCS Network

- DCS controller
  - CAN node
  - CAN I2C-HC Bridge
- AC coupled to DCS chip
- located at the EoS card



Tests and Status



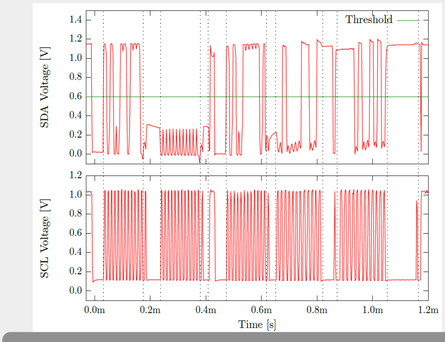


Voltage regulators

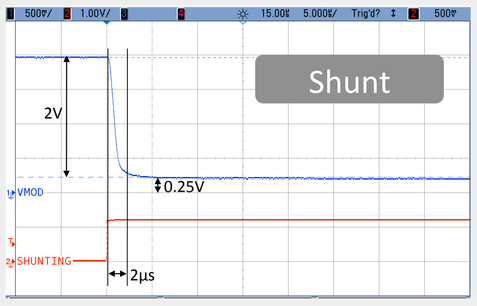
- As prove of principle
- Submission of PSPPv1 Nov 2013
- Minor bugs required workaround

- studied intensively in test setup
- Regulator variations measured for 6 chips
- Active regulator stable by ≈ 0.14%
- Stable communication
- Switching time of shunt fast enough

- Successful tests with a real detector module:
  - Shunting by command
  - Over voltage protection
  - Influence on threshold
  - Influence on noise



I2C-HC communication



Shunt

- Submission of PSPPv2 May 2015
- bugs fixed
- build system with large number of nodes
- test for long-term stability
- continue with rad-hard design (e.g. TMR)

Layout of PSPPv2