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Ongoing studies for the control system of a serially powered ATLAS pixel detector at the HL-LHC

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In terms of the Phase-2 Upgrade of the ATLAS detector, the entire inner tracker (ITK) of ATLAS will be replaced. This includes the pixel detector and the corresponding detector control system (DCS). The current baseline is a serial powering scheme of the detector modules. Therefore a new detector control system for ATLAS pixel is being developed with emphasis on the supervision of serially powered modules and radiation tolerance. The concept of the DCS for ATLAS pixel after the Phase-2 upgrade is presented, as well as the status of development including tests with the prototype ASIC.

Summary

During a long shutdown in the beginning of the 2020s, when the LHC will be upgraded to the HL-LHC, the entire inner tracker of the ATLAS experiment at the LHC will be replaced. This also includes the innermost part of ATLAS, the pixel detector. The goal is to collect 3000/fb with this new detector. To ensure a stable and reliable operation for this time (˜10 years), there has to be a control system which steers and monitors the detector, similar to the detector control system (DCS) of the current pixel detector. Due to massive changes in the concept of the new pixel detector, the current DCS cannot be reused and a new one is being developed. This new DCS concept for the pixel detector contains three paths, a hard wired interlock path, a diagnostics path integrated into the data acquisition and a control and feedback path for user interactions during operation. In this contribution we describe an improved concept of the control and feedback path, especially designed for the case of a serially powered detector. Though the operation of a parallel powering scheme with DC-DC converters is also possible. The control and feedback path is made up by a network of two nodes: The first node, the DCS controller, is located at the end of each sub structure (disc or half stave). The second node, the DCS chip, is located closely each detector module. To cope with the high radiation levels and the low material budget, these nodes are implemented in custom made ASICs. Communication between these two nodes is transmitted by an I2C bus, which was enhanced with four check bits to provide better reliability. To meet the standards of the ATLAS DCS, the communication from the DCS chip to the DCS computers is realized by a CAN bus.

Besides the new concept, prototypes of the DCS chip, will be introduced. After promising tests with a first prototype, the PSPP chip, a second improved version, the PSPPv2 chip was developed. This chip contains all components, which are foreseen in the concept of the DCS chip. This includes the physical layer for an AC coupled two wire bus, a shunt regulator, a large shunting transistor, an ADC, I2C slave logic and a comparator. The PSPPv2 chip has recently been tested and the results will be presented.

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