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Rad-Hard Vertical JFET switch for the HV-MUX system of the ATLAS upgrade ITk

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This work presents a new silicon vertical JFET technology, based on the trenched 3D detectors developed at CNM, to be used as switches for the HV powering scheme of the ATLAS upgrade Inner Tracker. An optimization of the device characteristics is performed by TCAD simulations. Special attention has been paid to the on-resistance and the switch-off and breakdown voltages to meet the specific requirements of the system. The radiation damage mechanisms have been simulated to ensure that the devices will remain operational through the whole experiment life-time. Finally, a description of the technological process will be shown.

Summary

The high-luminosity tracker upgrade of the LHC will demand a substantial improvement of both the radiation sensors and their associated electronics in the ATLAS experiment, in terms of performance, radiation hardness, and compactness. Specifically, the upgrade of the silicon strip sensors represents a large increase in area and in the number of sensors. Cable space limitations do not permit each sensor to be individually biased. Therefore, collections of sensors will need to share a common high voltage bias.
A High-Voltage Multiplexing (HVMUX) scheme has been proposed in which a failed sensor is disconnected from the bias bus in order to permit normal operation of the remaining sensors. Each sensor requires a slow-controlled switch that can survive the high radiation environment and operate in a high magnetic field, and is capable of switching more than 500V.
This work presents a new silicon vertical JFET switch, based on the trenched technology developed at the CNM for 3D-detectors, which fulfils the HVMUX specifications. This VJFET, produced on a high-resistivity p-type substrate, is conceived as a cellular device, where each cell presents a conduction channel, surrounded by a deep trench with circular or hexagonal layout. The trenches, typically less than 100 µm deep, are filled with highly-doped n-type polysilicon to form the gate electrode. The source electrode is implemented with a highly-doped p-type diffusion localised at the centre of each cell. The drain electrode is performed on the backside with a blanket implant, far away from the trenches, which gives the device a voltage capability above 1000V.
In normal operation, Gate-to-Source Voltage is held at 0V, allowing a current flow through the cell channel. If VGS is increased above the threshold value (VOFF), the channel becomes fully depleted and the VJFET turns off. In fact, its operation in depletion mode (normally-ON) stands out among the main features of this device as it does not need a voltage to be applied on the device gate for the sensors to be biased. As it is a 3D device with vertical conduction, high voltage capability and low switch-off voltage are achieved, with a high radiation-hardness in terms of ionization damage. The layout configuration and the p-type substrate election will contribute to reduce the effects of radiation displacement damage. Finally, the cellular design and the custom fabrication will allow meeting the specifications for the ITk. Simulations have been already done in 2D and 3D configurations, confirming all these features.

A thorough TCAD simulation analysis of the device characteristics as a function of several geometric and technological parameters will be presented. The main figures of merit (RON, VOFF, and breakdown voltages) are evaluated considering the full device configuration and the edge termination strategy. In addition, simulation results on the mechanisms of radiation degradation will be presented, with a suitable procedure for its simulation. The final contribution will include several issues related with the process technology and a complete update of the fabrication procedure.

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