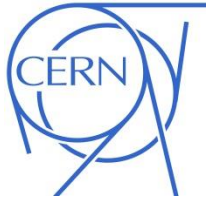
MPA-LIGHT:

Design and results of a 65 nm digital readout Macro Pixel ASIC prototype with on-chip particle recognition for the Phase II CMS outer tracker upgrade

A. Caratelli, **D. Ceresa**, R. Francisco, J. Kaplon, K. Kloukinas and A. Marchioro.

PH-ESE, CERN

TWEPP '15, Wednesday the 30th September, 2015



CMS was originally designed to run at
Luminosity = 1 x 10^{34} cm^{-2} s^{-1}

HL-LHC will improve up to
Luminosity = 7.5 x 10^{34} cm^{-2} s^{-1}

Phase II upgrades prepares CMS for HL-LHC

Technical Proposal for the Phase-II Upgrade of the CMS Detector: http://cds.cern.ch/record/2020886

Main Outer Tracker requirements:

+ POWER

Up to pile up = 200 → Pixelated sensor

L1 rate = 750 KHz → Larger bandwidth

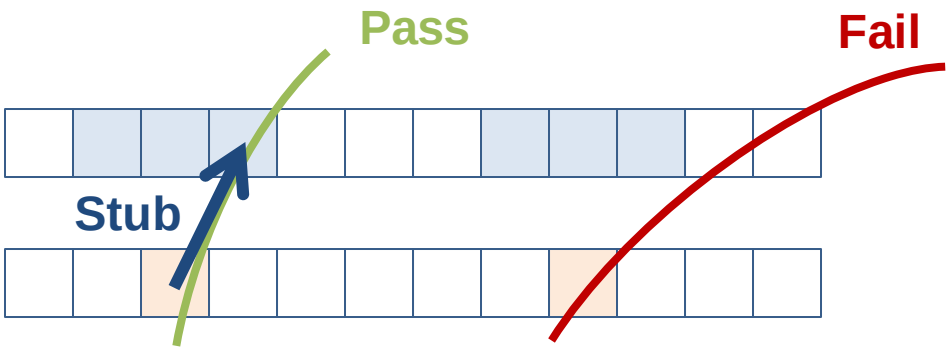
L1 Latency = 12.8 us → Larger buffers

Contribution to Level 1 decision → **P_T modules**

New technologies ← Reduce Material

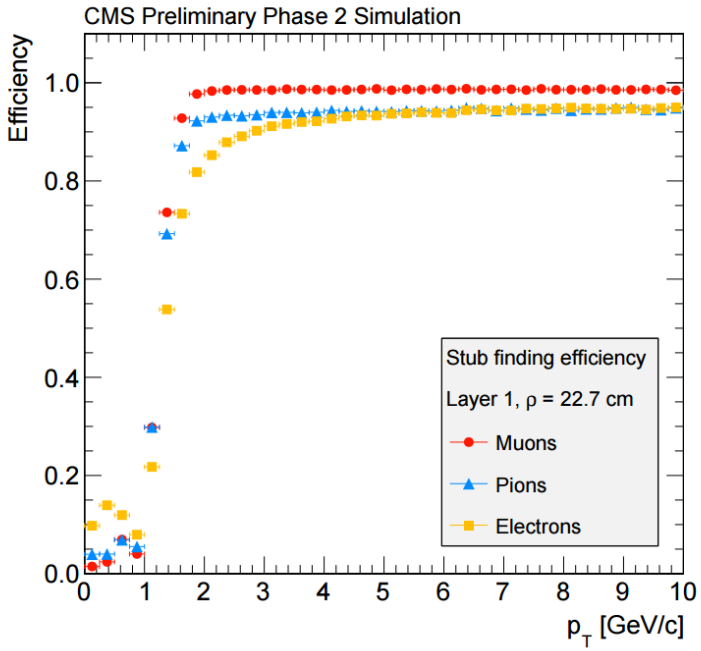
- POWER

P_T module discriminates particle



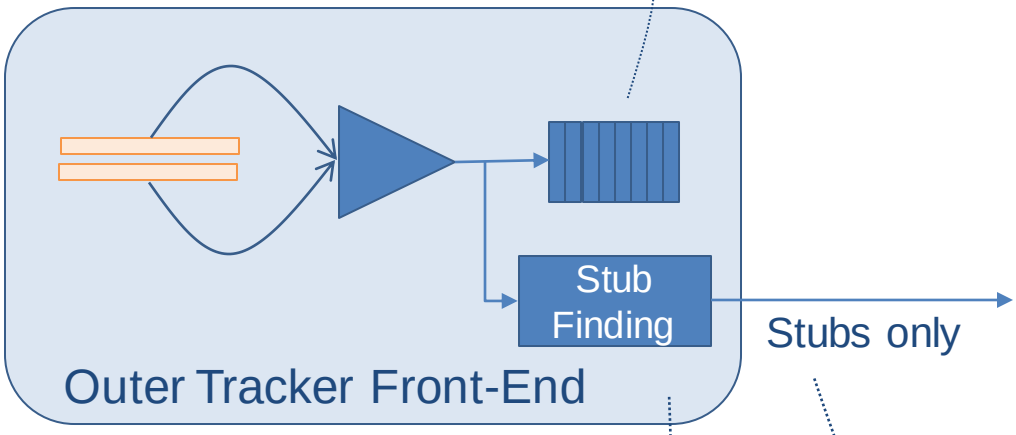
The module is composed by two sensor layers

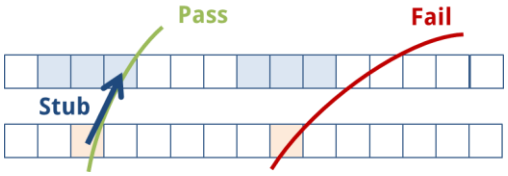
Particle are discriminated according to their transverse momentum



Outer Tracker working principle:

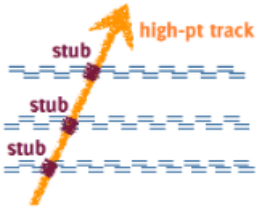
Triggered readout:
The electronics stores the full frame at each event.



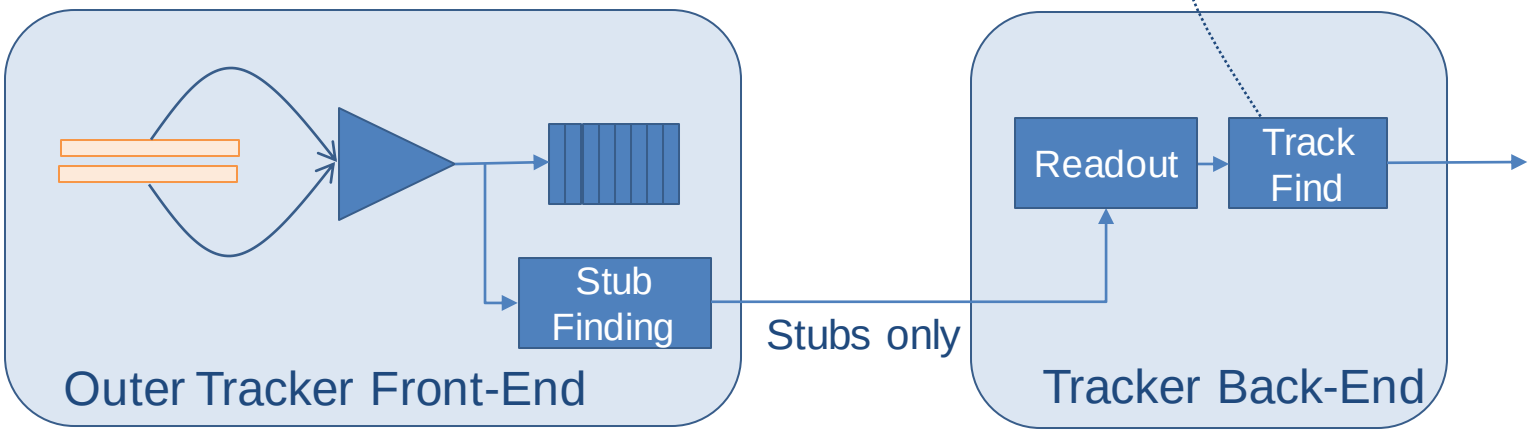


Trigger-less readout:
The electronics provides the stubs found at each event.

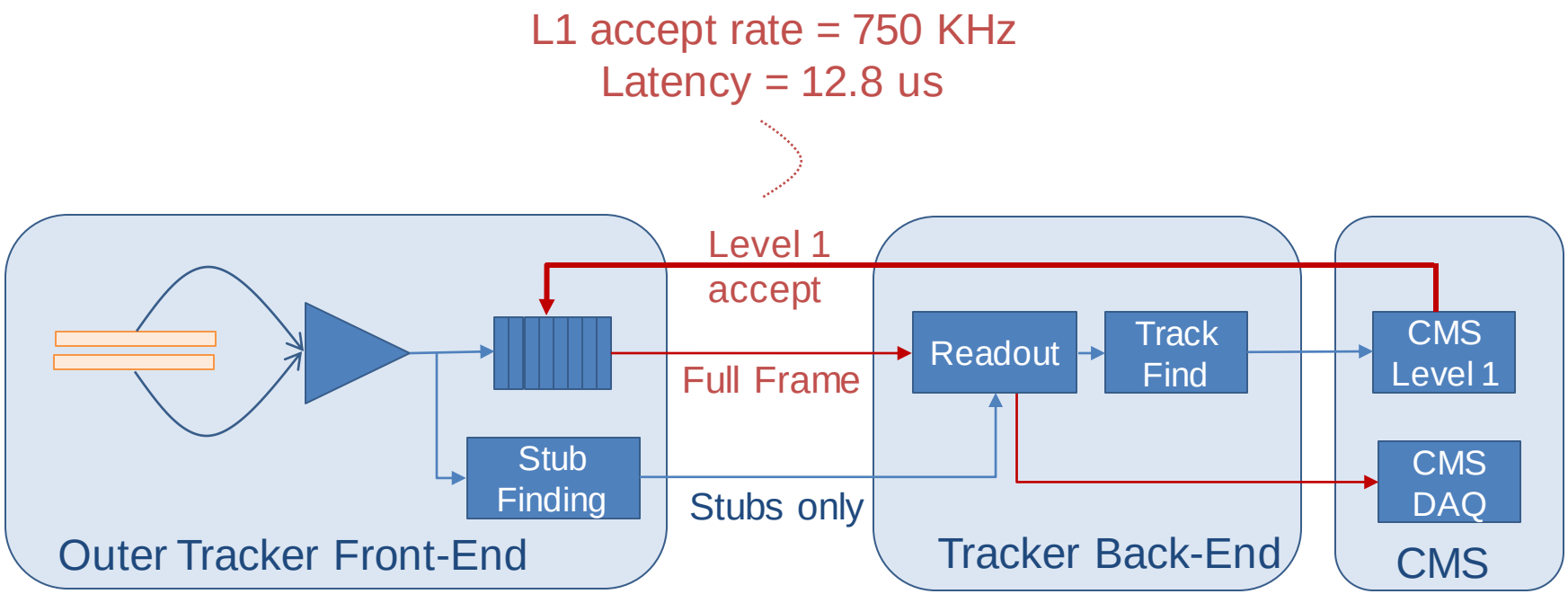
Outer Tracker working principle:



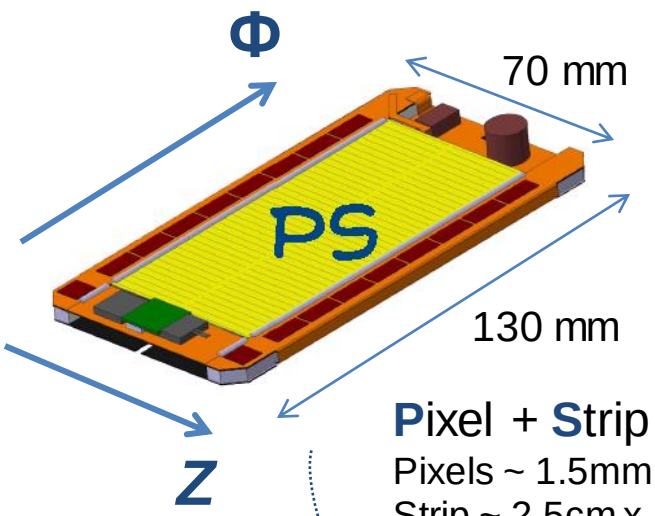
Dedicated talk: “Track Finding in CMS for the Level-1 Trigger at the HL-LHC”, M. Pesaresi



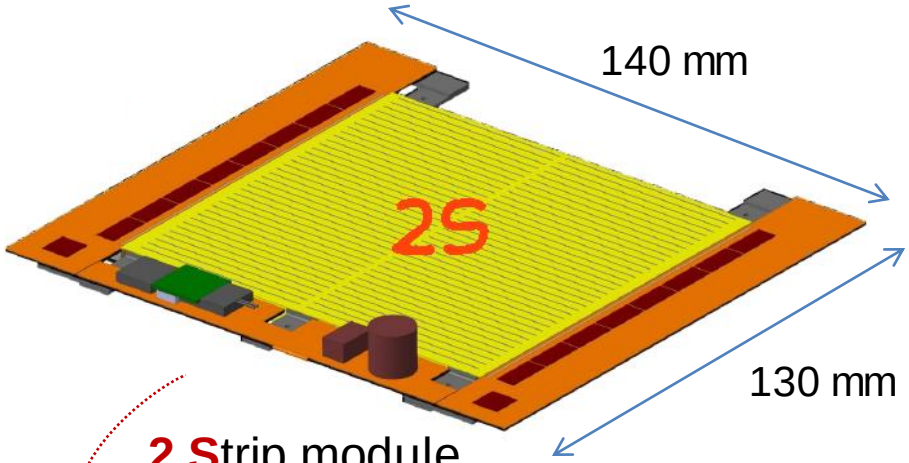
Outer Tracker working principle:



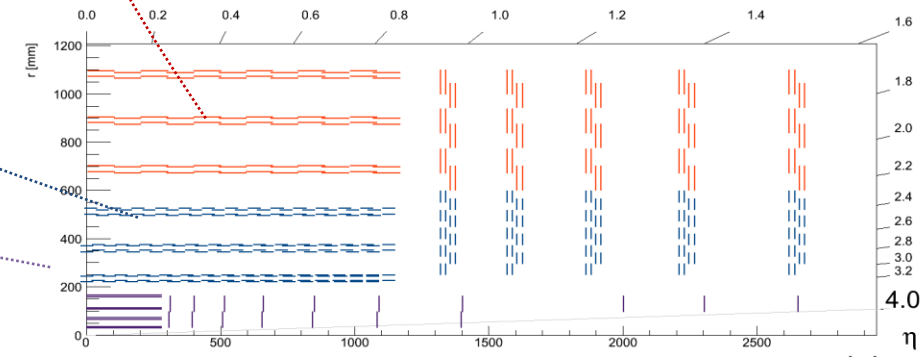
2 x P_T modules:



Pixel + Strip module
Pixels ~ 1.5mm x 100um
Strip ~ 2.5cm x 100um
20 cm < r < 40 cm
TID ~ 100 Mrad



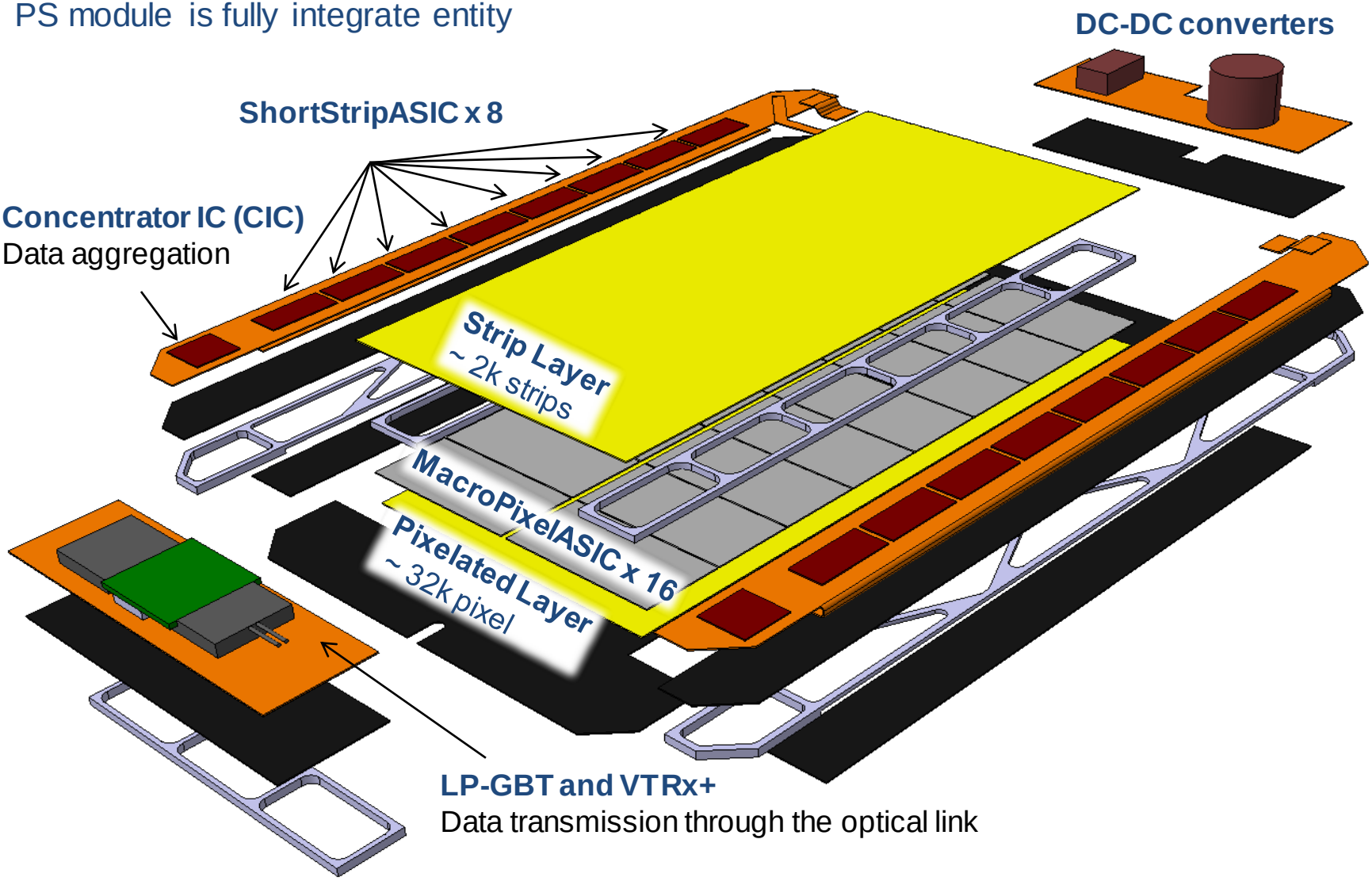
2 Strip module
Strips ~ 5 cm x 90 um
r > 40 cm
TID ~ 40 Mrad



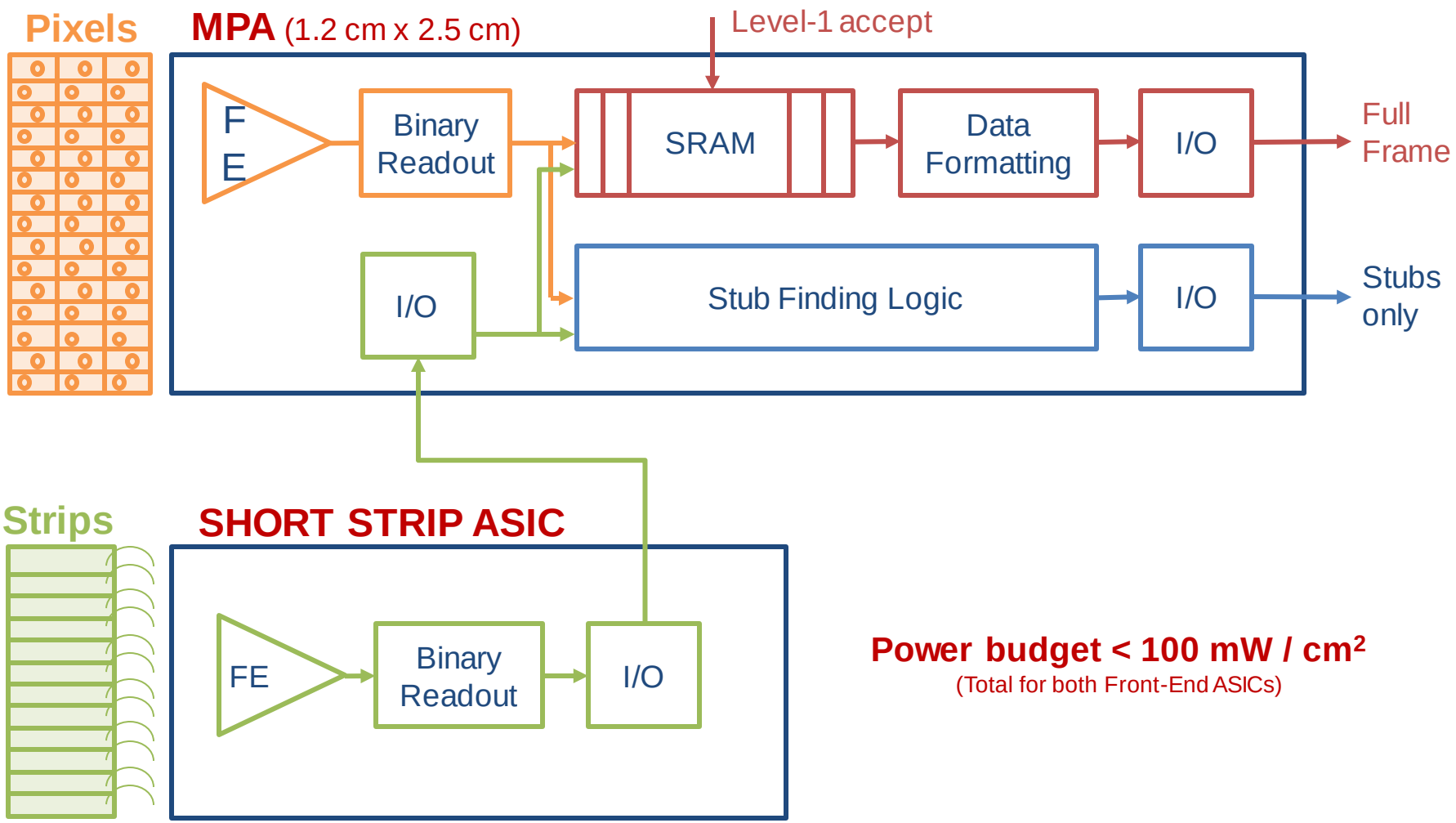
Inner Tracker (RD53)
Pixel Detector

Pixel + Strip module exploded view

PS module is fully integrate entity



Pixel Strip module Front-End ASICs



Power budget < 100 mW / cm^2
(Total for both Front-End ASICs)

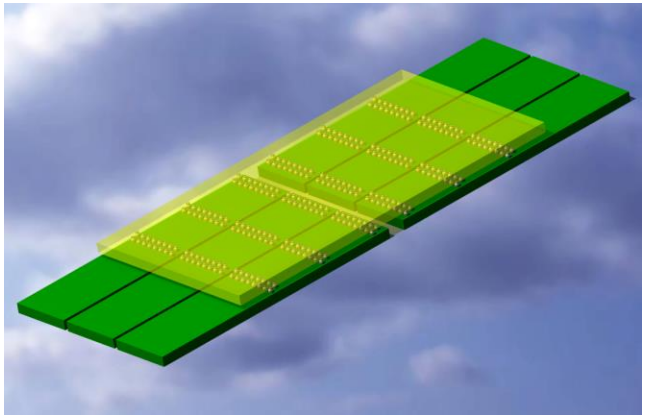
MPA-Light: the MPA prototype

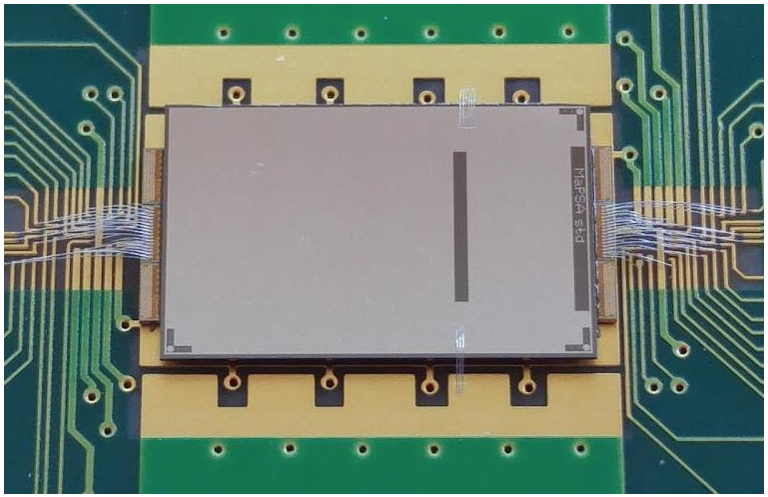
Analog FE circuitry in 65 nm

Development of the sensor

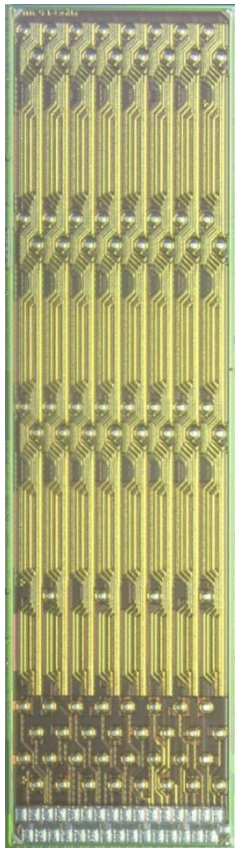
Module assembly

MaPSA-Light

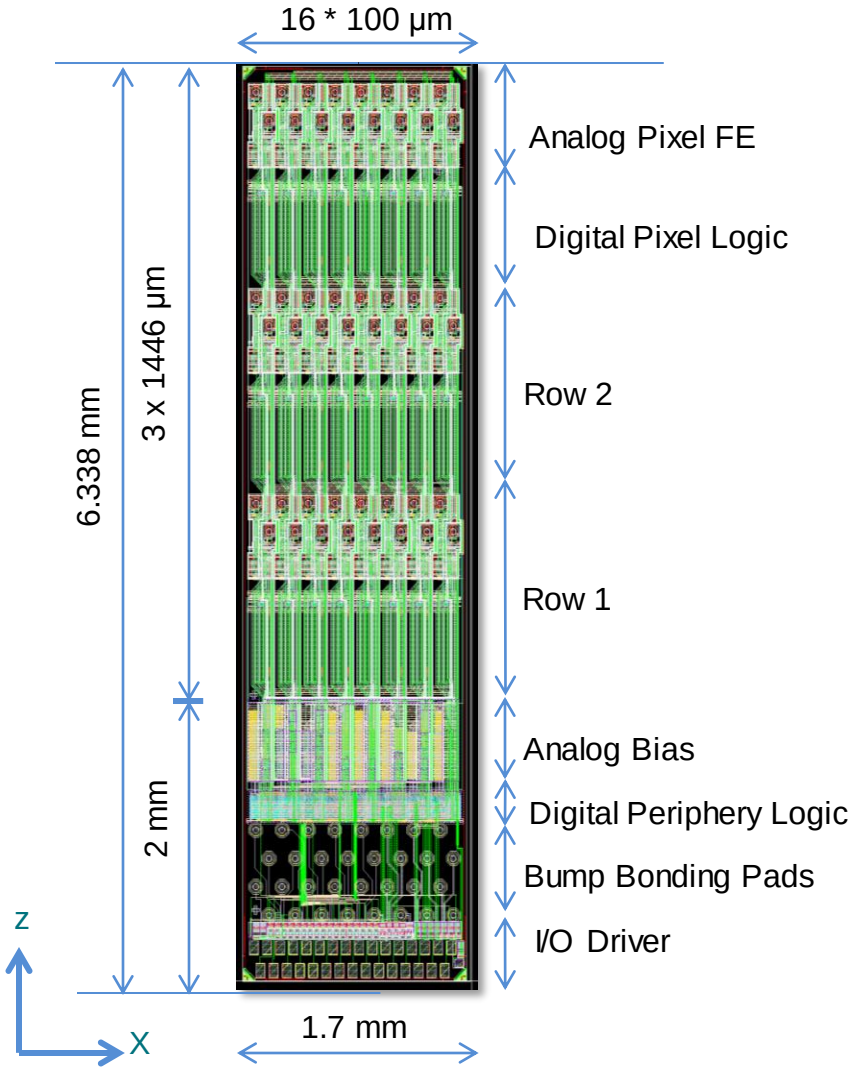


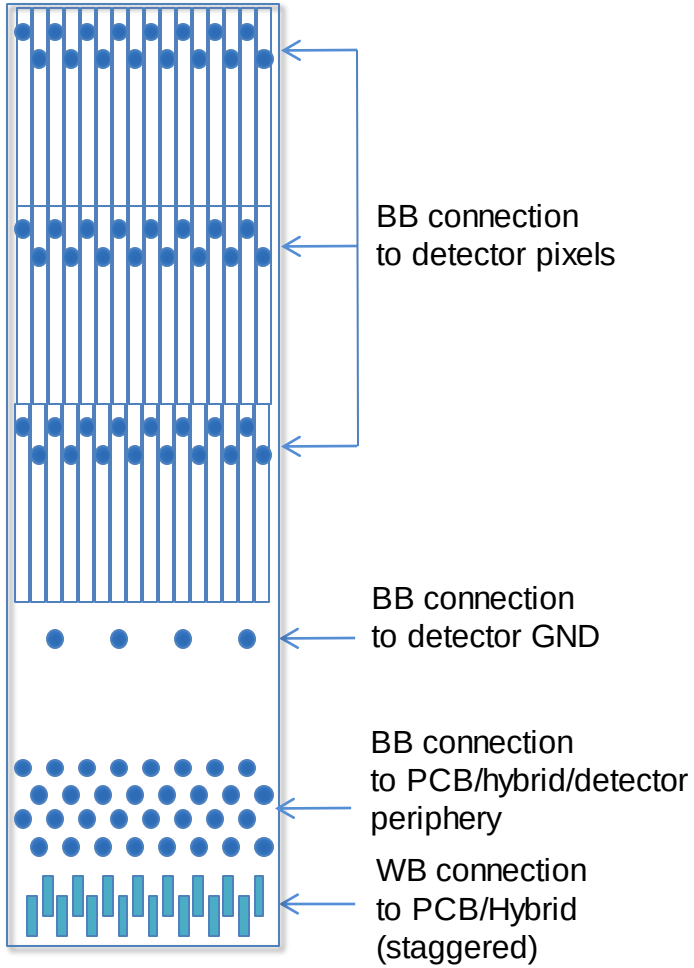


MPA-Light



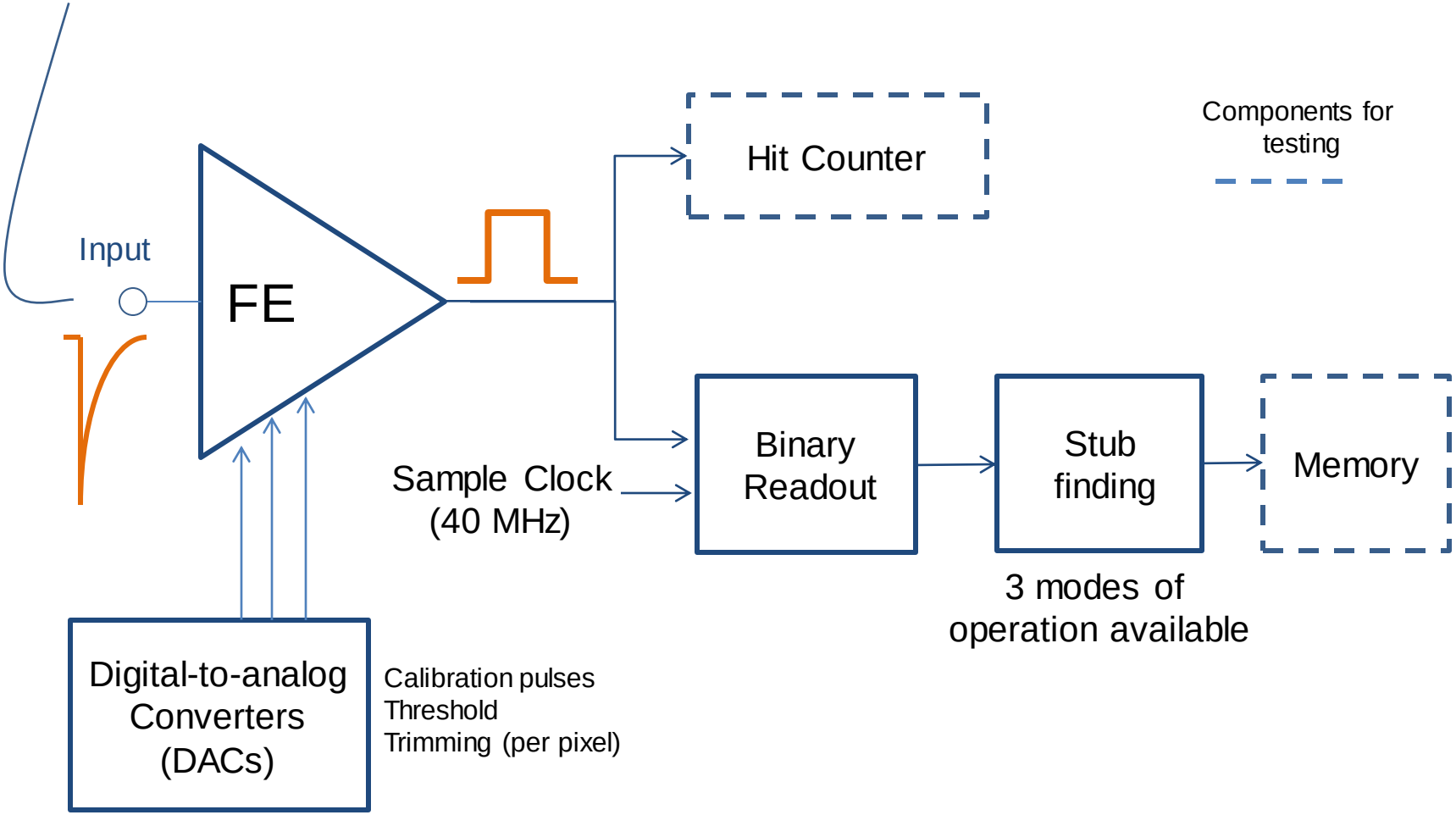
MPA-Light ASIC floorplan





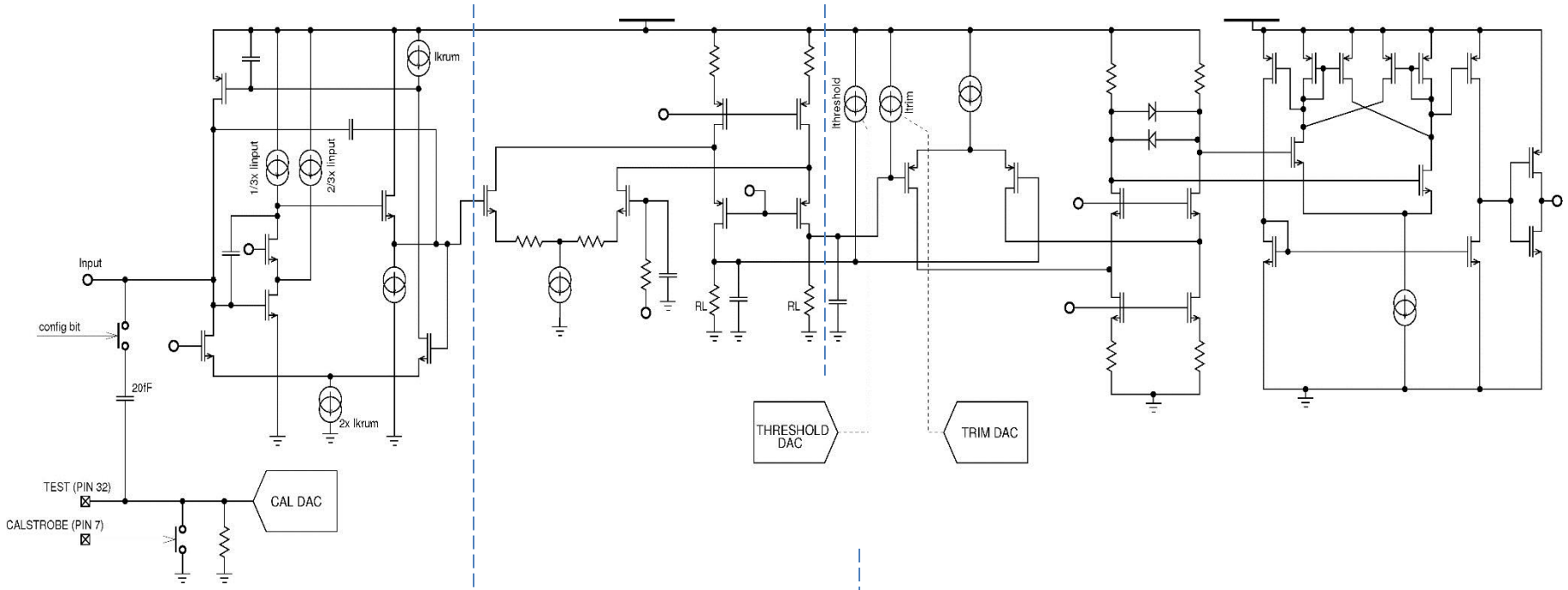
MPA-Light functional description

Test results are obtained without sensor i.e the input are from calibration capacitances



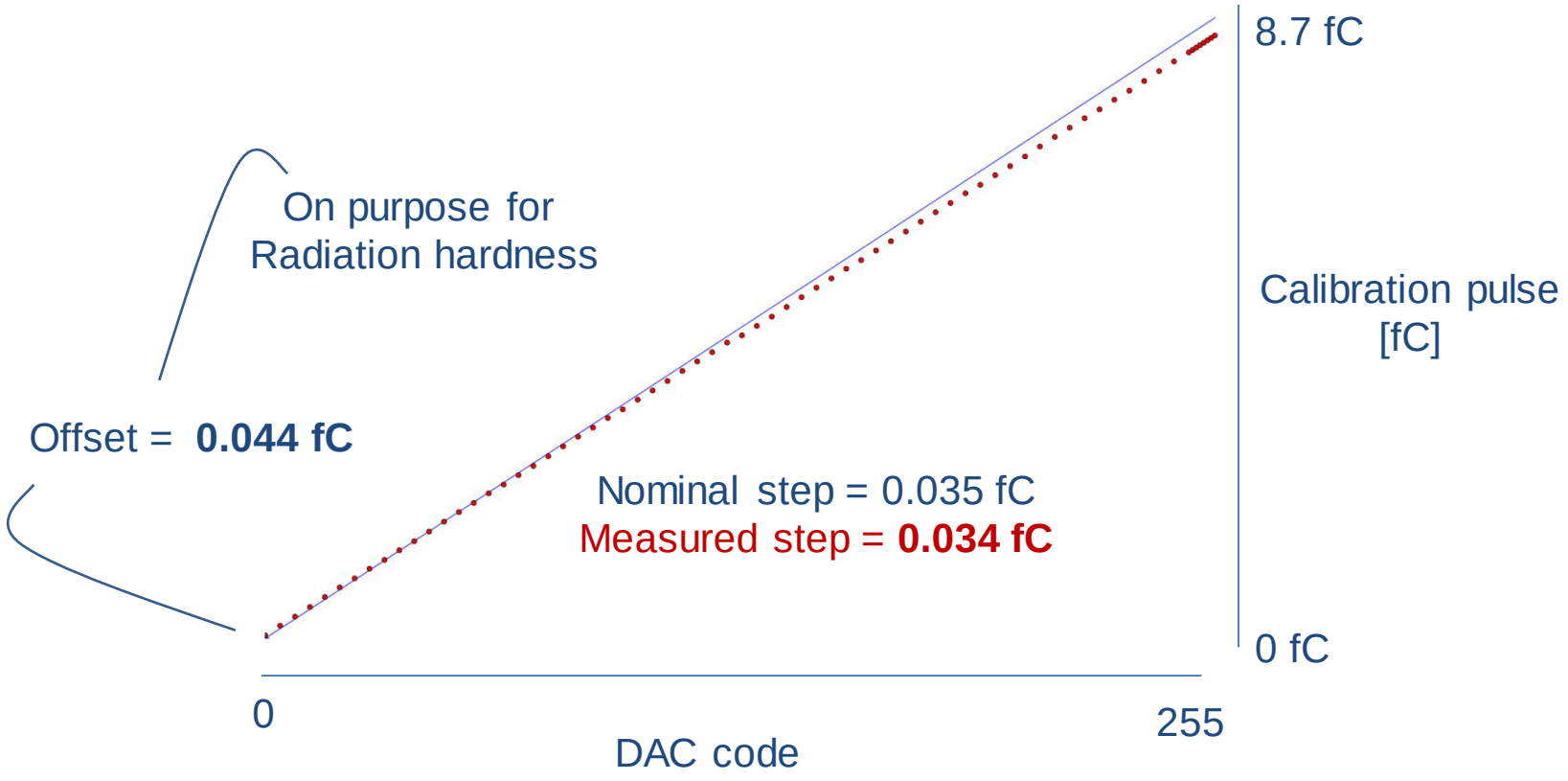
Analog Front-End schematic

designed by J. Kaplon

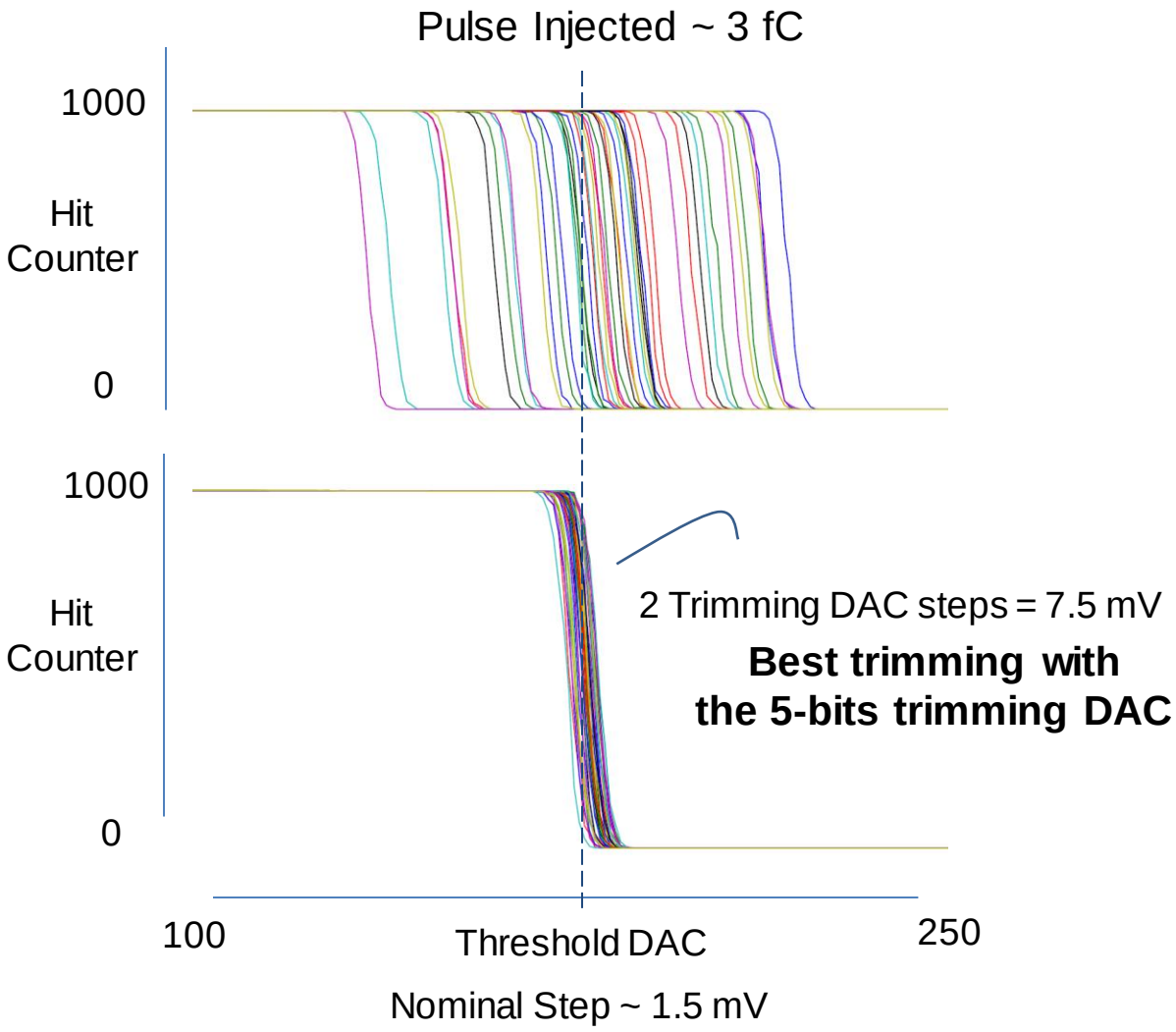


Current consumption < 30 uA / channel

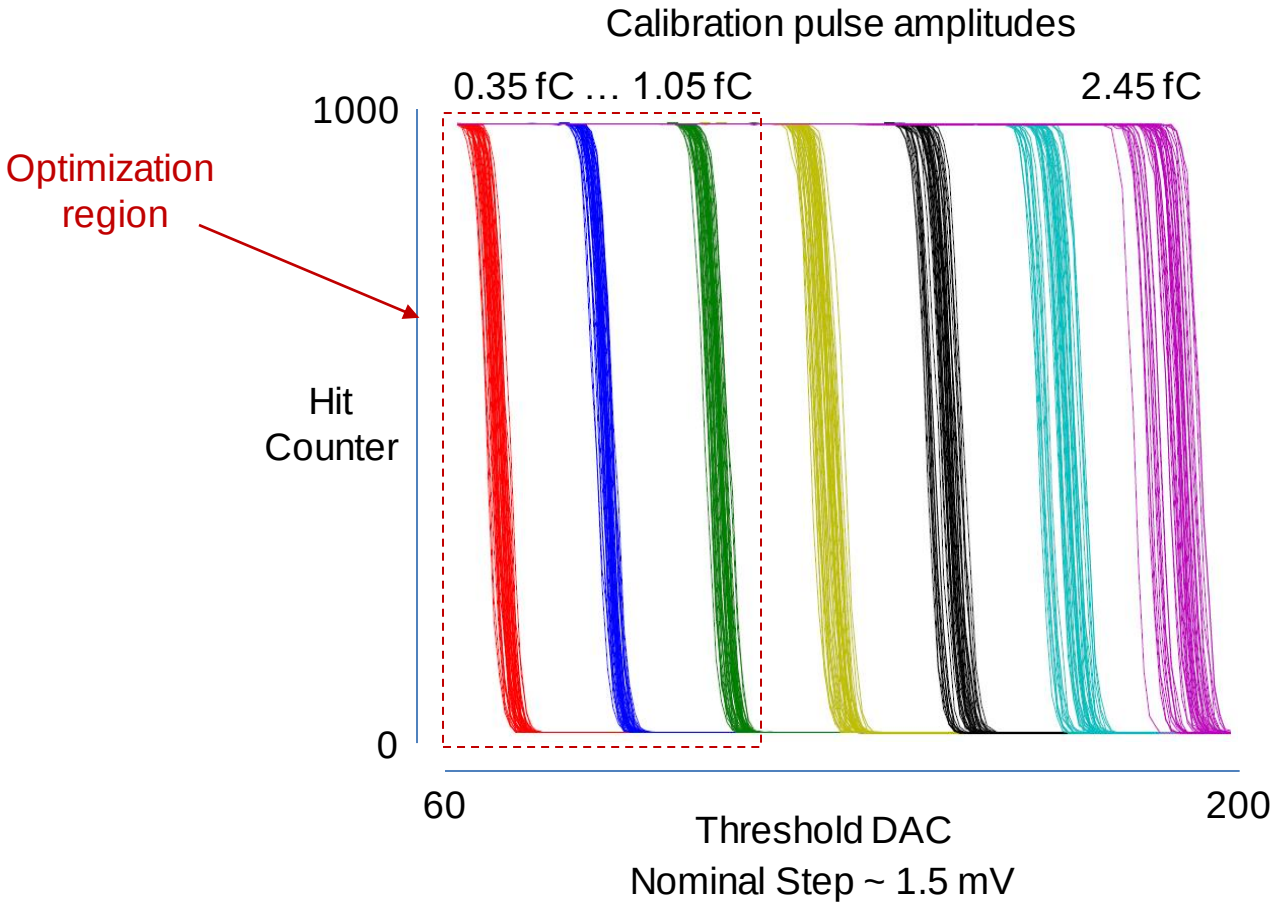
Calibration DAC measurement



Pixel Threshold spread

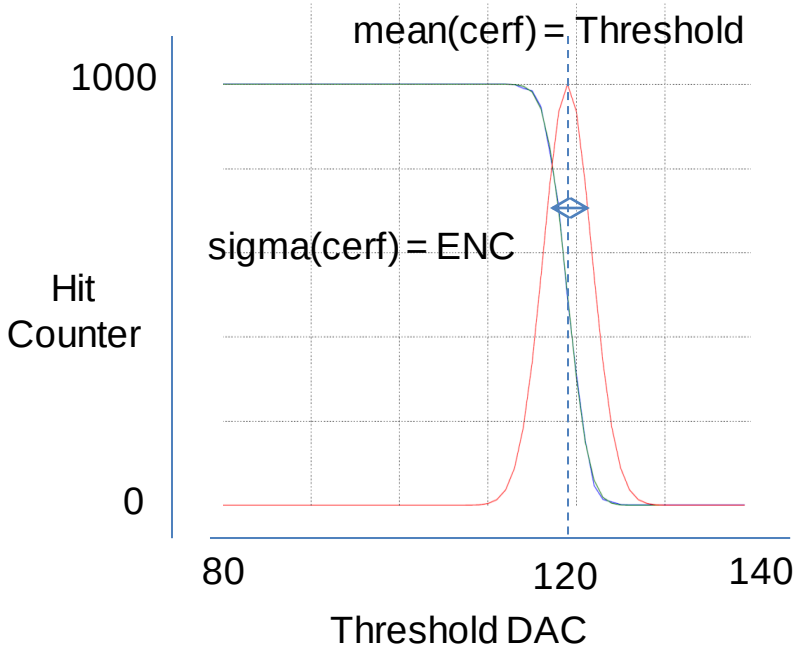


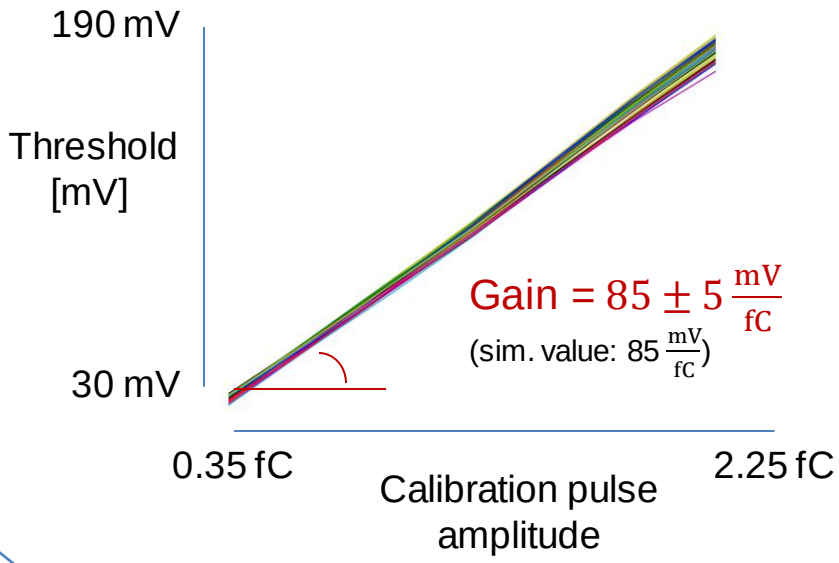
Gain and Noise from S-curves (1)



Gain and Noise from S-curves (2)

Complementary error function fitting



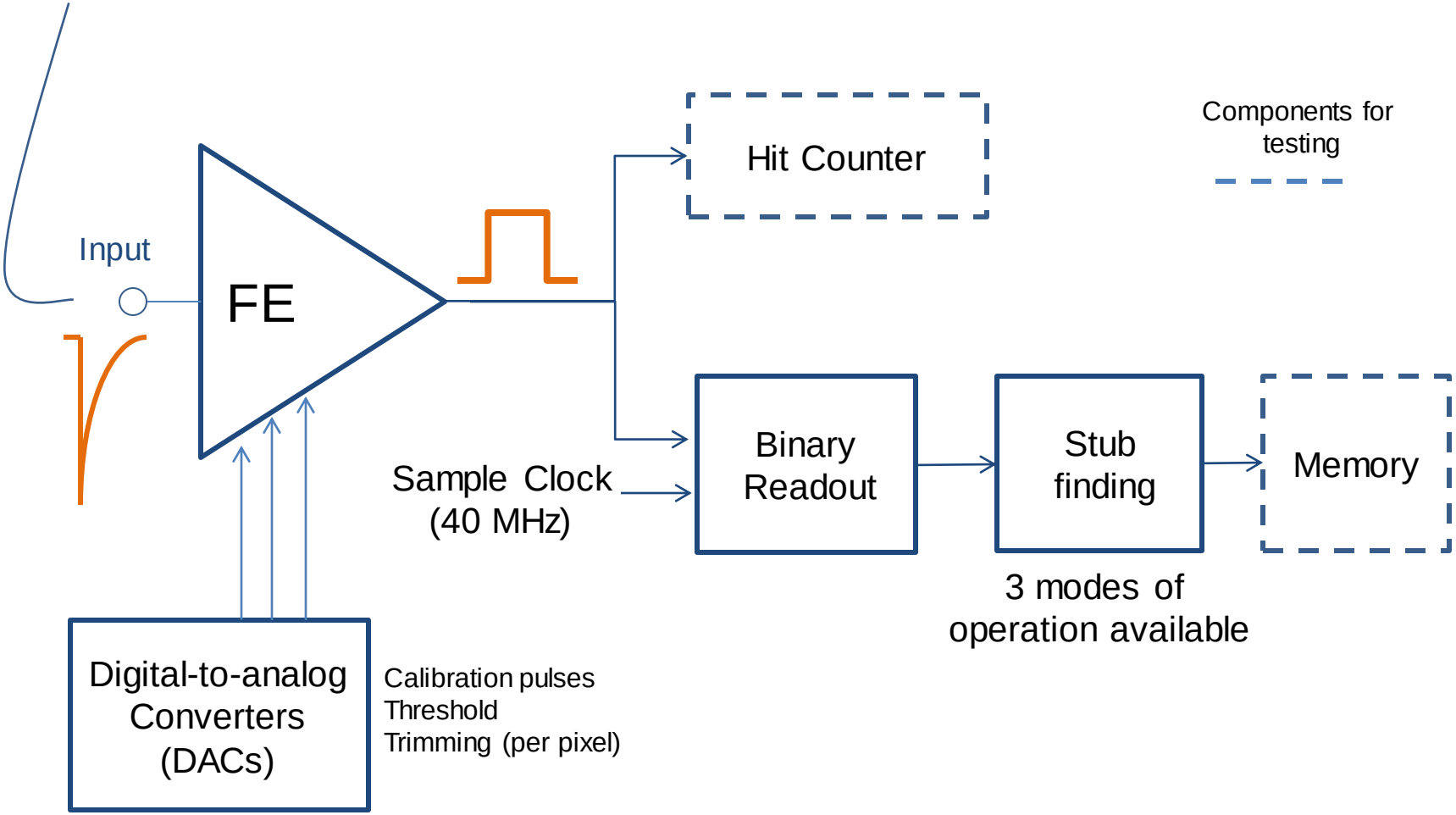


Equivalent Noise Charge = $276\ e^- \pm 27e^-$ (sim. value < 200 e^-)

SNR >> 20

MPA-Light functional description

Test results are obtained without sensor i.e the input are from calibration capacitances

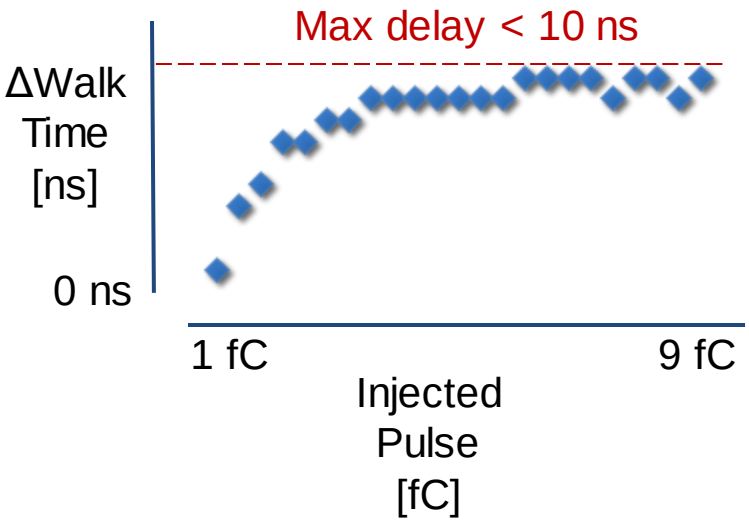


Binary readout allows FE studies:

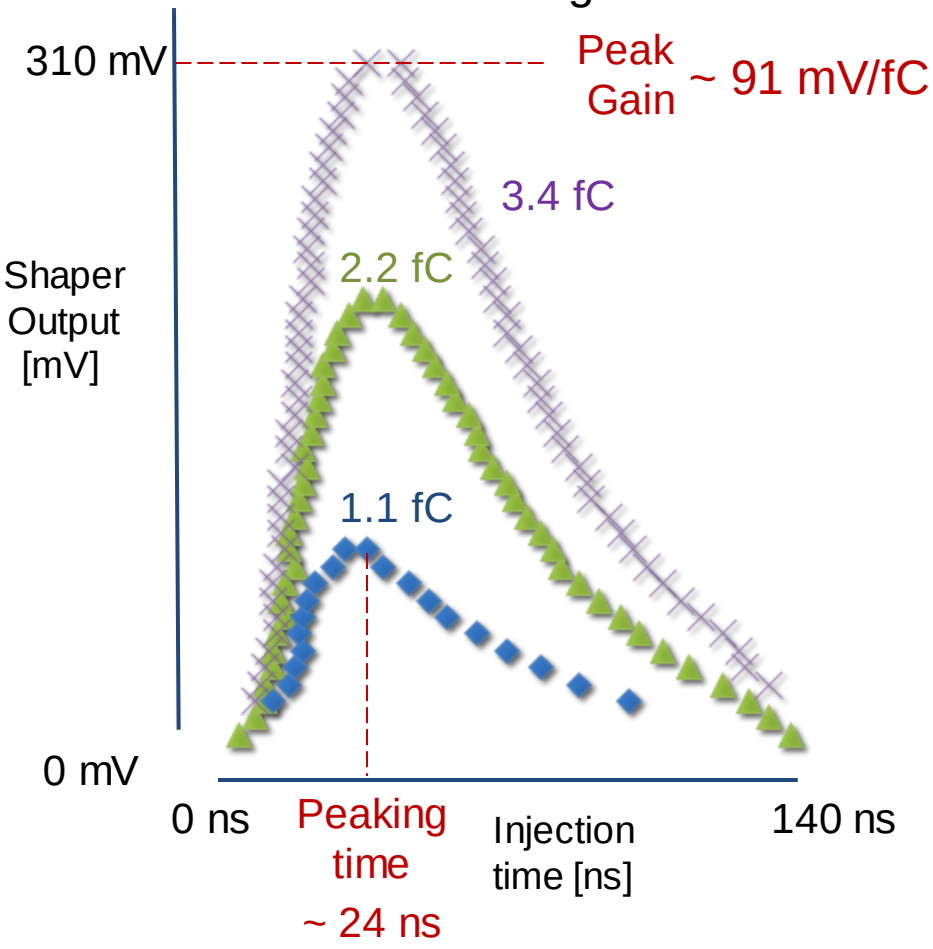
Simulations value:

- Time walk: < 14 ns from 0.5 fC to 12 fC
- Peaking time = 24 ns

FE walk time
(Threshold = 0.5 fC)



Shaper output
for different charge



MPA-Light digital logic testing

1. No Processing mode:
Used to test Binary readout
and Pixel Clustering

From
Binary readout

Z

1	**1**	**1**	0	0	0
0	0	0	0	0	0
0	**1**	**1**	**1**	0	0

X

MPA-Light digital logic testing

1. No Processing mode:
Used to test Binary readout
and Pixel Clustering

From
Binary readout
+
Pixel Clustering

Z

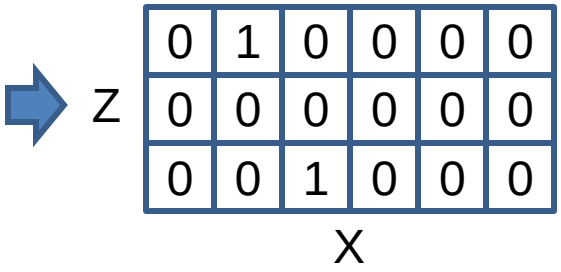
0	**1**	0	0	0	0
0	0	0	0	0	0
0	0	**1**	0	0	0

X

MPA-Light digital logic testing

From
Binary readout
+
Pixel Clustering

1. No Processing mode:
Used to test Binary readout
and Pixel Clustering



2. Data Processing mode:
Used to test Encoding
and Stub Finding Logic

Centroid List
X = 3, Z = 1
X = 2, Z = 3

MPA-Light digital logic testing

From
Binary readout
+
Pixel Clustering

1. No Processing mode:
Used to test Binary readout
and Pixel Clustering

Z

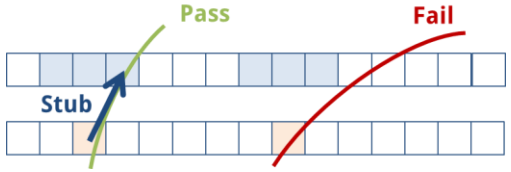
0	1	0	0	0	0
0	0	0	0	0	0
0	0	1	0	0	0

X

2. Data Processing mode:
Used to test Encoding
and Stub Finding Logic

Centroid List
X = 3, Z = 1
X = 2, Z = 3

Stub List
or X=3, Z=1, B=0
X=2, Z=3, B=-1



0	0	1	0	0	0

Tested with pattern from FPGA

Further details on the Stub finding logic: http://iopscience.iop.org/article/10.1088/1748-0221/9/11/C11012

MPA-Light digital logic testing

From
Binary readout
+
Pixel Clustering

1. No Processing mode:
Used to test Binary readout
and Pixel Clustering

Z

0	1	0	0	0	0
0	0	0	0	0	0
0	0	1	0	0	0

X

0	**1**	**1**	0	0	0

3. Strip Emulator mode:
Tested with oscilloscope

2. Data Processing mode:
Used to test Encoding
and Stub Finding Logic

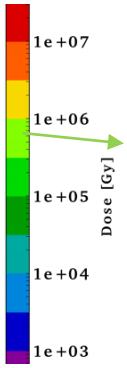
Centroid List
X = 3, Z = 1
X = 2, Z = 3

Stub List
or X=3, Z=1, B=0
X=2, Z=3, B=-1

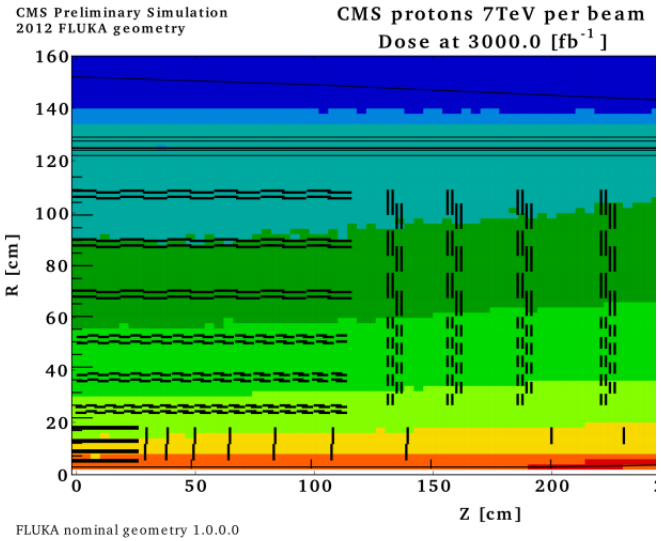
0	0	1	0	0	0

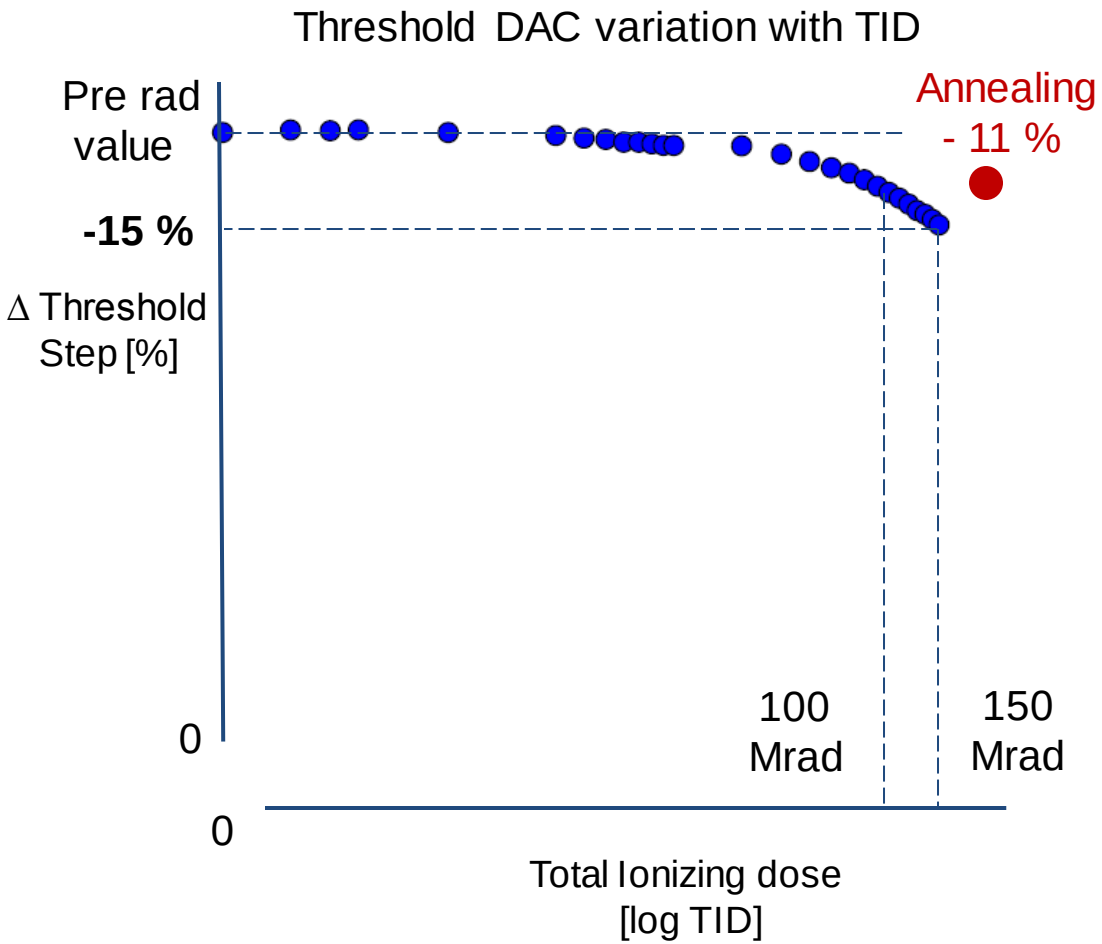
Tested with pattern from FPGA

Total Ionizing Dose (TID) with X-ray

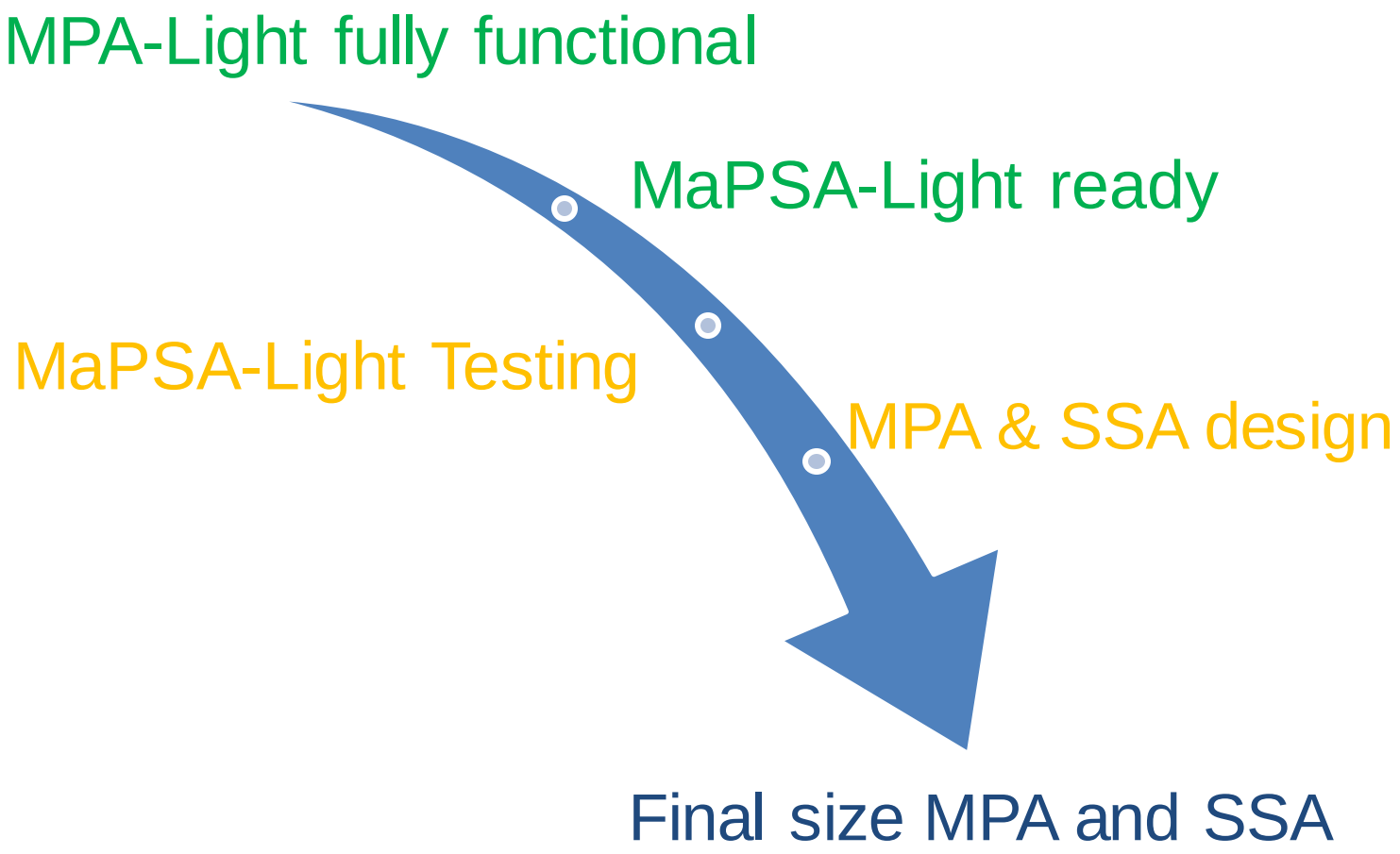


PS module
TID < 100 Mrad





Conclusion and future plans



Thanks to all the *CMS TRACKER PHASE II ELECTRONICS TEAM*

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PH-ESE-ME, CERN

TWEPP '15, Wednesday the 30th September, 2015

Backup slides

Davide Ceresa,
PH-ESE-ME, CERN

TWEPP '15, Wednesday the 30th September, 2015

Tracker Back-end **data transmission**

simulation and studies by S.Viret

TRG size (in bits)	Bend coding	Stub losses (in %)					
		All stubs			Good stubs		
		TOB 1	TOB 2	TOB 3	TOB 1	TOB 2	TOB 3
256	5	15.3	1.9	0.6	19.4	2.2	0.3
	3	12.3	1.3	0.5	15.9	1.4	0.2
	0	7.2	0.7	0.5	9.8	0.7	0.1
288	5	10.7	1.1	0.5	14.2	1.2	0.2
	3	8.2	0.8	0.5	11.1	0.8	0.1
	0	4.6	0.5	0.4	6.3	0.4	
312	5	8.2	0.8	0.5	11.1	0.8	
	3	6.1	0.6	0.5	8.4	0.5	
	0	3.3	0.4	0.4	4.6	0.3	
320	5	7.4	0.7	0.5	10.1	0.7	
	3	5.6	0.5	0.4	7.7	0.5	
	0	3.0	0.4	0.1	4.1	0.3	

	MPA/CBC bend bits	Proportion of PU4T (in%)	Stub losses (in %) Good stubs (pT>2/IP<1) TRG/RAW repartition (in bits) After CONC	
			TIB 1 10G-LEC 768b/128b	TIB 2 LP-LEC 384b/64b
PU140/T2-SB	4/4	10		
	3/3	10	0.2+/-0.4	0.0+/-0.5
PU140/T3-SB	4/4	10		
	3/3	10	0.1+/-0.5	0.0+/-0.5
PU200/T2-SB	4/4	10		
	3/3	10	0.5+/-0.3	0.3+/-0.4
PU200/T3-SB	4/4	10		
	3/3	10	0.2+/-0.4	0.1+/-0.4

Stub transmission to tracker back-end is clearly critical for the first barrel layer

Reduced thanks to:
Bend bits reduction
Tight Stub threshold
Different LP-GBT transmission mode

Good stub losses lower than 0.5% in all the tracker at Pile Up 200

Tracker power budget is limited

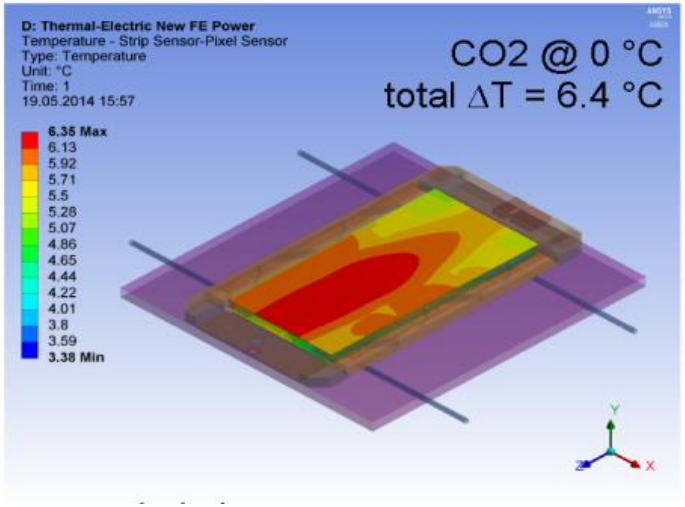
Total Power Allocated per 16 MPAs and SSAs: **4W**

Total Power Allocated per MPA + SSA: **250 mW**

Rough Power Estimation:

Analog	70 mW
L1 Memory	70 mW
SSA	40 mW
Remaining	**70 mW**

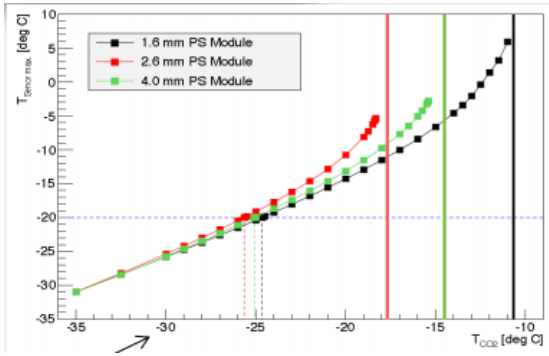
- I/O
- Clock Distribution
- Data Transport
- Stub Finding Logic
- L1 Data Logic
- Output Interface



PS Module Masses

1.6 mm		2.6 mm		4.0 mm	
AL-C V2-4	2.70	AL-C V2-4	4.39	AL-C V2-4	6.26
CFRP	4.41	CFRP	4.41	CFRP	4.41
Glue	2.17	Glue	2.19	Glue	2.18
Hybrid	1.76	Hybrid	1.82	Hybrid	1.90
Parylene	0.10	Parylene	0.10	Parylene	0.10
Sensors	4.54	Sensors	4.54	Sensors	4.54
Chips	2.70	Chips	2.70	Chips	2.70
GBT/DCDC	0.75	GBT/DCDC	0.75	GBT/DCDC	0.75
	19.13	+ 1.75 g	20.90	+ 1.95 g	22.84

all masses are in grams

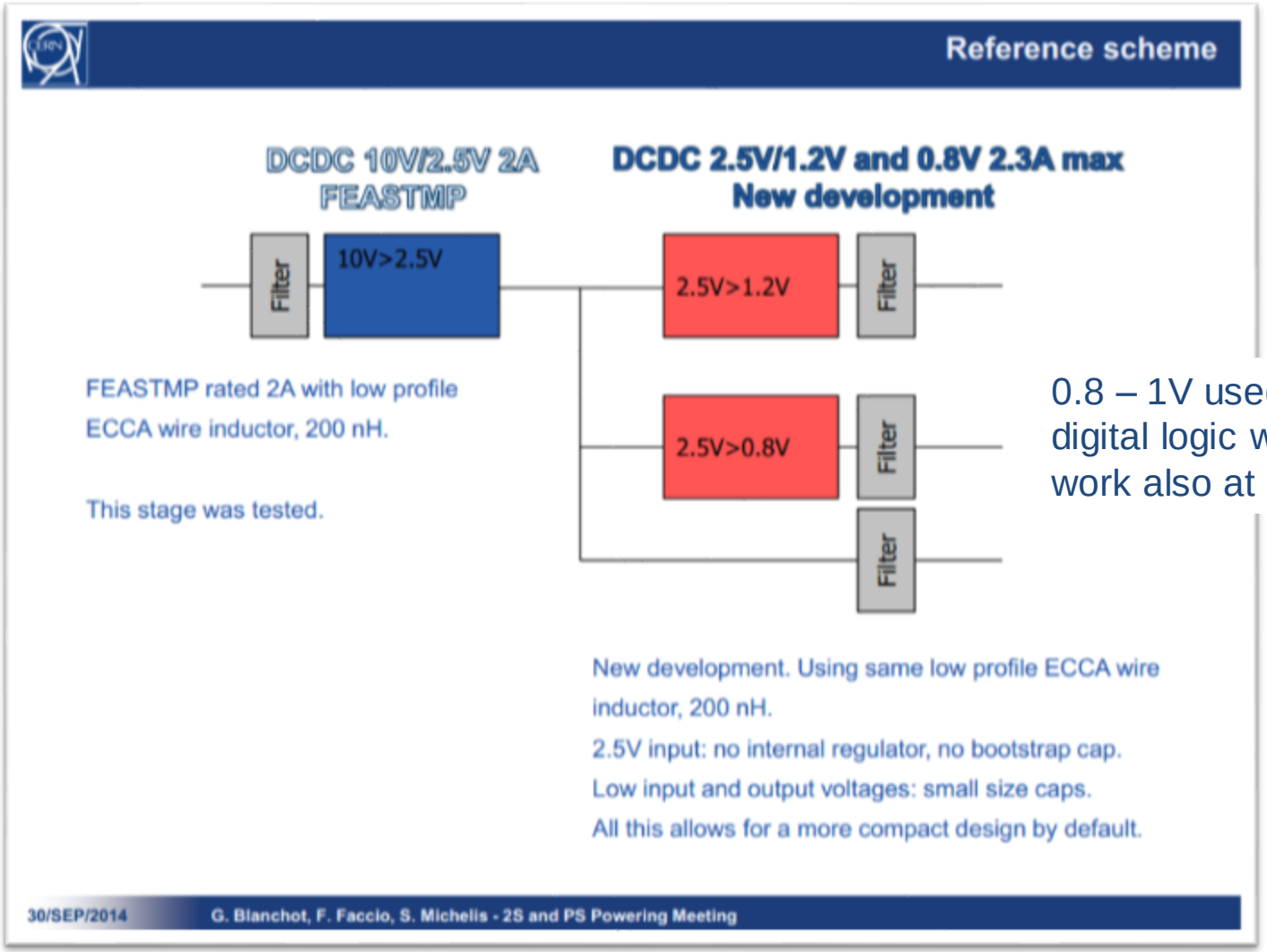


PS module	CO2 temperature @ working point [°C]	thermal runaway [°C]
1.6 mm	-24.7	-10.8
2.6 mm	-25.6	-17.5
4.0 mm	-25.1	-14.5

Working temperature cooling: ~ -30C

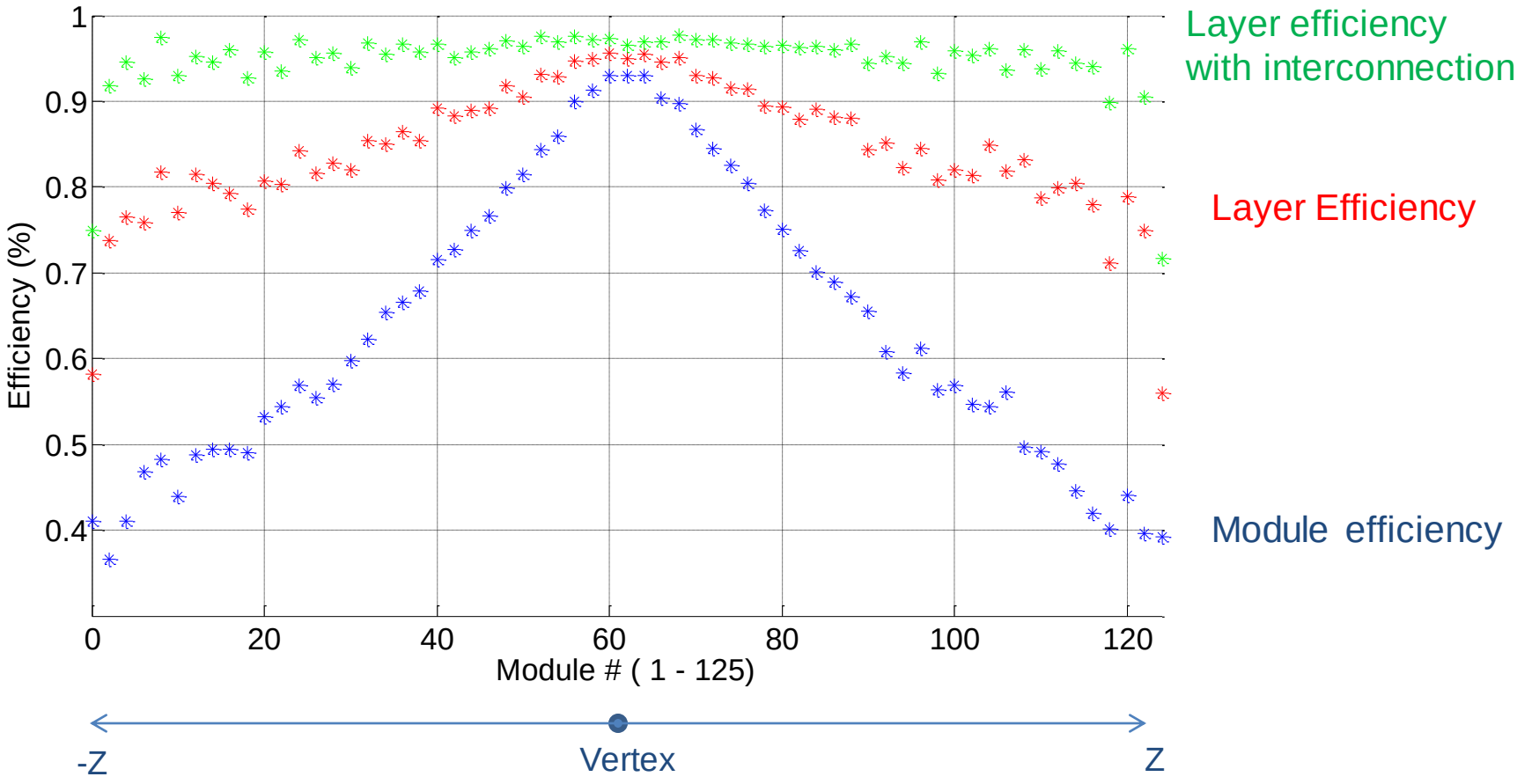
Powering reference scheme

slide and studies from G. Blanchot, F. Faccio and S.Michelis



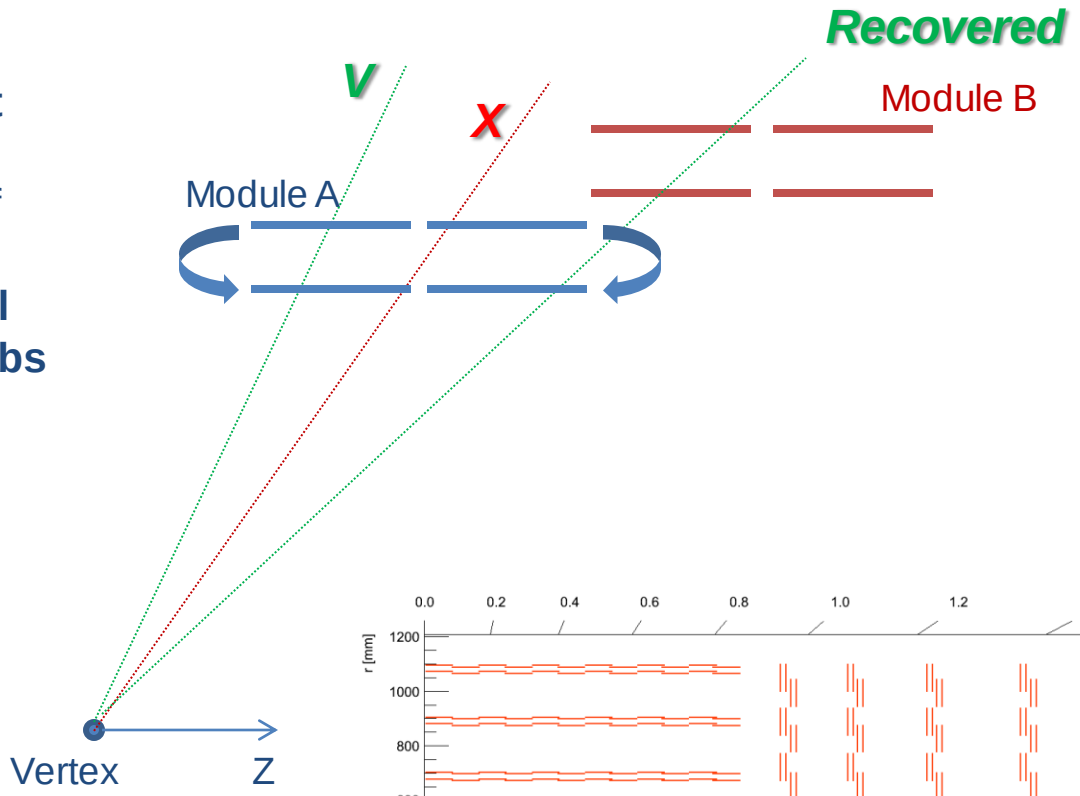
0.8 – 1V used to power digital logic which can work also at low voltage

Stub Finding logic efficiency results



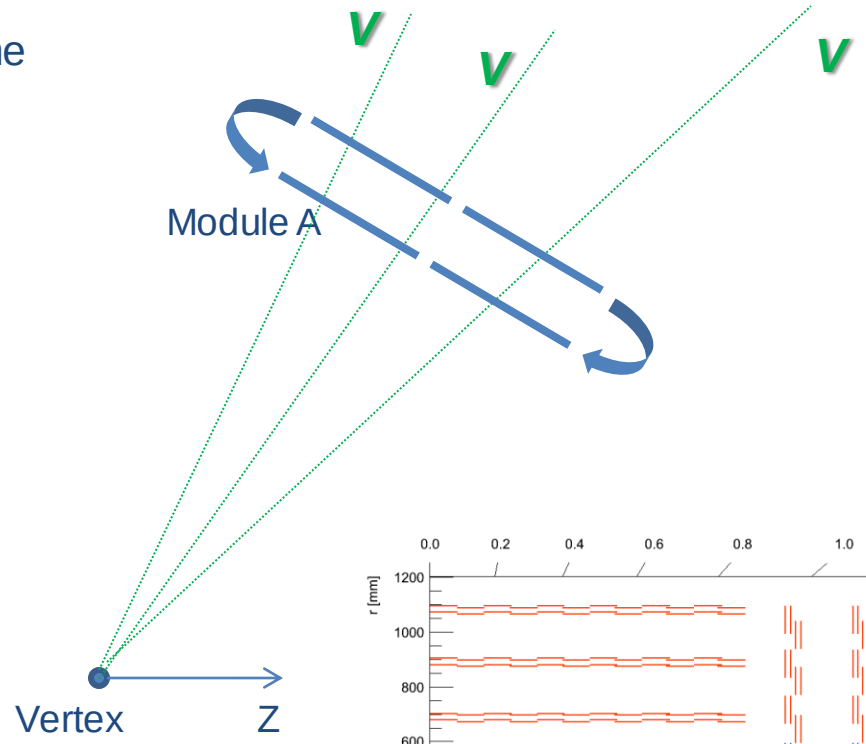
Stub Finding logic efficiency results

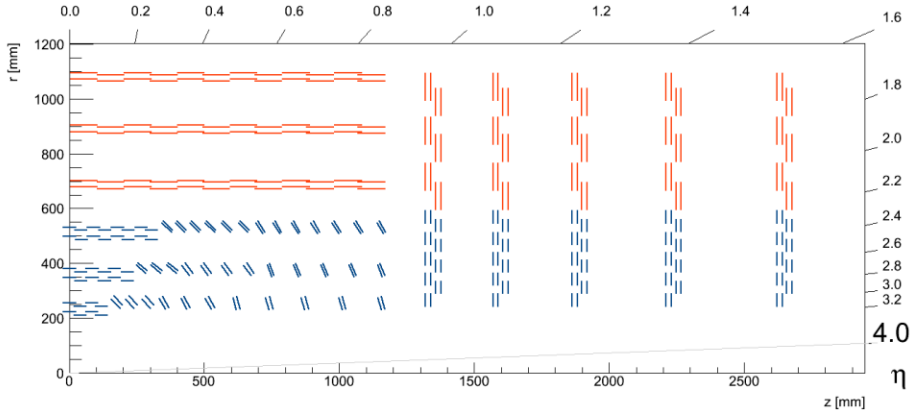
Without an **interconnect technology** (ex: TSV) between the two sides of the module, **tracks crossing the middle will not be identified as stubs**



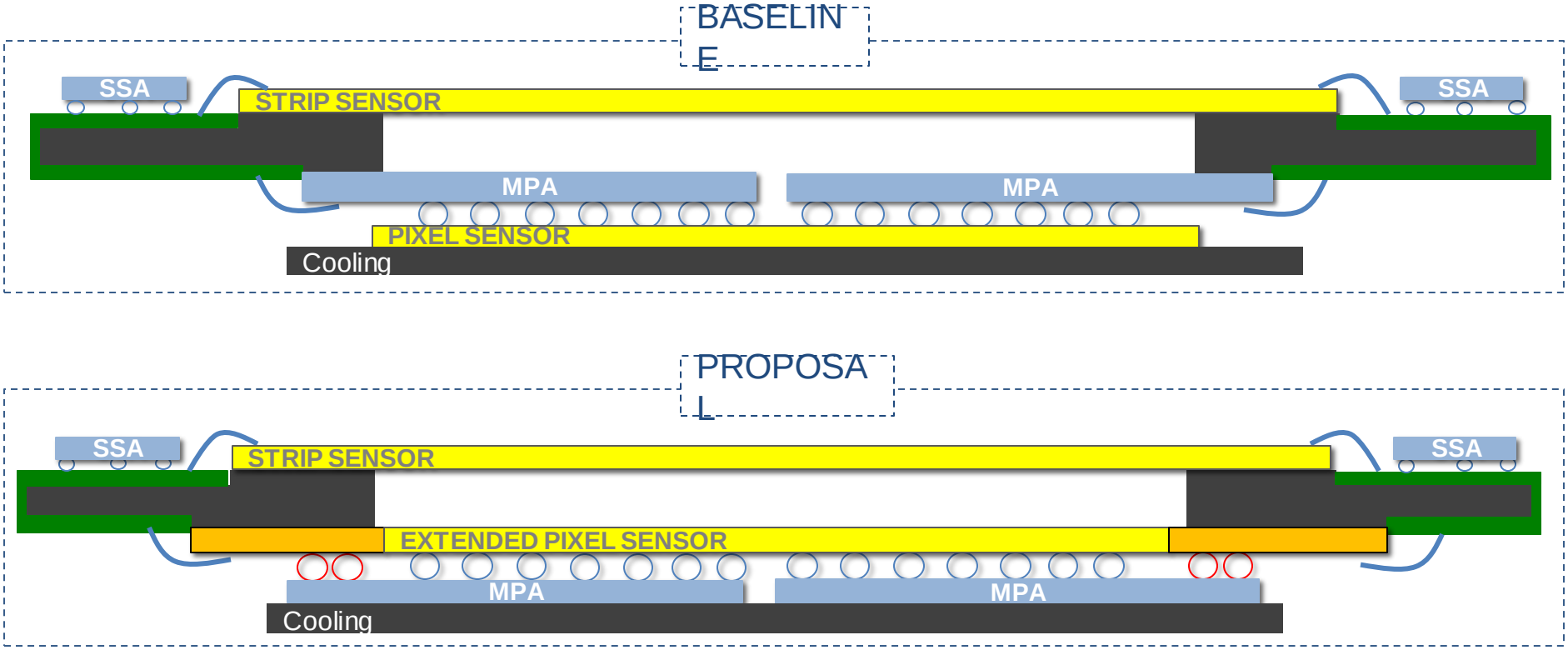
Stub Finding logic efficiency results

Tilted layout solves the problem and decrease the number of modules, but complicates mechanics





Flipped MaPSA concept



- Only bump bonding in MPA design
- No extra material between sensors
- Better cooling of MPA

- Digital IO through sensor periphery
- Temperature gradient across the sensor surface
- Larger sensor can create problem in final production

MPA-Light test system overview

developed by A. Caratelli

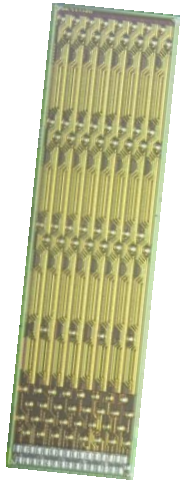
Test system controlled by Python routines

Communicates with IP bus

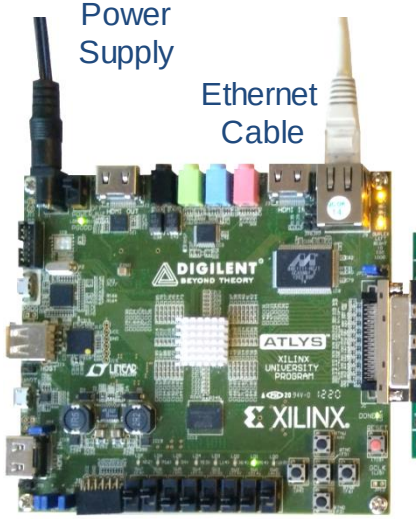
Power Supply

Ethernet Cable

MPA-Light



FPGA
Handle configuration, readout and control the interface board

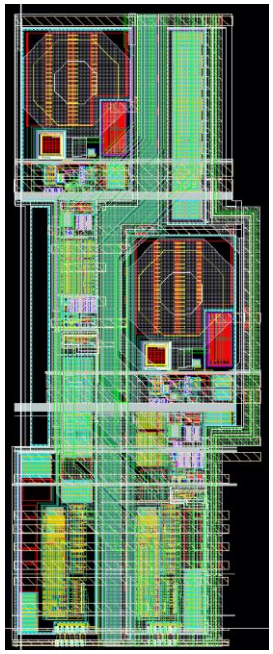


Interface Board
Voltage and Current generator and monitors
designed for the CLICpix readout by Szymon Kulis

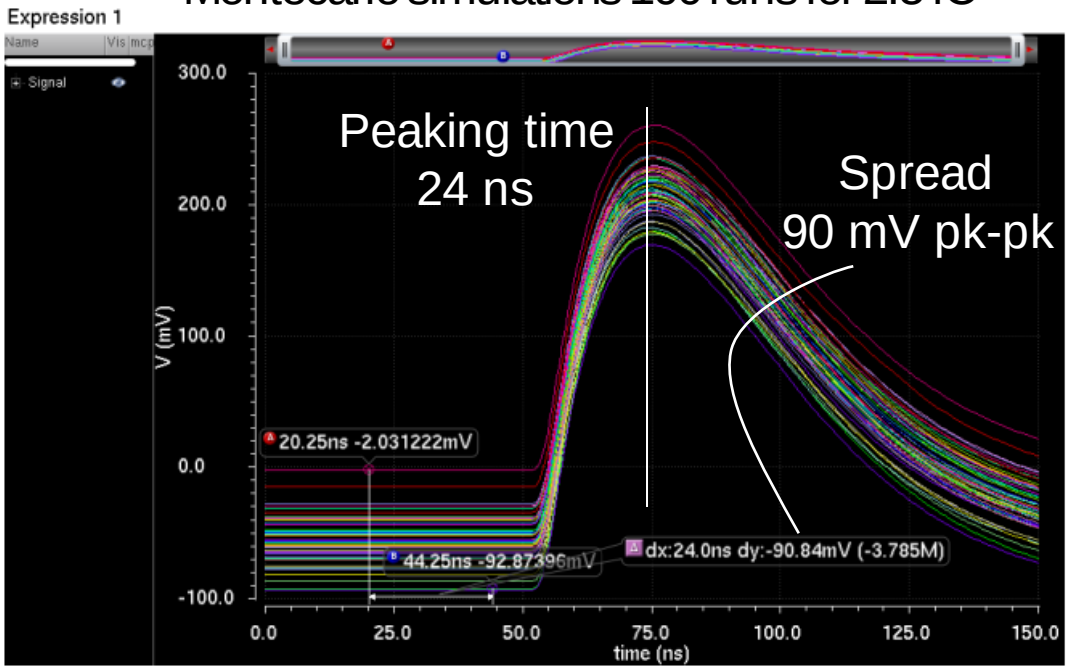
Load board
Exchangeable board for the ASIC wire bonding and decoupling

Analog Front-End simulation results

designed by J. Kaplon



Montecarlo simulations 100 runs for 2.5 fC



Other simulation results:

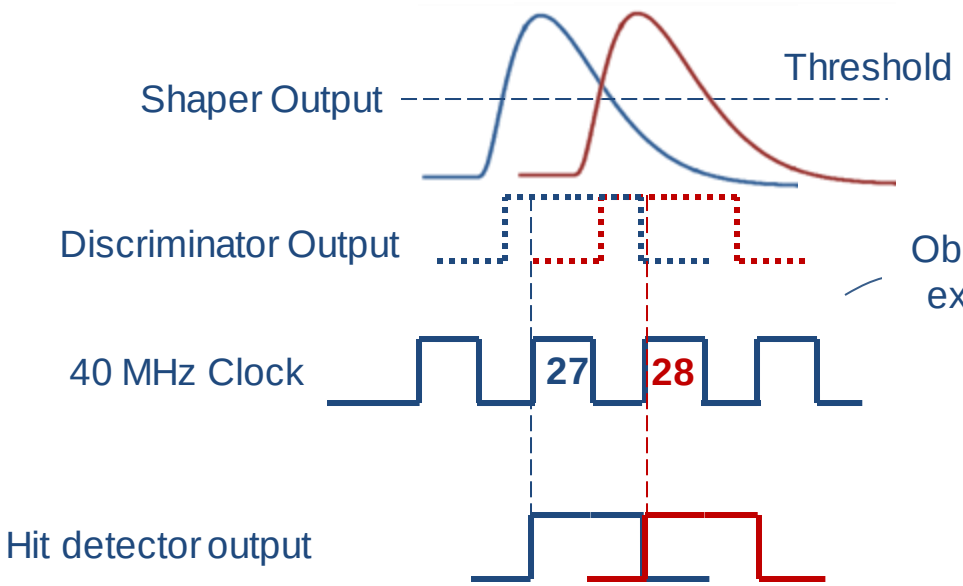
Gain from S curves: 85 mV/fC

Time walk : < 14 ns with threshold at 0.5 fC and signal from 0.75 to 12 fC

Noise(Worst case): < 200 e- (SNR >> 20)

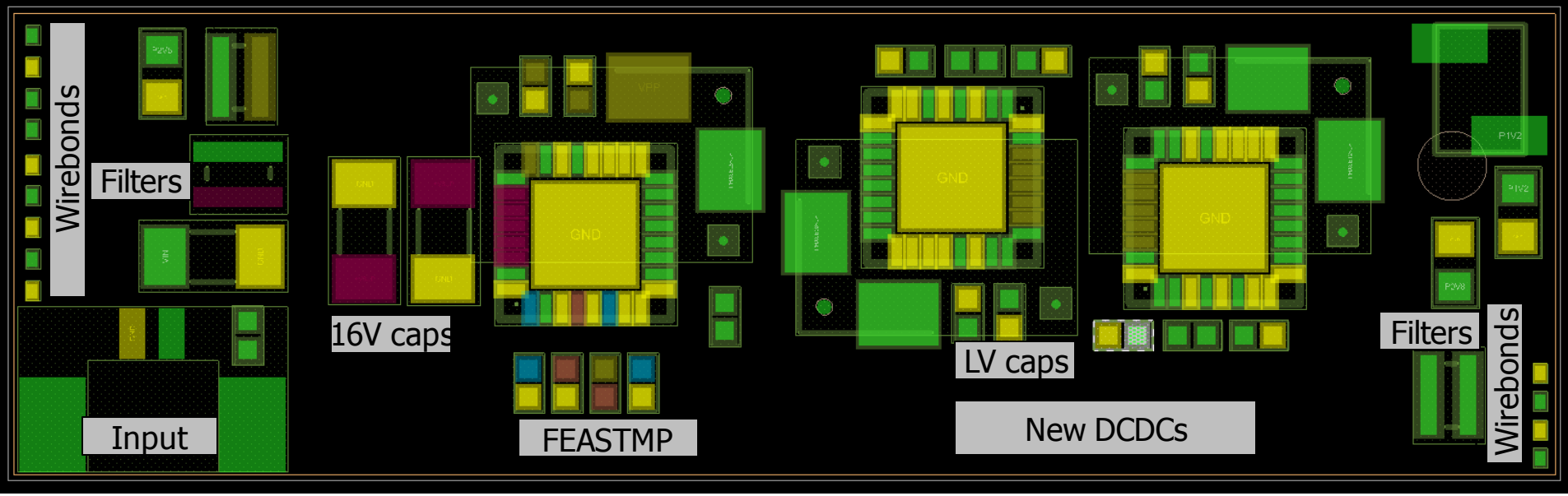
Binary readout allows FE studies

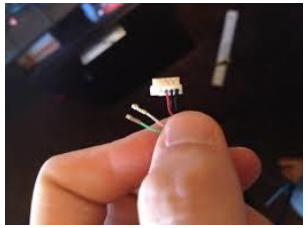
Changing the calibration injection point and using the synchronous readout we can characterize the shaper of the analog FE



Observing when the time stamp change we can extract the rising time of the shaper from zero to the set threshold

Service Board with Staged DCDC scheme





Input power: low profile Molex Picoblade 2 poles connector (stands our current rating).

The filters will stay out of the shield area, must be on sides.

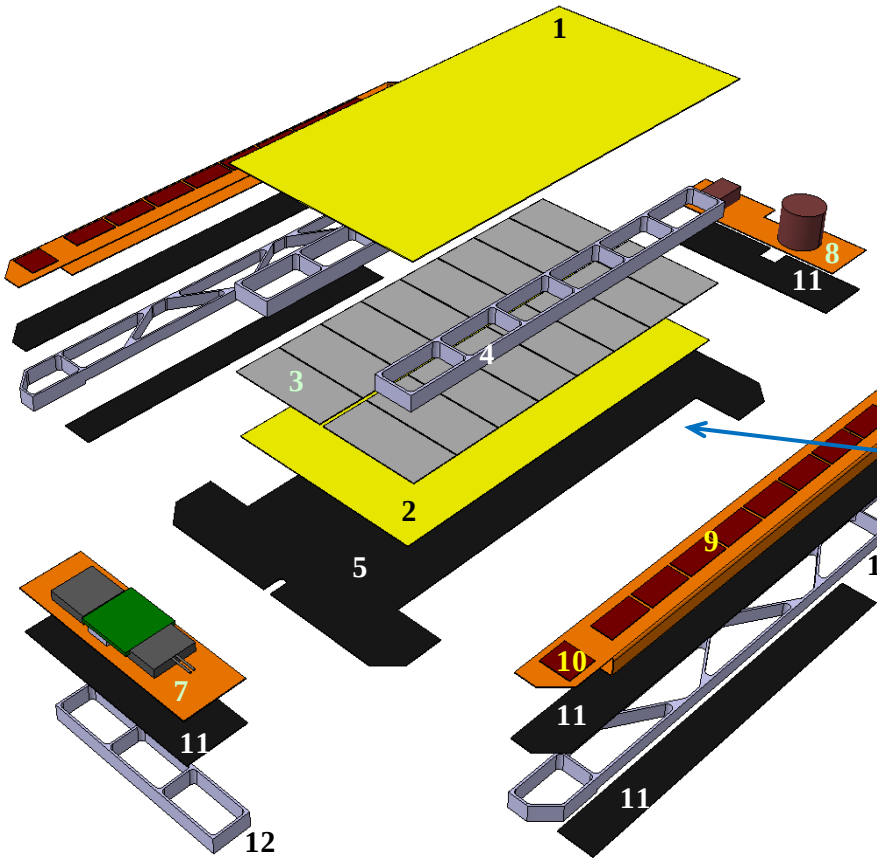
Wirebond based IO implemented so far.

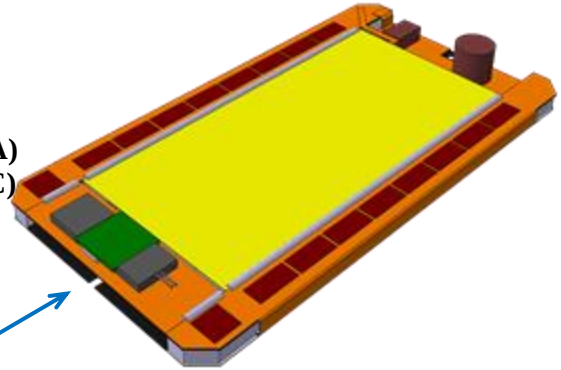
The same low mass ECCA based coil is used for the 3 converters.

The new LV DCDCs still based on teh FEASTMP geometry. However we can consider a smaller package for this chip.

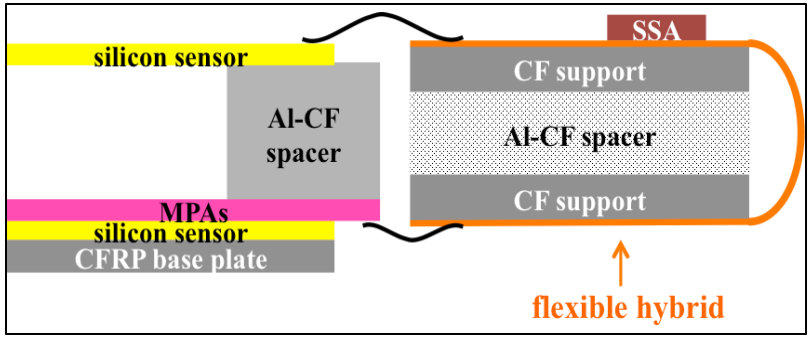
The 3 DCDC stages can be fitted in the available board space without excessive compromise.

1. Silicon strip sensor
2. Silicon pixel sensor
3. Macro-Pixel ASIC (MPA)
4. Al-CF sensor spacer
5. CFRP base plate
6. FE Hybrid
7. Opto-Link Hybrid
8. Power Hybrid
9. Short-strip ASIC (SSA)
10. Concentrator IC (CIC)
11. Hybrid CF support
12. Al-CF Hybrid spacer



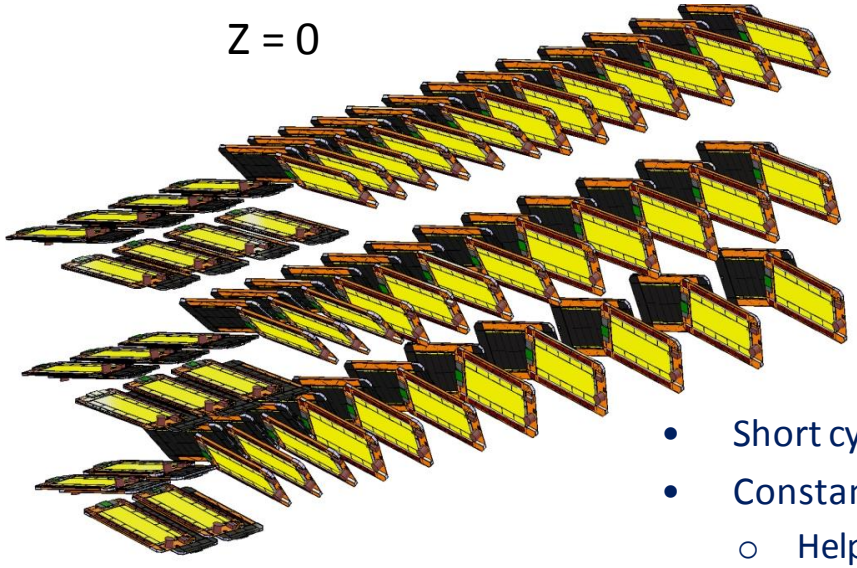


Support and cooling via a large-area base plate



More realistic tilted geometry

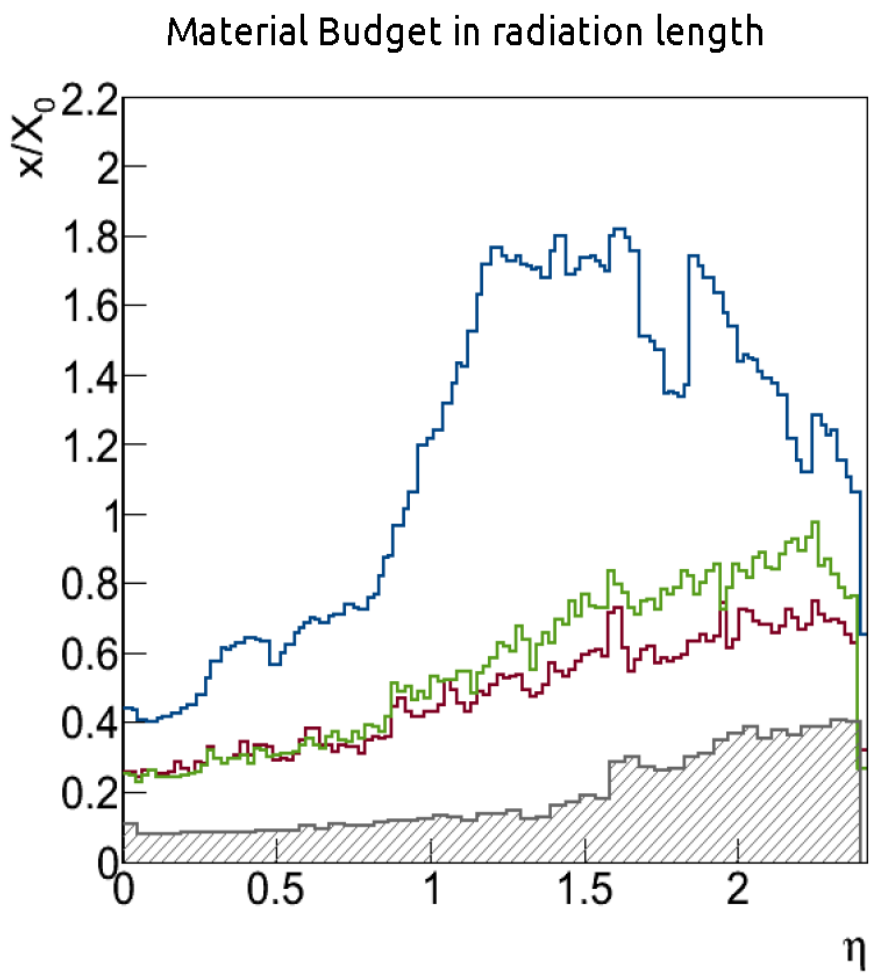
Z = 0



- Short cylindrical section in the center
- Constant tilt angle in several successive rings
  - Helps avoiding clashes
  - Also, reduces support structure variants.

Material budget full tracker

S. Mersi at al., Performance of Tilted Inner Barrel, CMS Upgrade Workshop 1 April 2014



CMS Phase-1

CMS Phase-2 Flat
estimate, if keeping ~ phase-1 pixels material

CMS Phase-2 Tilted
estimate, if keeping ~ phase-1 pixels material

Phase-1 Pixel