Contribution ID: **57** Type: **Oral**

Design and results of a 65 nm digital readout Macro Pixel ASIC (MPA) prototype with on-chip particle recognition for the Phase II CMS Outer Tracker upgrade

Wednesday 30 September 2015 14:50 (25 minutes)

The High Luminosity LHC (HL-LHC) requires major upgrade to the CMS experiment. In particular, the Phase II CMS Tracker upgrade needs a completely new readout ASIC called Macro Pixel ASIC (MPA) for its Pixel-Strip modules. It will extract and digitise analogue signals from pixelated sensor and perform digital processing at 40 MHz frequency. The digital processing includes particle recognition based on transverse momentum discrimination, global event storage and position encoding. The first prototype of the ASIC was designed, fabricated and tested. The successful results obtained will be presented and will drive the final development of the project.

Summary

The higher luminosity for the Phase-II upgrade of LHC entails new challenges in the design of the CMS silicon outer tracker. In the inner part of the outer tracker, the higher granularity needed to keep the occupancy level at a few percent and the requirement of having a good estimation of the z-coordinate of the hit gives rise to the need of pixelated sensors. Furthermore, to keep the Level 1 (L1) trigger rate at an acceptable level (500 kHz - 1MHz) requires the capability to perform quick recognition of particles with high transverse momentum (pT). Particle recognition is based on the concept that a low momentum track bends more in the 3.8 T magnetic field of CMS than a high momentum one. In order to measure the track bending, each module is composed by two closely spaced sensor layers. One layer is a pixelated sensor to ensure the high granularity, while the other one is a strip sensor to limit the power consumed by the readout ASICs and to reduce the number of electrical lines on the hybrid. This module is called Pixel-Strip (PS) Module. The readout electronics of the PS modules must combine high speed and low power dissipation and is based on the Macro Pixel ASIC (MPA). It is a hybrid pixel detector readout chip with a pixel array of 1920 pixels of 100 μm x 1496 μm. The synchronous and binary pixel output is processed on-chip to find L1 track trigger primitives and to encode the positions of the tracks. Rad-hard memories store the track positions which are sent out only upon receipt of a L1 trigger, while the readout of the primitives is data-driven. A prototype of the MPA, called MPA-Light, was designed and fabricated in a low power CMOS 65 nm technology. The MPA-Light includes the same pixel size and the same analog front-end as the final version, but a smaller pixel array. It integrates bump-bond pads for sensor connections and wire-bond pads for module connection. A pulse counting mode is available for calibration and testing purposes. The binary readout architecture generates 1-bit information with a with a time stamp of 25ns in response to a pulse from the analog front-end. The entire pixel array binary readout output can be saved in a memory or can be used for the on-chip particle recognition logic. The latter performs hit cluster reduction, position encoding and high momentum particle recognition. The data processing is simultaneous with the data acquisition and the result of each processing step can be saved in the memory. Electrical characterization has been done using a custom PCB connected to an FPGA for automated testing. Test results will be presented.

Primary author: CERESA, Davide (CERN)

Co-authors: CARATELLI, Alessandro (Ecole Polytechnique Federale de Lausanne (CH)); MARCHIORO, Alessandro (CERN); KAPLON, Jan (CERN); KLOUKINAS, Kostas (CERN); DE OLIVEIRA FRANCISCO, Rui (CERN)

Presenter: CERESA, Davide (CERN)

Session Classification: ASICs

Track Classification: ASICs