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Front-End electronics for the FAZIA project

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FAZIA is a multidetector specifically designed to optimize ion identification in heavy-ion experiments. This multidetector is modular and it is based on three-layer telescopes made of two silicon detectors followed by a thick (10 cm) CsI scintillator associated to a photodiode. Its electronic is fully digital. The objective to push at maximum the ion identification capability while preserving excellent energy resolution, will be reached also using pulse shape analysis techniques and making an intensive use of high-speed flash ADCs. This paper presents the front-end part of this electronics.

Summary

FAZIA is a multi-detector for detection and identification of products issued from heavy-ion reactions below 100 Mev/nucleon. The array will cover selected parts of the solid angle with hundred telescopes. Each telescope is composed of 3 individual detectors (Si1 + Si2 + CsI). The goal to push at maximum the ion identification capability while preserving excellent energy resolution, will be reached using pulse shape analysis techniques and making an intensive use of high-speed flash ADCs with rates up to 250 Ms/s and 14 bits resolution. The large number of electronic channels led to a new concept where the whole instrumentation is integrated in the vicinity of the multi-detector and embedded inside the vacuum chamber. The conceptual FAZIA block is a set of 16 telescopes with its front-end electronic and cooling system. The electronics of a block is constituted of 8 front-end cards, two power-supply cards, one card which manages and gets the data coming from the front-end cards. The block located in the vacuum chamber, communicates with the outside world via an optical fiber. The block is powered with a 48V power supply from which all the needed bias voltages (with regulation) are generated. The FAZIA experiment gathers several Nuclear Physics institutes from a few countries (Italy, France, Poland, etc..). About the block development, INFN Naples and Bologna have developed all the mechanical mainframe, its power supply card and its block card. IPN Orsay has developed the Front-End card. INFN Florence has developed the detectors, their kaptons and their mechanical structure. The dimensions of the Front-End card are 299 mm x 88 mm. It is a 16-layer card. All components are located on the top surface. The power consumption is about 28W. This card is subdivided into three parts. The first one concerns the power-supply part which gathers three low-voltage switching regulators and four high-voltage devices for silicon detectors (up to 350V). The second part concerns two FPGA whose functions are data waveform recording from 6 high speed analog-to-digital converters, high resolution energy calculation through digital filtering, local trigger generation, data packing and transmission of acquired data at 400 Mbits/s to the acquisition system. A L-group of six ADC around each FPGA. Three of them are clocked at 250 MHz, the three others at 100 MHz. a PIC microcontroller (μC) for slow-control, high voltage and pulse generator managing and temperature reading. The third and last part concerns the analog electronics. It gathers he six preamplifiers serving the three detectors of two telescopes, the analog amplification and derivative channels to obtain a current signal from the charge one and a pulse generator for calibration.

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