GBT Link Testing and Performance Measurement on PCIe40 and AMC40 Custom Design FPGA Boards

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TWEPP 2015
Topical Workshop on Electronics for Particle Physics
28 September - 02 October 2015
IST - Lisbon - Portugal

Abstract

The high-energy physics experiments at the CERN's Large Hadron Collider (LHC) are preparing for Run3, which is foreseen to start in the year 2021. Data from the high radiation environment of the detector front-end electronics are transported to the data processing units, located in low radiation zones through GBT (Gigabit transceiver) links. The present work discusses the GBT link performance study carried out on custom FPGA boards, clock calibration logic and its implementation in new Arria 10 FPGA.

Introduction

GBT Interface links are error resilient data communication protocol for high energy physics experiment. Each link provides users with two options: standard and latency optimized mode of operation. The GBT functionality can be realized using Commercial Off-The-Shelf (COTS) components for electronics located in non-radiation zone. This work describes the efficient physical implementation, performance and stability study of the GBT [1-2] protocol on two custom readout boards namely AMC40 and PCIe40. AMC40 board uses Altera Stratix V FPGA, while PCIe40 board uses Altera Arria 10 FPGA.

Design Implementation

GBT coding sub-layer is independent of FPGA architecture chosen. However, MGT (Multi-Gigabit Transceiver) is FPGA dependant.

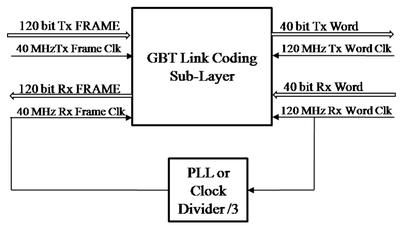


Figure 1: Basic signal block for GBT Coding Sub-layer

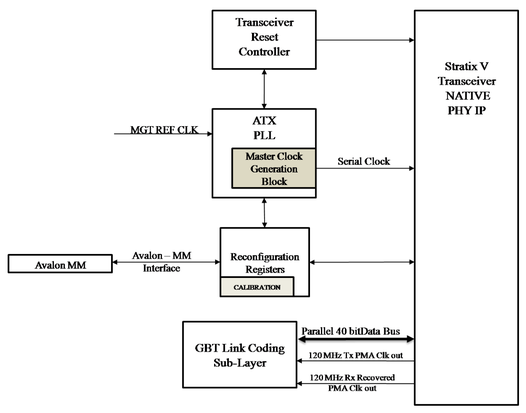


Figure 2: Stratix V Transceiver Design Connectivity

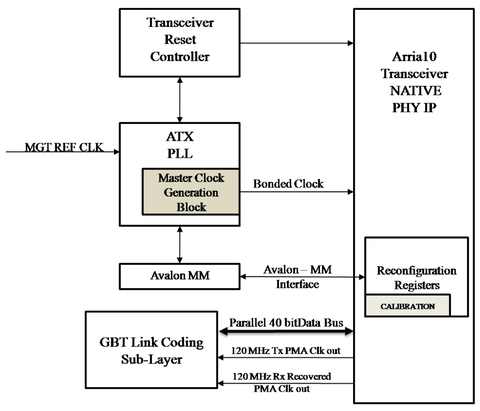


Figure 3: Arria 10 Transceiver Design Connectivity

Both the designs use **PMA** (Physical Media Attachment) **bonded mode** configuration. In this mode a single CGB (Clock Generation Buffer) divides the output it receives from Transceiver PLL to create the parallel clock inputs for all Tx/Rx channel PMA modules. This mode helps in reducing the number of independent clock domains. Accordingly in Stratix V and Arria 10, GBT PMA links are grouped into 3 and 6 links respectively to form a single **GBT Bank**.

Resource Estimation

For resource estimation a standard reference design from CERN GBT team is used having same configurations on both boards. The reference design altogether contains 4 links operating in two different modes as shown in table 1.

Table 1: Reference Design configuration

Configuration Parameter	Value
No of GBT Bank	2
Bank 1	*No of Links* = 1 *Tx Mode* = *STANDARD* *Rx Mode* = *LATENCY OPTIMIZED*
Bank 2	*No of Links* = 3 *Tx Mode* = *LATENCY OPTIMIZED* *Rx Mode* = *STANDARD*

Table 2: Shows the comparison of resource utilization in two boards for Standard Reference Design

Parameters	**AMC40**		**PCIe40**	
FPGA Family *Device Part Number*	**Stratix V** **5SGXEA7N2F45C3**		**Arria 10** **10AX115S4F45I3SGE2**	
	Occupancy Ratio	Percentage of Occupancy	Occupancy Ratio	Percentage of Occupancy
Logic utilization (in ALMs)	10,542 / 234,720	4%	9,055 / 427,200	2 %
Total registers	20060		18338	
Total block memory bits	202,752 / 52,428,800	< 1 %	126,464 / 55,562,240	< 1 %
Total RAM Blocks	56 / 2,560	2 %	40 / 2,713	1 %
Total HSSI PMA RX Serializers/Deserializers	4 / 48	8 %	4 / 72	6 %
Total PLLs	11 / 92	12 %	10 / 176	6 %

Latency Measurement

GBT will be used for sending trigger, timing and busy line distribution. As these are latency critical data path, the total latency is measured between user transmitted parallel data frame and received data frame, after optical loopback. The path includes GBT encoding/decoding, Serializer/Deserializer and Electrical/Optical conversion. The pathway for latency measurement: `Tx Data Frame - GBT Tx - MGT Tx (Serialization) - Optical Loopback - MGT Rx (De-serialization) - GBT Rx - Rx Data Frame`

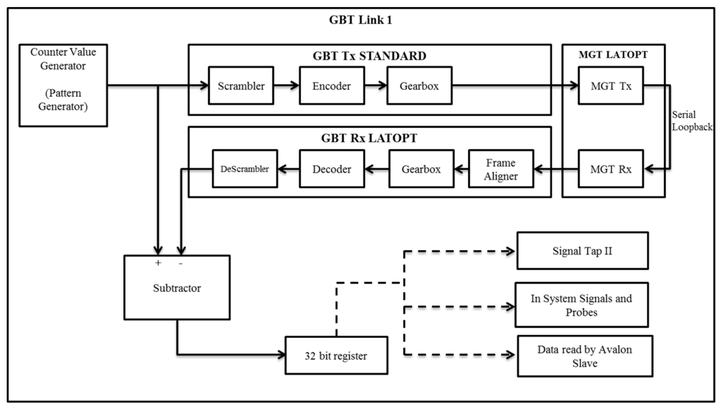


Figure 4: Latency Measurement Test Setup.

Table 3: GBT Latency Measurement

	Different Mode of operations			
Tx Side →	Standard	Standard	Latency Optimized	Latency Optimized
Rx Side →	Standard	Latency Optimized	Standard	Latency Optimized
AMC40	600 ns	350 ns	350 ns	150 ns
PCIe40	450 ns	350 ns	200 ns	150 ns

Bit Error Rate (BER) Analysis

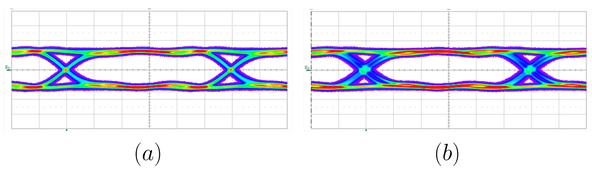
In our test setup we have made PCIe40 board to AMC40 board connection. The Altera Transceiver Toolkit (TTK) full functionality is not available for Arria 10 ES1. Thus, results for PCIe40 are preliminary.

Table 4: BER Measurement

Parameters	AMC40	PCIe40
Test Setup	AMC40 (Tx) - optical cable - AMC40 (Rx)	PCIe40 (Tx) - optical cable - AMC40 (Rx)
Tx configuration Parameter		
V_{OD} control	50	29
Pre – emphasis 1st post – tap	0	0
Pre – emphasis pre – tap	0	0
Pre – emphasis 2nd post – tap	0	0
Rx configuration Parameter		
DC Gain	1	1
Equalization Control factor	0	0
DFEEnabled	off	off
PLL reference Clock Frequency	120 MHz	120 MHz
Test Pattern	PRBS31	PRBS31
Results of TTK		
BER (Bit Error Rate)	1.115E-12	5.0723E-10 #
EyeWidth/EyeHeight	26/127	23/89

The results will be further investigated

Jitter and Eye Measurement



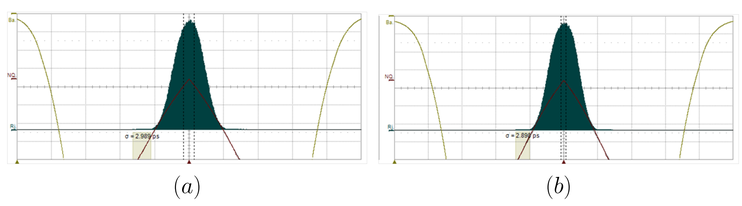
(a) (b)

Figure 5: Showing the Eye Diagram for Tx Optical using GBT encoded data (a) AMC40 and (b) PCIe40

Table 5: Shows the comparison of Minopod performance in two boards

	AMC40	PCIe40
Eye Height	378 mV	373 mV
Eye Width	190.4 ps	176.8 ps

	AMC40	PCIe40
Deterministic Jitter (Dj)	5.503 ps	13.125 ps
Periodic Jitter (Pj)	6.75 ps	7.24 ps
Data Dependant Jitter (DDj)	11.228 ps	21.647 ps
Inter Symbol Interference (ISI)	11.095 ps	21.657 ps
Duty Cycle Jitter (DCD)	2.000 ps	1.912 ps
Random Jitter(Rj)	3.245 ps	3.204 ps
Total Jitter (Tj)	51.148 ps	58.185 ps
Standard Deviation(σ)	2.989 ps	2.898 ps

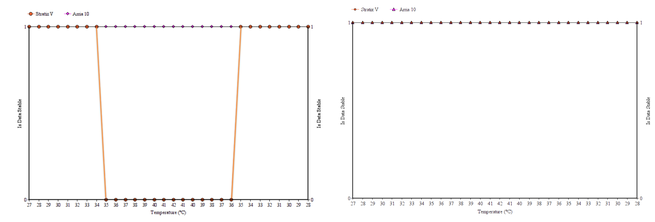


(a) (b)

Figure 6: Showing the Jitter Spectrum for (a) AMC40 and (b) PCIe40

Link Stability with Temperature Variation

With temperature variation phase drift happens. This is detrimental for latency optimised transmission mode as shown in fig. 7. For mitigating this issue a section on clock calibration is discussed. Temperature Sensing Diode (TSD) internal to FPGA is used for on chip temperature monitoring.



(a) (b)

Figure 7: Showing the data stability vs temperature variation of both the custom boards when GBT operating in (a)Tx Latency Optimized mode (b) All other modes

Clock Calibration

Stratix V FPGA

The calibration is needed when a GBT Tx Link is operating in latency optimized mode. We have found that in AMC40 (Stratix V FPGA) Tx Word Clk exhibits non-deterministic phase shifts with respect to Tx Frame Clk. We have investigated and compared three possible solutions for this problem.

I. *NON-DETERMINISTIC SOLUTION*

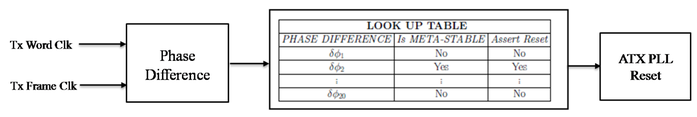
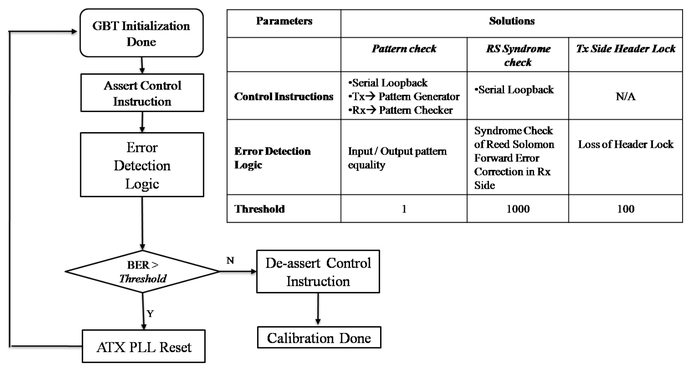


Figure 8: Clock Calibration based on manually tabulated phase error look-up table

II. *DETERMINISTIC SOLUTION*



Parameters	Solutions		
	Pattern check	***RS Syndrome check***	***Tx Side Header Lock***
Control Instructions	•Serial Loopback •Tx→ Pattern Generator •Rx→ Pattern Checker	•Serial Loopback	N/A
Error Detection Logic	Input / Output pattern equality	Syndrome Check of Reed Solomon Forward Error Correction in Rx Side	Loss of Header Lock
Threshold	1	1000	100

Figure 9: Clock Calibration based on data frame error detection

III. *MODIFIED Tx GEARBOX*

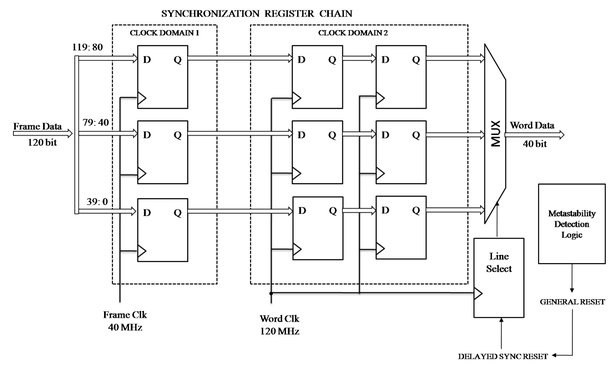


Figure 10: Synchronization Register Based Clock Domain Crossing with Metastability Detection

Arria 10 FPGA

Fortunately, the Arria 10 FPGA automatically calibrates the PLL and PHY at every power-up before entering user-mode. But if there is loss of MGT reference clock or it was not ready during start up, User-Coded Reset Calibration is required.

Conclusions

1. With this comparative analysis, we have proven that the GBT protocol can indeed be implemented with success in both the 28nm Stratix-V and 20 nm Arria-10 Altera FPGAs.
2. The source code of developed firmwares are archived in CERN espace, and more resources are available to users on requests.

Reference

1. Barros Marin, M., et al. "The GBT-FPGA core: features and challenges." Journal of Instrumentation (2015)
2. S. Baron, et al."Implementing the GBT data transmission protocol in FPGAs " Topical Workshop on Electronics for Particle Physics. 2009
3. GBT-FPGA project `https://espace.cern.ch/GBT-Project/GBT-FPGA`