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GBT Link testing and performance measurement on PCIe40 and AMC40 custom design FPGA boards

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The high-energy physics experiments at the CERN's Large Hadron Collider (LHC) are preparing for Run3, which is foreseen to start in the year 2020. Data from the high radiation environment of the detector front-end electronics are transported to the data processing units, located in low radiation zones through GBT (Gigabit transceiver)1 links. The present work discusses the GBT link performance study carried out on custom FPGA boards.

Summary

Most of the experiments at the LHC are going for a major readout architecture modification in preparation for the high luminosity RUN3, expected to start in 2020. As an example, the upgrade architecture in ALICE involves the design of new data concentrator multiplexing and trigger distribution unit called the Common Readout Unit (CRU), located in the counting room. The requirement is to transfer data with very high reliability from the detectors situated in the high radiation environment to the counting room in the non-radiation zone and transferring trigger signals while maintaining a constant latency. GBT Interface links are chosen for this interface as it provides radiation tolerant deterministic latency based data communication path with forward error correction mechanism.
The GBT link provides users with two options: standard and latency optimized mode of operation. In standard mode, the data transfer has an uncertainty of +/- one clock cycle in the transfer time. In latency optimized mode data transfer features register based clock domain crossing (CDC) for deterministic latency. Register based CDC requires calibration, to guaranty a stable behavior over a comfortable operating temperature range. New calibration logic has been developed for auto-initialization of the GBT firmware. The phase alignment between the regenerated clock and the received clock is monitored to make sure that the data is sampled at correct clock edge. Each link also supports two types of coding scheme, namely GBT Frame, and Widebus. A detailed study of the latency measurement and its temperature stability analysis is done for reliability testing of the design in time critical communication. For easy system integration of the GBT firmware, an Altera QSYS framework wrapper is designed. A stable jitter free clock source is required for proper functioning of GBT protocol. Clock jitter measurement is done, to observe that it is lying within the jitter tolerable margin. A Bit Error Rate (BER) analysis is done using a pseudo random pattern generator and checker, to measure the performance with variation in coding scheme, optical link length and temperature variation. The channel performance of the transceiver link in serial and optical loopback is studied by interpreting the eye pattern. The GBT links, if bonded together uses less clock resources. Results of these studies will be discussed.

References:
(1) Barros Marin, M., et al. "The GBT-FPGA core: features and challenges."Journal of Instrumentation 10.03 (2015): C03021.

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