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# Development of the 40 MHz readout for the upgraded LHCb VELO

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The upgraded LHCb VELO (vertex detector) will be equipped with silicon hybrid pixel detectors reading out at 40 MHz. The high data rates will be handled by high-end computing servers installed with FPGA cards. The output stage of the ASIC will be equipped with a custom developed output serialiser capable of handling the high rates while operating at low power. The firmware development will be described together with the irradiation tests of the output stage prototype.

## Summary

The upgraded LHCb VELO (vertex detector) will consist of 52 silicon pixel modules, each read out by 12 VeloPix ASICs. Due to the triggerless operation of the upgraded detector, each event must be read out without data loss and transmitted to the event filter farm, where the event rate must be reduced from the 30 MHz of colliding bunches to the storage output rate. This leads to high demands on the data rate throughput from the VELO. The total data rate per module, close to 50 Gb/s, will be processed by an FPGA installed in a high-end computing server performing several tasks at an event rate of 40 MHz.

The first task in the FPGA is the time unscrambling of the data packets which arrive with a latency which is dominated by the depth in the pixel readout column of individual hits. After unpacking the individual data packets from a custom data-transfer protocol the time ordering must be performed at the full 40 MHz speed. Following the time-ordering a spatial sorting permits the identification of isolated hits, which is used to speed up the CPU-based clustering algorithm.

The output stage of the VeloPix ASIC is critical for the high speed, low power, operation of the chip. The data rates can exceed 15 Gb/s per individual ASIC, and the power budget is limited due to the operation in vacuum of irradiated silicon modules. A new data serialiser and wireline driver circuit, the GWT, has been developed to meet these demands. It is developed in 130 nm technology and operates with a shift-register-free topology to optimise power consumption.

During this development period the HDL code is being simulated with Modelsim, and implemented on an Altera Stratix V FPGA. Expected VeloPix data signals from a full detector simulation combined with the anticipated LHC bunch filling schemes is used as input data to the FPGA simulation. Through a well-aligned design of the firmware and software algorithms, the time available for the fully software-based high-level trigger is maximised. The status of the firmware development, emulation and test

status will be described, as well as the tests of the GWT prototype for transmission speed and SEU resistance.

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