Qualification of the CMS Phase 1 Upgrade HF Front-end Electronics

Andrew Whitbeck

Fermi National Accelerator Laboratory

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Upgrade Motivation



- Forward hadron calorimeter:
 - steel absorber and quartz fiber to produce cerenkov light
 - Photo Multiplier Tubes (PMTs)
- Anomalous signals from particles incident on PMT windows or PMT housing producing large isolated signals



- 50 ns strategy was to move anomalous signals to the empty BX
 - unable to mitigate these effects in 25 ns operation

Upgrade Overview

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- New PMTs installed with thinner windows to reduce cerenkov light — installed during LS1
- PMT electronics will be replaced to convert from single to dual anode readout
 - asymmetry in redundant readings provide handle for PMT window events
- All new frontend electronics
 - to handle larger number of channel
 - pulse timing for distinguishing early anomalous signals
 - improved hardware for control system



Frontend Overview



- Next Generation Clock & Control Module (ngCCM) distributes clock, fast synchronization signals & slow control signals
- QIE cards contain digitizing ASICs, serializing/formatting FPGAs & optical transmitters
- Calibration module distributes LED light into photodetectors for monitoring





QIE card





QIE card components

- Fermilab
- FEAST-MP DC-DC converters for voltage regulation
- Versatile link transmitters high speed, rad. hard



- Microsemi Bridge
- Microsemi IGLOO2
- QIE10 ASIC

Charge Integrator & Encoder (QIE)



- 10th generation ASIC well suited for calorimeter readout (350 nm SiGe)
- Provides deadtimeless charge integration & digitization at ~40 MHz pipelined with 4 identical integrators
- 8 bit ADC code (-3 fC to -330 pC) with ~1% resolution implemented using 4 ranges of varying sensitivity and a pseudo-logarithmic ADC



• 6 bit TDC code (500 ps resolution) for measuring arrival time of pulses

Single chip testing

- ~4000 QIE chips needed for HF production
- Chips tested with automatic robot and custom board with clam shell mount ~3k chips tested per week
 - chips automatically sorted based on test results
- functionality testing yielded 85% of chips
- Testing showed low variability from manufacturing — <5% for all tests



QIE10	Efficiency	Remaining Yield
Original		10076
Hard Failures	97.2%	9790
Voltages	98.9%	9680
Register Tests	97.2%	9462
LVDS Output	95.4%	9043
Misc	97.7%	8980
Pedestal Tests	96.8%	8800
ADC Functionality	91.6%	8180
TDC Functionality	98.6%	8173
TOTAL	81.1%	8173



IGLOO2 FPGA

- Provides clocks to 12 QIEs with programmable phase adjustment
- Captures data from 12 QIEs (received from 8 DDR outputs for each QIE)

BER of serialized data < 1e-12

- Uses TDC discriminator from QIE to computes 4-bit trailing-edge TDC
- Formats & serializes data with native 5 Gbps SERDES (8b10b encoding)



BER for serialized data at input to VTTx modules



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ref. versus phase adjusted QIE clock

Optical data links

- CERN developed VTTx transmitters used for data link to backend
 - links are operated at 5.0 Gbps asynchronously from the LHC clock eliminates need for a high performance jitter cleaning circuit
 - data comes at 4.8 Gbps pad words inserted to fill data stream
- Large optical power margin between VTTx & PPOD



Communication

- Microsemi Bridge used monitoring & configuring QIE card
- Receives I²C commands from ngCCM over backplane
- Multiplexes I²C lines to various devices (VTTxs, IGLOO2s, UniqueID chip, temperature sensors)



Clock & control module



FEAST-MP DC-DC Versatile Link transceiver Microsemi IGLOO2



Clock & control module



- Receives clock and control data from next-generation Front End Controller (ngFEC), implemented with FC7 and GLIB
 - uses Gigabit Transceiver (GBT) protocol implemented with an IGLOO2 & VTRx @ 4.8 Gbps
 - large bandwidth allows for constant error checking with a PRBS on the link
- Distributes LHC clock & slow control data to each frontend module
 - Individual I²C lines are used to communicate with the various slots
- Remote programming of IGLOO2 FPGAs on QIE cards
- Additional VTRX and a VTTx provide a redundant control path



System level diagram





Integration & acceptance testing

- commissioning frontend with backend electronics (µHTR & ngFEC)
 - GBT/I²C communication extensively validated with write-verify tests for each frontend register
 - data readout validation:
 - pattern tests, monitoring invalid 8b10b codes, checking for pedestal stability, and internal charge injection
- Suite of tests will be performed on a each of the 180 QIE cards to qualify them
 - check pedestals, TDC functionality, control link, and data link integrity
 - Use calibration system to take LED data for validating/ characterizing QIE response to fast analog signals
 - All channels will be calibrated with dedicated charge injection hardware for scanning through a wide range of DC currents



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pulse from QIE internal charge injection

QIE calibration



- QIE response measured with well-calibrated DC current source
- Charge injector will be controlled via a commercial external 16-bit DAC
 - dynamic range of 50 fC to -60 pC
 - random noise ~2 ADC
- Measure response with a piece-wise linear function for each cap-ID and each range separately separately
 - including prior knowledge about the structure of the flash ADC we get 32 constants per chip



Summary



- Design of new frontend electronics for CMS HF upgrade has been presented
 - new digitizing ASIC improves noise rejection
 - high speed optical transmitters provide increased bandwidth for higher channel density
 - faster optical transceivers allow for more reliable control links and facilitate faster monitoring & configuring
- Qualification testing plans are finalized & work is ongoing at CERN
- Electronics are expected to be installed at the end of this year & used in 2016 data taking

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Backup

