Front-end electronics for Micro Pattern Gas Detectors with integrated input protection against discharges

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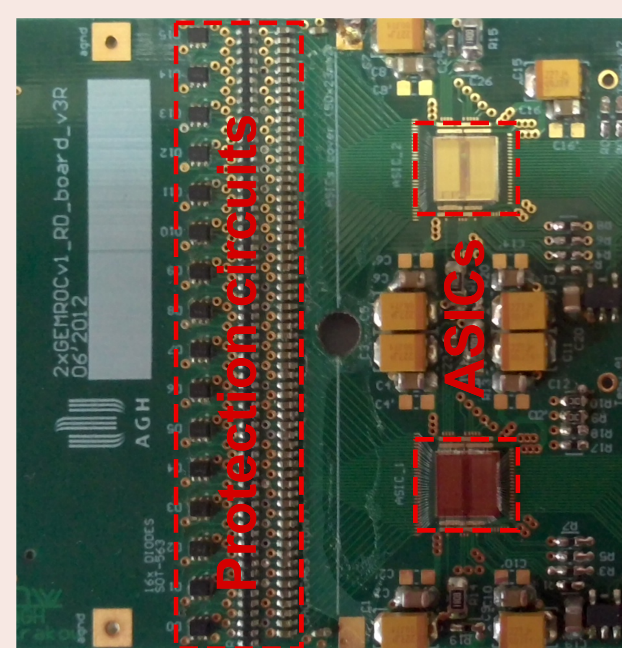
Motivation

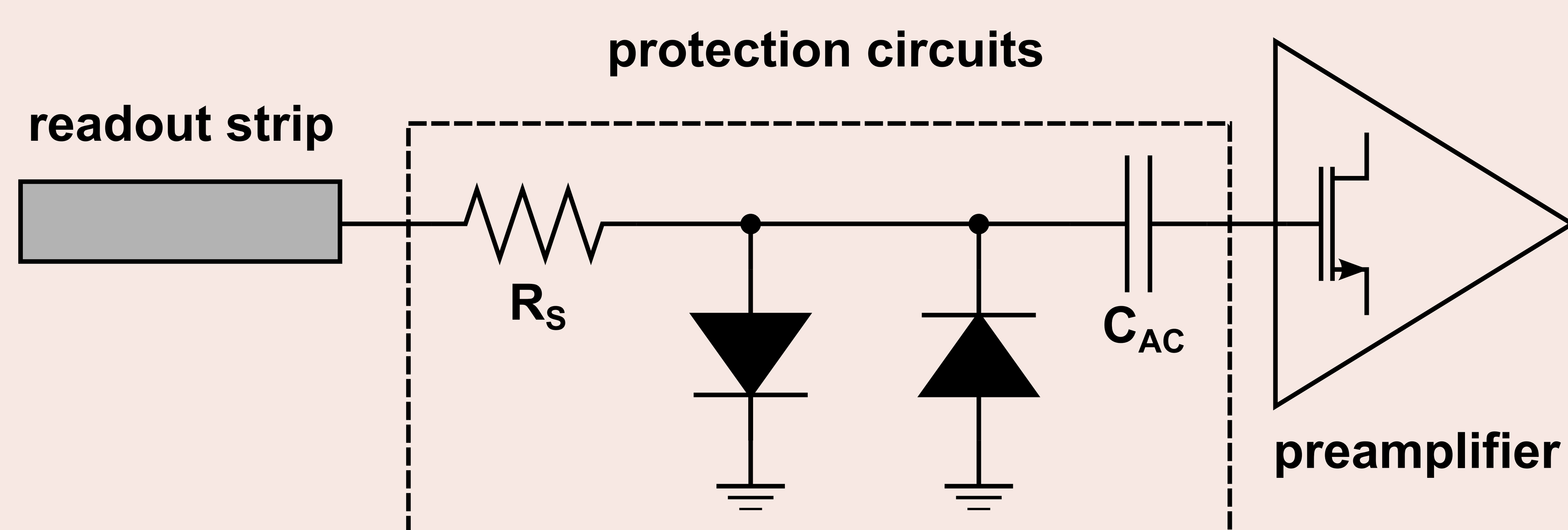
One of the major problems that have to be addressed in the design of the front-end electronics for readout of MPGDs, is its resistance to possible random discharges inside active detector volume. This issue becomes particularly critical for the electronics built as ASICs implemented in a modern CMOS technology. With continuous downscaling of the CMOS technologies the breakdown voltages of transistors are becoming lower and lower and for any CMOS device input protection is needed to prevent damages during handling and assembling of such devices. Therefore, the problem of Electro Static Discharge (ESD) is being continuously investigated in the field of CMOS integrated circuits. The vendors of the CMOS technologies deliver recommended ESD protection circuits, which are qualified according to the standards used in the electronics industry. Within these standards the voltages vary in the range from 2kV to 10kV. Although the voltages are comparable with the voltages used for biasing the MPGDs, the equivalent electrical circuit of a MPGD is different compared to the circuit used in the ESD. First of all, in case of a discharge occurring in the MPGD the resistance of the discharging path is much lower. Thus, a protection circuits against discharges in the MPGDs have to handle much higher currents and the typical circuits recommended for protection against ESD are not adequate at all.

The poster presents test results of input protection structures integrated with a specific design of the front-end electronics designed and manufactured in the 350nm CMOS process from the ams (Austriamicrosystems). The structures were tested using an electrical circuit to mimic discharges in the detectors for different voltage and current parameters of the sparks. The front-end electronics connected to the MPGD is exposed to multiple discharges so that not only determination of absolute maximum rating for the protection circuits is important but also the lifetime measured in the number of discharges.

Protection circuits build of SMD components

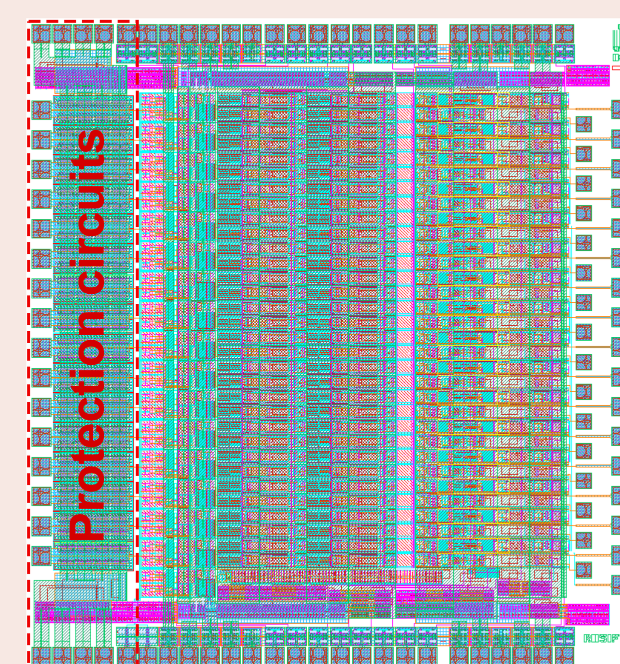
- Large area occupied by the SMD components (7 mm × 42 mm for 64 channel readout).
- Additional stray capacitance.
- Advanced and expensive PCB technology.
- Demanding assembly techniques.
- High cost of elements.

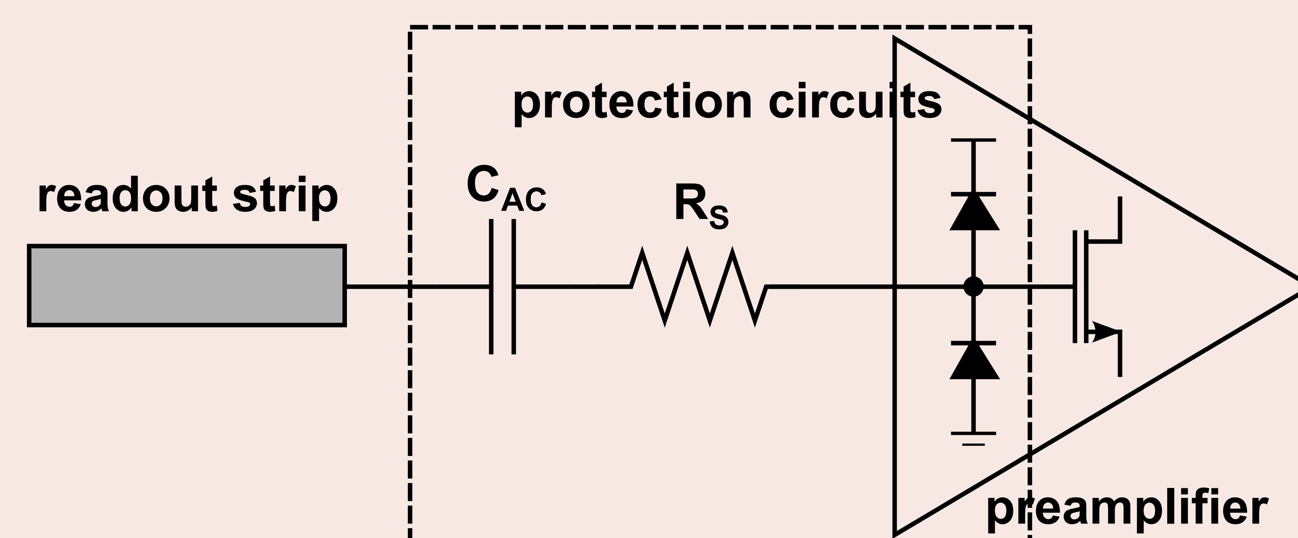




Integrated protection circuits

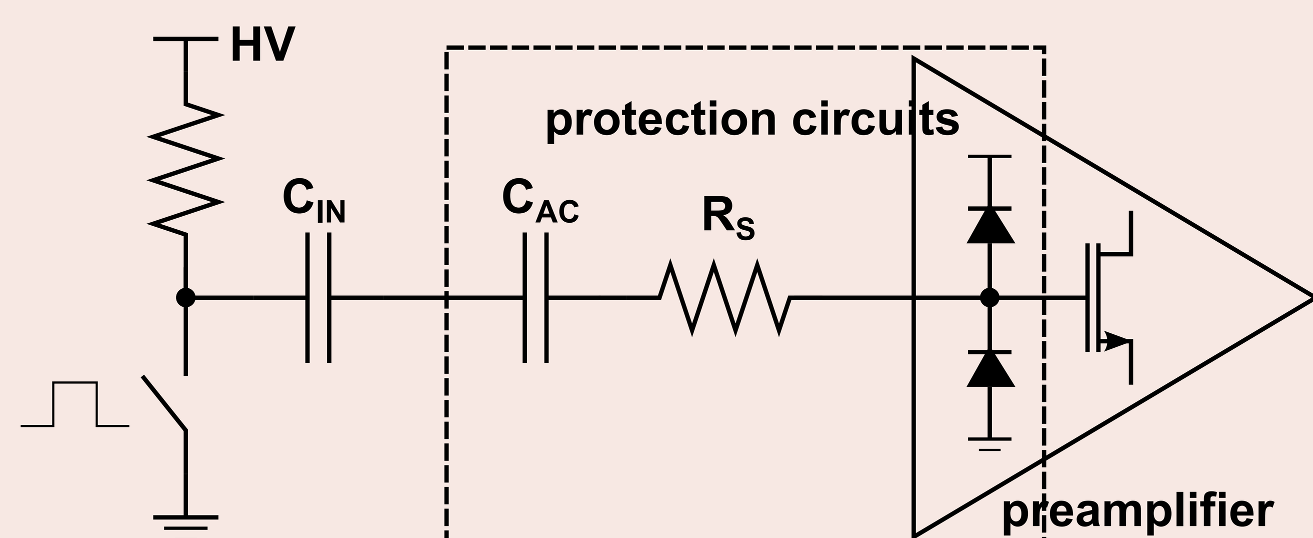
- Small area (0.42 mm × 2.4 mm for 16 channel prototype).
- Additional junction capacitance.
- Less expensive PCB technology.
- Much less demanding assembly techniques.
- No additional cost of elements.
- Specifically tuned for given type of MPGD.





Discharge measurements

- Charge injected through 1nF capacitor C_{IN}.
- HV increased in 200 V steps from 0 to 1800 V.
- Standard tests: 5 pulses @ 1 Hz frequency.
- Aggressive tests: 1000 pulses @ 10 Hz frequency.
- Different values of resistor R_S used: 20, 33, 43, 56, 68 Ω.
- Different footprints of resistor R_S used: 1206, 0805, 0603.
- After every HV step analogue performance (gain) of a given channel was measured.
- No deterioration in the front-end performance was observed.



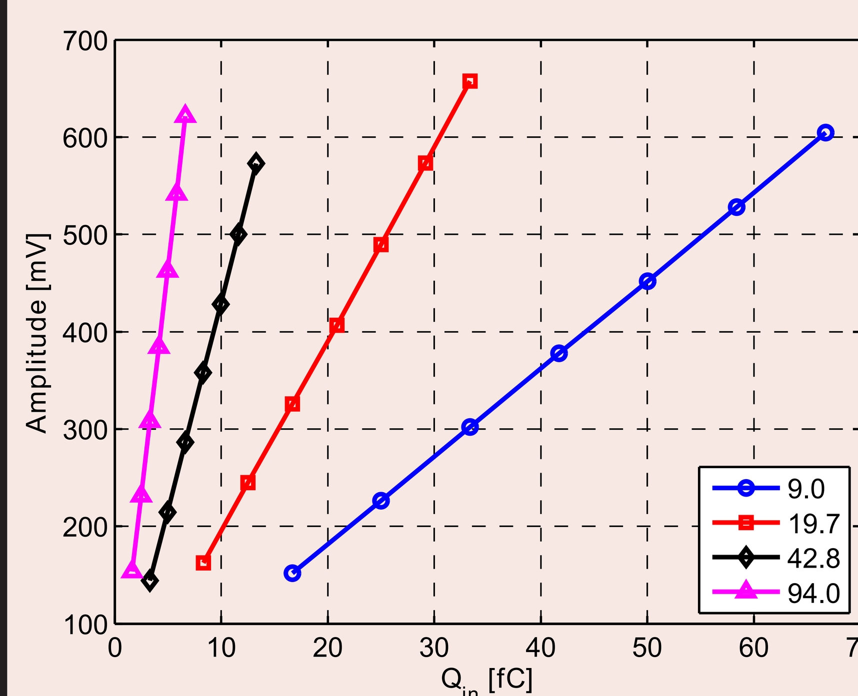
Front-End performance

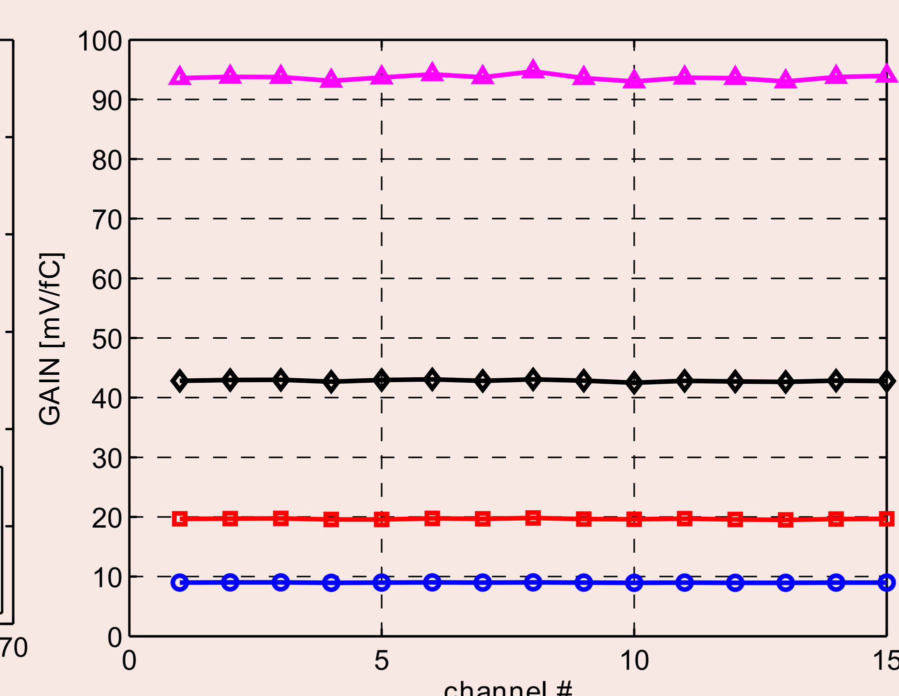
ASIC specification:

- Dedicated for MPGD.
- Measured parameters: X/Y, T, E_X/E_Y.
- Four gain modes (×1, ×2, ×4, ×10) to work with different gas gains.
- Input signal range up to 250 ke^-
- Two shaping modes: 0.3 μs and 1 μs .
- ENC about 1100 e^- @ 1 μs shaping mode.

Measurement results

gain[mV/fC]	ENC[e^-]
9.0	1120
19.7	1100
42.8	730
94.0	730





Future prospects

The accomplished discharge measurements showed no degradation in the ASIC performance, so in the near future more extensive tests will be performed to assess lifetime of the protection circuits. In the next step new prototype with protective diodes of different geometry, in order to reduce input capacitance of the front-end, is planned. It is also foreseen to evaluate the possibility of integration of the series resistor R_S.

Acknowledgements

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