



Contribution ID: 193

Type: Poster

## Front-end electronics for Micro Pattern Gas Detectors with integrated input protection against discharges

Wednesday, September 30, 2015 4:38 PM (1 minute)

One of the major problems that have to be addressed in the design of the front-end electronics for readout of MPGDs, is its resistance to possible random discharges inside active detector volume. This issue becomes particularly critical for the electronics built as ASICs implemented in a modern CMOS technology, for which the breakdown voltages are in the range of a few Volts, while the discharges may result in voltage spikes of even thousand of Volts. The paper presents test results of input protection structures integrated in the ASIC using an electrical circuit to mimic discharges in the detectors.

### Summary

One of the major problems that have to be addressed in the design of the front-end electronics for readout of MPGDs, is its resistance to possible random discharges inside active detector volume. A commonly used solution to this problem are input protection circuit built of discrete Surface Mount Device (SMD) components. Such a solution has, however, several drawbacks, including large area occupied by the SMD components and associated stray capacitance, necessity of using advanced and expensive Printed Circuit Board (PCB) technology, demanding assembly techniques, and high cost of the components themselves. These issues become particularly critical for systems with high channel counts and high density readout employing the front-end electronics built as multichannel ASICs implemented in modern CMOS technologies.

With continuous downscaling of the CMOS technologies the breakdown voltages of transistors are becoming lower and lower and for any CMOS device input protection is needed to prevent damages during handling and assembling of such devices. Therefore, the problem of Electro Static Discharge (ESD) is being continuously investigated in the field of CMOS integrated circuits. The vendors of the CMOS technologies deliver recommended ESD protection circuits, which are qualified according to the standards used in the electronics industry. Within these standards the voltages vary in the range from 2kV to 10kV. Although the voltages are comparable with the voltages used for biasing the MPGDs the equivalent electrical circuit of a MPGD is different compared to the circuit used in the ESD. First of all, in case of a discharge occurring in the MPGD the resistance of the discharging path is much lower. Thus, a protection circuits against discharges on MPGDs have to handle much higher currents and the typical circuits recommended for protection against ESD are not adequate at all.

On the other hand, the resistance of the front-end circuit against sparks occurring in MPGDs depends on the design of the front-end circuit itself, in particular on its input impedance. Therefore, the input protection circuit should be tuned specifically for a given type of MPGD and given design of the input stage if one wants to minimize additional capacitance and resistance at the input, which will affect the noise performance of the system.

The paper presents test results of input protection structures integrated with a specific design of the front-end electronics designed and manufactured in the 350nm CMOS process from the Austria Microsystems (AMS). The structures were tested using an electrical circuit to mimic discharges in the detectors for different voltage and current parameters of the sparks. The front-end electronics connected to a MPGD is exposed to multiple discharges so that not only determination of absolute maximum rating for the protection circuits is important

but also the lifetime measured in the number of discharges. Therefore, some number of test structures was exposed to the lifetime test.

**Authors:** Dr WIACEK, Piotr (AGH University of Science and Technology); Dr KOPERNY, Stefan Zenon (AGH University of Science and Technology); Dr FIUTOWSKI, Tomasz (AGH University of Science and Technology (PL)); Prof. DABROWSKI, Wladyslaw (AGH University of Science and Technology (PL))

**Presenter:** Dr FIUTOWSKI, Tomasz (AGH University of Science and Technology (PL))

**Session Classification:** Poster

**Track Classification:** ASICs