
Contribution ID: **192** Type: **Oral**

# The PCIe-based readout system for the LHCb experiment

*Thursday, 1 October 2015 16:30 (25 minutes)*

The upgrade of the LHCb experiment at CERN will implement a trigger-less readout system in which all the data are transported to the computing farm over 12000 optical links without hardware filtering. The event building and event selection is entirely operated in the farm.
Another originality of the system is that data from the detector arrive directly in computers through a specially designed PCIe card called PCIe40.
This presentation will explain these design choices and will describe the performance of the PCIe40 board and the overall system.

## Summary

The LHCb experiment is designed to study differences between particles and anti-particles as well as very rare decays in the beauty and charm sector at the LHC. However, the existing hardware trigger running at maximum 1 MHz introduces limits in LHCb's data-taking capabilities.
Therefore, the detector will be upgraded in 2018 in order to significantly increase its efficiency. It will implement a trigger-less readout system in which all the data from every LHC bunch-crossing are transported to the computing farm over 12000 optical links without hardware filtering. The event building and event selection are carried out entirely in the farm.
Another original feature of the system is that data transmitted through these fibres arrive directly in computers through a specially designed PCIe card called PCIe40.

The same board handles the data acquisition flow and the distribution of fast and slow controls to the detector front-end electronics. It embeds one of the most powerful FPGAs currently available on the market with 1.2 million logic cells. The board has a bandwidth of 480 Gbits/s in both input and output over optical links and 100 Gbits/s in each direction over the PCI Express bus to the CPU.

We will present how data circulate through the board and in the PC server for achieving the event building.

We will focus on specific issues regarding the design of such a board with a very large FPGA, in particular in terms of power supply dimensioning and thermal simulations.

The features of the board will be detailed and we will finally present the first performance measurements.

**Primary author:** RETHORE, Frederic (Centre National de la Recherche Scientifique (FR))

**Co-authors:** HACHON, Frederic (Centre National de la Recherche Scientifique (FR)); CACHEMICHE, Jean-Pierre (Centre National de la Recherche Scientifique (FR)); LE GAC, Renaud (CPPM CNRS/IN2P3)

**Presenter:** RETHORE, Frederic (Centre National de la Recherche Scientifique (FR))

**Session Classification:** Systems, Planning, installation, commissioning and running experience

**Track Classification:** Systems