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Development and experimental study of the Read-out ASIC for Muon Chambers of the CBM Experiment

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The measurement results of the front-end ASIC for GEM detectors for Muon Chambers in the CBM experiment are presented. The MUCH ASIC was designed and prototyped via Europractice by means of the 0.18 um CMOS MMRF process of UMC (Taiwan). The parameters of the analog channels, including the CSA, fast and slow shapers, discriminators were measured. The channels provide a sufficient dynamic range of 100 fC, low power consumption of 10 mW and ENC of 1000 el at 50 pF detector capacitance. The further plans on the chip development is also discussed.

Summary

The measurement results of the front-end ASIC for GEM detectors readout in the CBM experiment are presented. The ASIC was developed for the use as a part of the muon system in the Compressed Baryonic Matter (CBM) experiment at the upcoming FAIR facility in Darmstadt (Germany).

The ASIC was designed and prototyped via Europractice by means of the 0.18 um CMOS MMRF process of UMC. The die size is 3240 x 1525 um2. The chip has 90 pads. To perform the lab tests it was packaged in CPGA120.

The design has the following main parameters: dynamic range of 100 fC, channel hit rate of 2 MHz, ENC of 1000 e- at 50 pF equivalent detector capacitance, power consumption of 10 mW per channel. The chip includes 8 analog processing chains, each consisting of preamplifier, two shapers (fast and slow), differential comparator and an area efficient 6 bit SAR ADC with 1.2 mW power consumption at 50 Msps sampling rate. The chip also includes the threshold DAC and the output serializer.

The preamplifier is based on the folded cascode CSA architecture with additional gain boosting. The preamplifier gain is set to 5 mV/fC. Input signal polarity is negative. The CSA output signal rise time is 50 ns.

Since CBM MUCH GEMs will have different granularity, the requirements to the front-end electronics are also different for the central and peripheral parts. Thus, the preamplifier is followed by two chains: a slow channel optimized for S/N ratio in order to use it in the periphery, and a fast channel, adapted to the hit rate of the inner detector part, where the occupancy is the highest. The fast channel is also supposed to use for the timestamp determination. Time over threshold method is used for the software timestamp correction. Both channels are realized with CR-RC shapers with different peaking times, 60 ns and 260 ns accordingly. The ENC of the fast and slow shaper no more than 1500 el and 1000 el correspondently at 50 pF of the equivalent detector capacitance.

The test PCB was developed to provide the measurements of the ASIC. The PCB includes analog 50 Ohm buffers, linear power supplies, equivalent detector capacitance blocks, calibration capacitances, digital drivers. The logic signal level shifters, transceivers and digital connectors are placed to the PCB to use it with the Nexys4 FPGA development board. The FPGA board is necessary to generate the digital code sequences to control the ADC and the DAC data registers and to process the digital signals from the ASIC SAR ADC.

The parameters of the analog channels were measured, including the CSA, fast and slow shapers, discriminators. The channels provide a sufficient dynamic range of 100 fC, low power consumption of 10 mW per channel and ENC of 1000 el at 50 pF detector capacitance for the slow shaper.

Prototypes of the gas-filled detectors based on the GEM and TGEM technologies have been studied with the prototype front-end ASIC. A prototype system is being developed in PNPI (Gatchina) and MEPhI (Moscow) for the use as muon tracker in the CBM experiment. The noise, energy and time resolution were estimated at different count rates. Main aim of the lab tests was to reach a noise at level of 1000 el rms for the slow channel at low detector capacitances. The tests results are presented. Further development of the next MUCH ASIC version is planned.

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