Trigger Algorithms and Electronics for the ATLAS Muon NSW Upgrade

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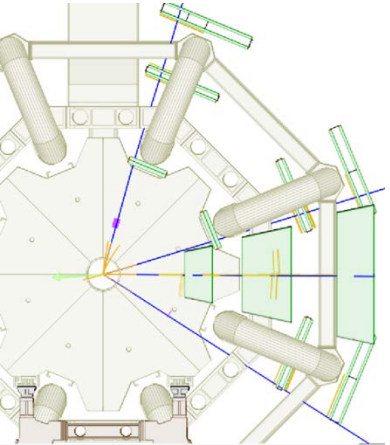
on behalf of the ATLAS Muon Collaboration



Topical Workshop on Electronics for Particle Physics
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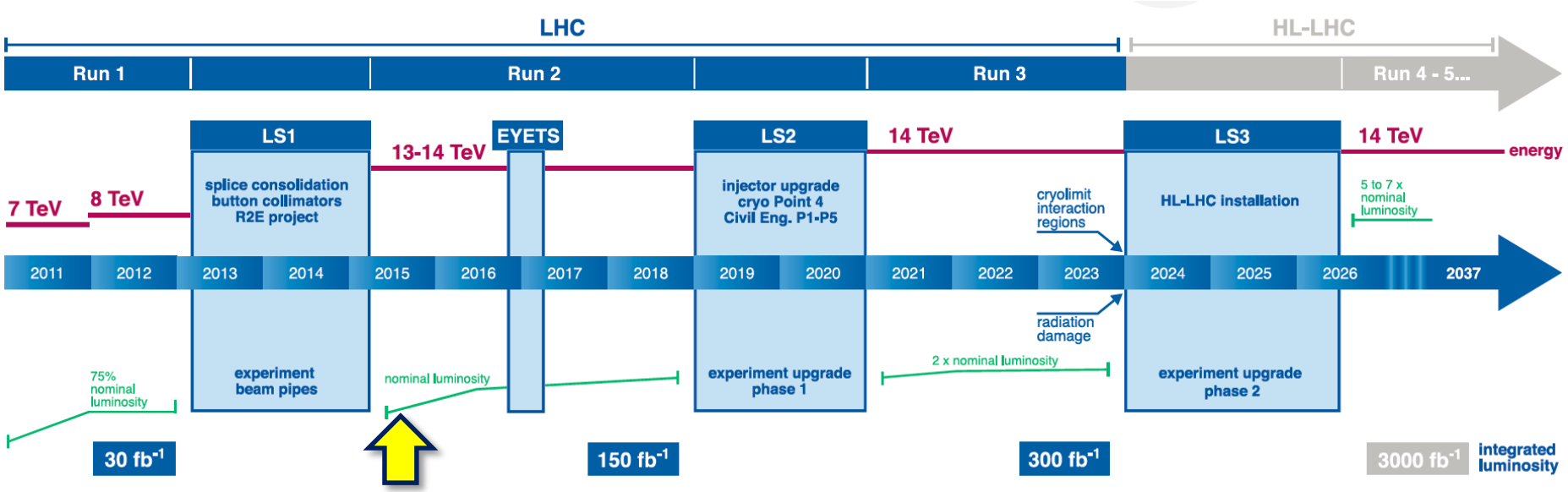
Outline

- Introduction: ATLAS Muon NSW Upgrade
- Part I: NSW Trigger Processors and Trigger Algorithms
- Part II: NSW Trigger Front-end Electronics
- Conclusions and Outlook

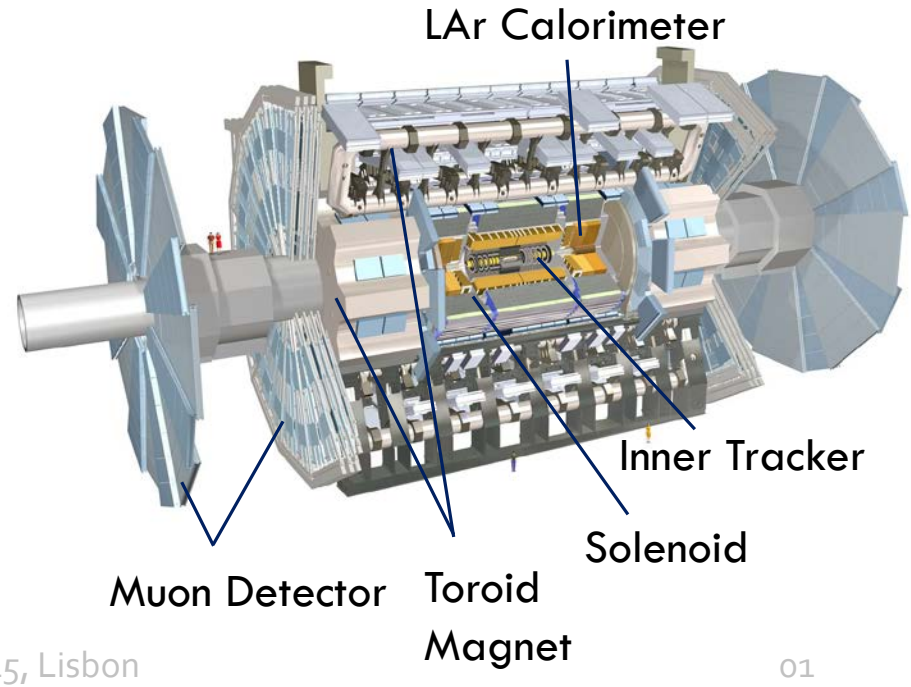
Introduction – LHC and ATLAS upgrade schedule



We Are Here!

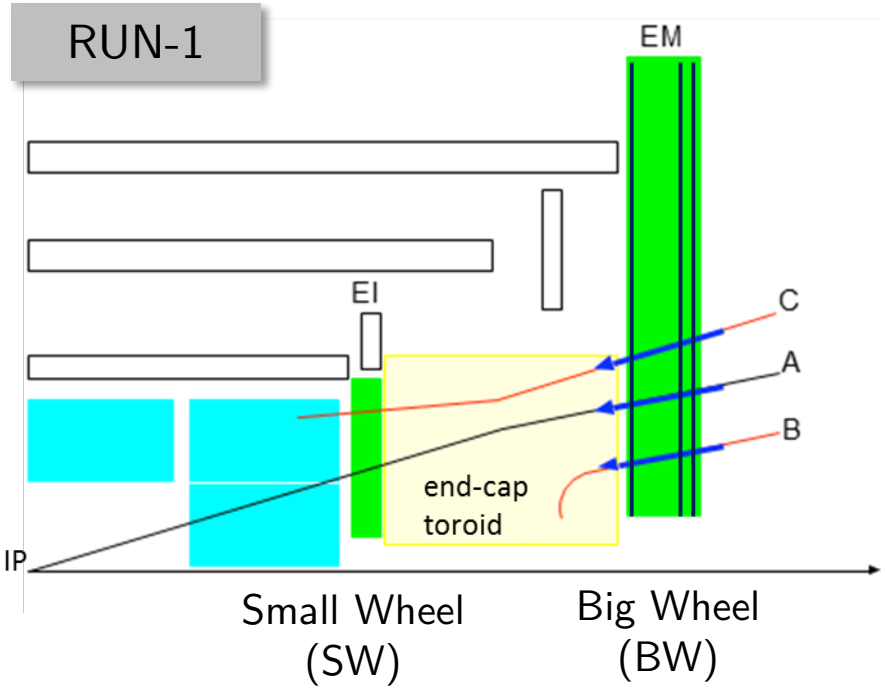
ATLAS Main Upgrades

- Phase-0: Insertable B-Layer (IBL) in LS1
- Phase-1: Muon New Small Wheels, Calorimeter trigger, Fast Tracker
- Phase-2: New Inner Tracker, New Trigger architecture, Muon Spectrometer …



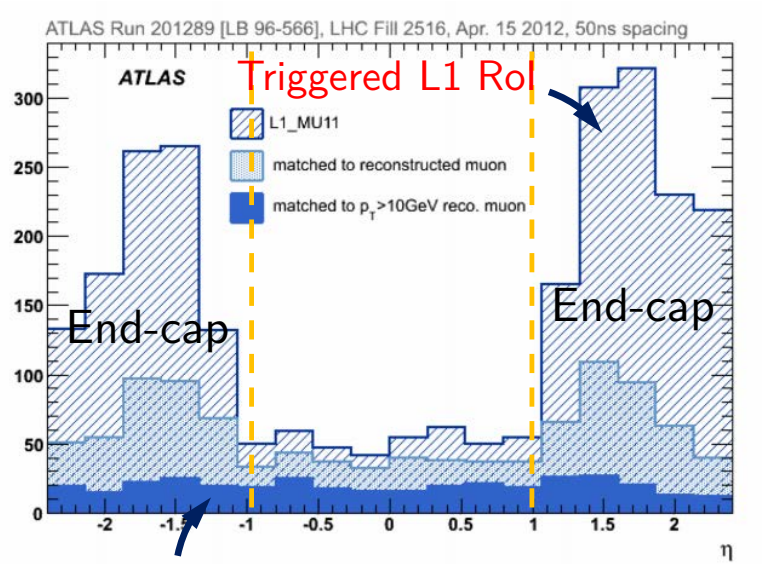
Introduction – ATLAS Muon NSW Upgrade

- RUN-1 ATLAS Level-1(LV1) Muon Trigger in the End-cap Region only relies on segment measurements at the Big Wheel using Thin Gap Chambers



η Distribution of LV1 muon (p_T>10 GeV)

50 ns Bunch Spacing

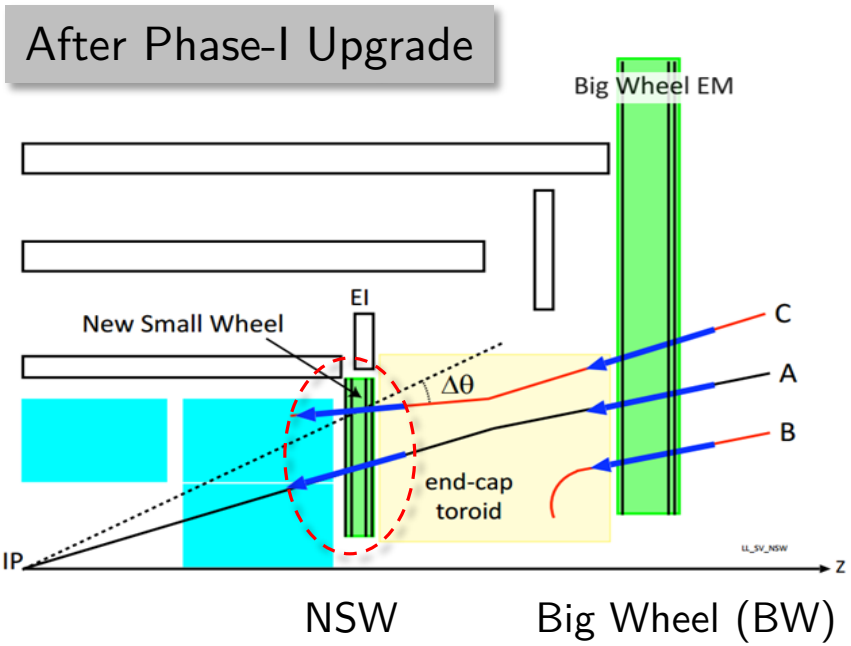


Matched with off-line
(p_T>10 GeV)

⇨ Trigger rate dominated by the End-cap due to backgrounds: "fake" and real muons indistinguishable at high luminosity

Introduction – ATLAS Muon NSW Upgrade

- Muon New Small Wheel (NSW) Upgrade: Replace Small Wheel to improve End-cap LV1 trigger & maintain good tracking for LHC high luminosity runs

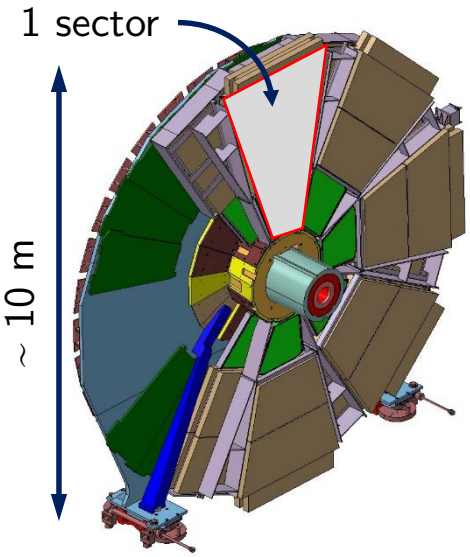


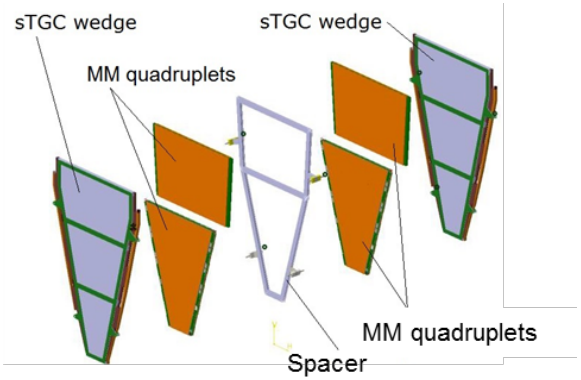
Trigger → $1.3<|\eta|<2.4$ $1.0<|\eta|<2.4$

- Accurate on-line segment measurements at NSW together with Big Wheel segments to eliminate non-IP originating backgrounds
- With NSW, LV1 muon ($p_T>20$ GeV) trigger rate expected to be reduced from 60 kHz to 22 kHz @ $L=3\times10^{34}cm^{-2}s^{-1}$, $\sqrt{s}=14$ TeV, 25 ns BC
- Requirements for NSW trigger:
  - 1 mrad on-line segment pointing accuracy (Phase-II requirement)
  - ~ 1 μs latency to be in time with Big Wheel trigger (~ 500 ns for fiber)
  - 95% on-line track reconstruction efficiency

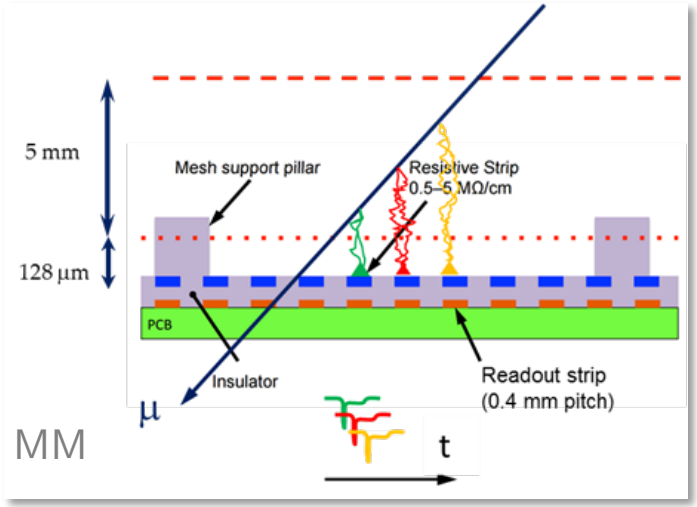
Introduction – ATLAS Muon NSW Upgrade

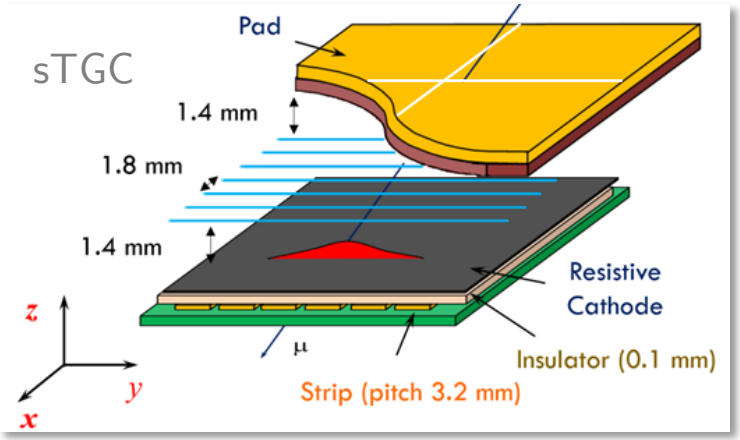
- NSW Detector Technologies:
  - Micromesh Gaseous Structure Detector, Micromegas (MM)
  - Small-strip Thin Gap Chamber (sTGC)





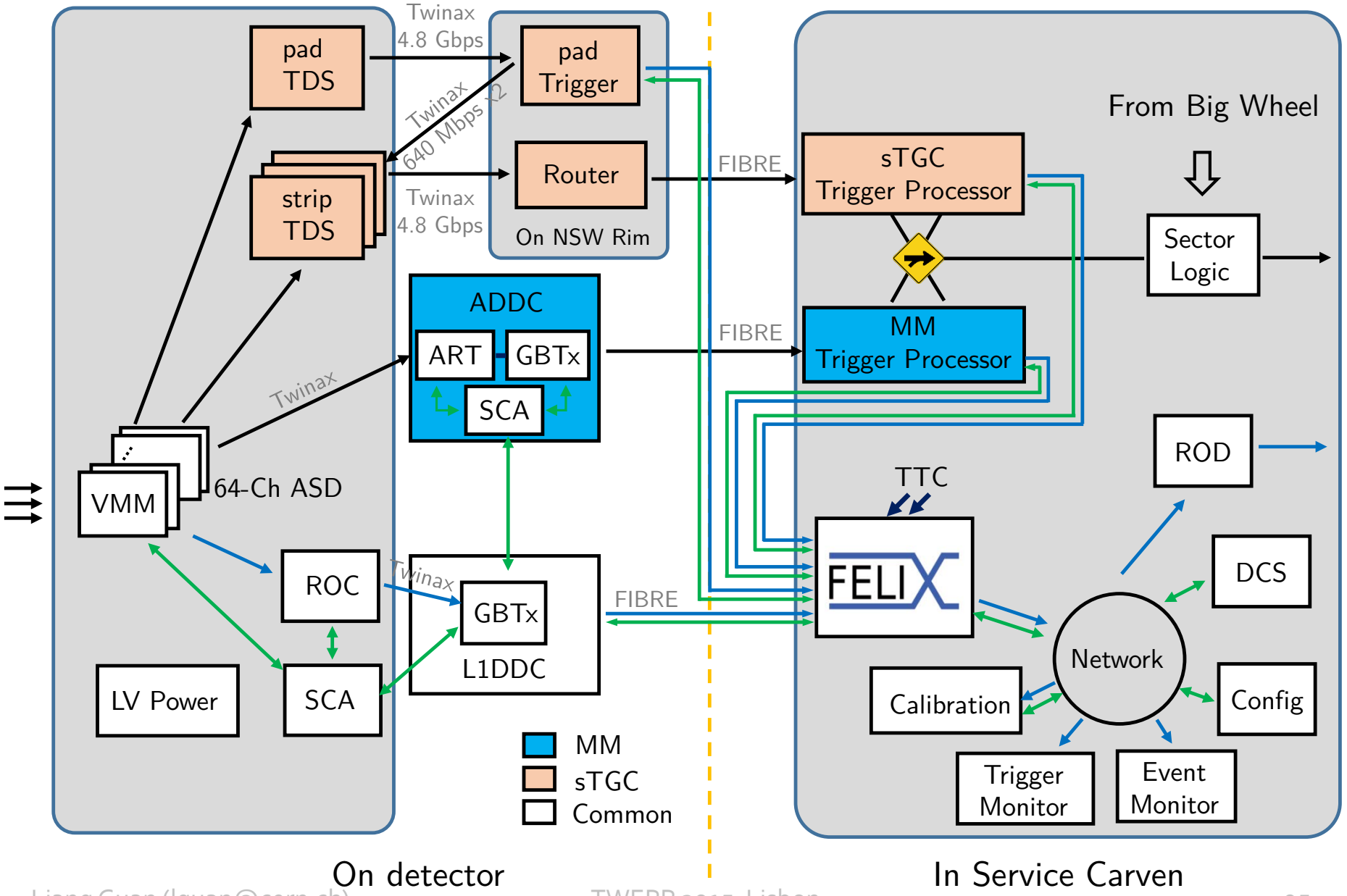
Readout channels:
- MM: ~ 2.1 M
- sTGC: 280k (strip) + 46k (pads) + 28k (wires)





- Both detector technologies will be used for trigger and tracking (only trigger discussed here)

Introduction – NSW Trigger and Readout Complex



Part I: NSW Trigger Processors and Trigger Algorithms

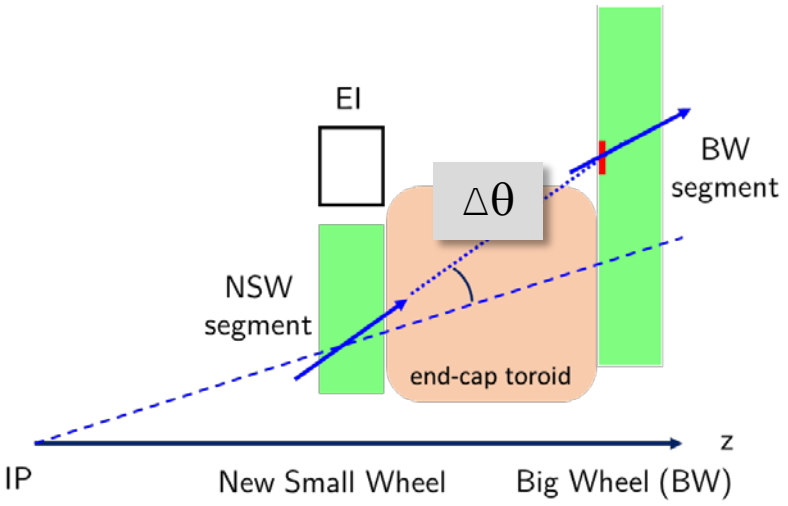
NSW Trigger Primitives Raw Information

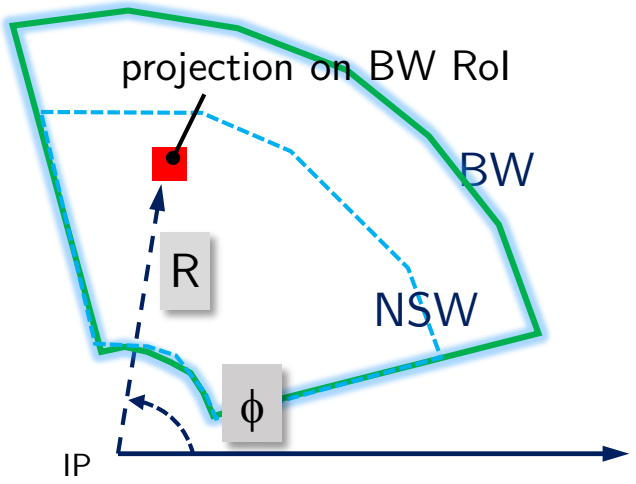
- NSW Trigger Processors reconstruct segments on each sector

Segment pointing — Projection on BW RoI

Data format for 1 segment

Field	sTGC hit	MM hit	Δθ (mrad)	ϕ index	R index	Spare
#. of bits	2	2	5	6	8	1
		Resolution:	1 mrad	20 mrad	0.005 (η)	

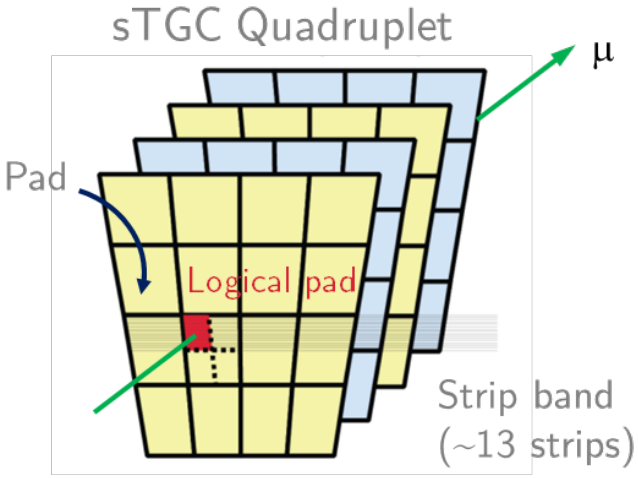




- MM and sTGC employ separate Trigger processor to find segments
- Baseline design: send 8 candidates per sector per Bunch Crossing

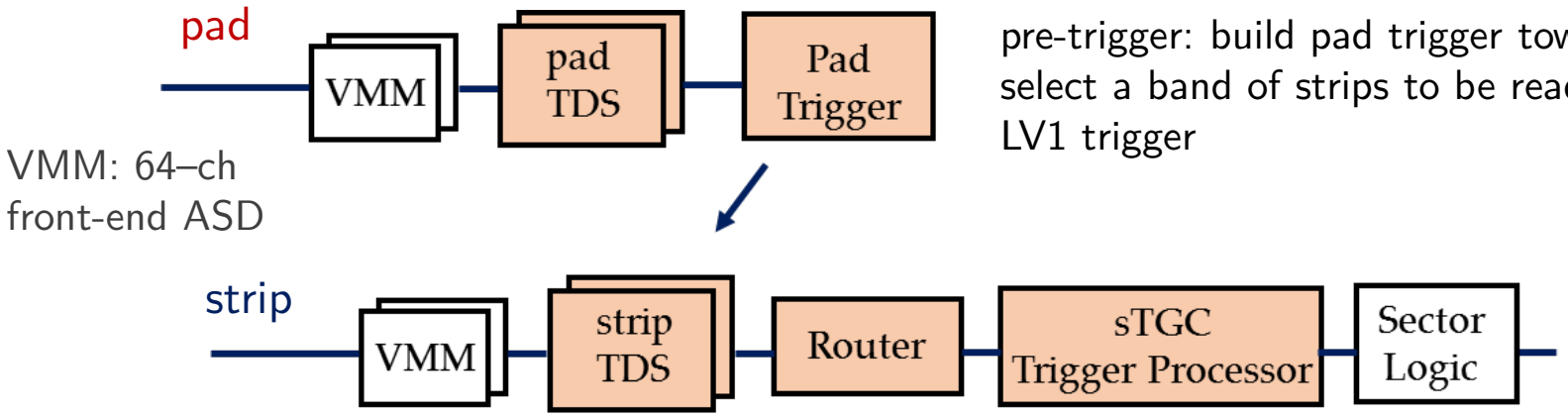
sTGC Trigger Algorithm

- sTGC Trigger Scheme



Data Arriving at sTGC Trigger Processor:

- Strip Band-ID
- Pad Tower ϕ–ID
- Charges of strips in selected band



pre-trigger: build pad trigger tower to select a band of strips to be read out for LV1 trigger

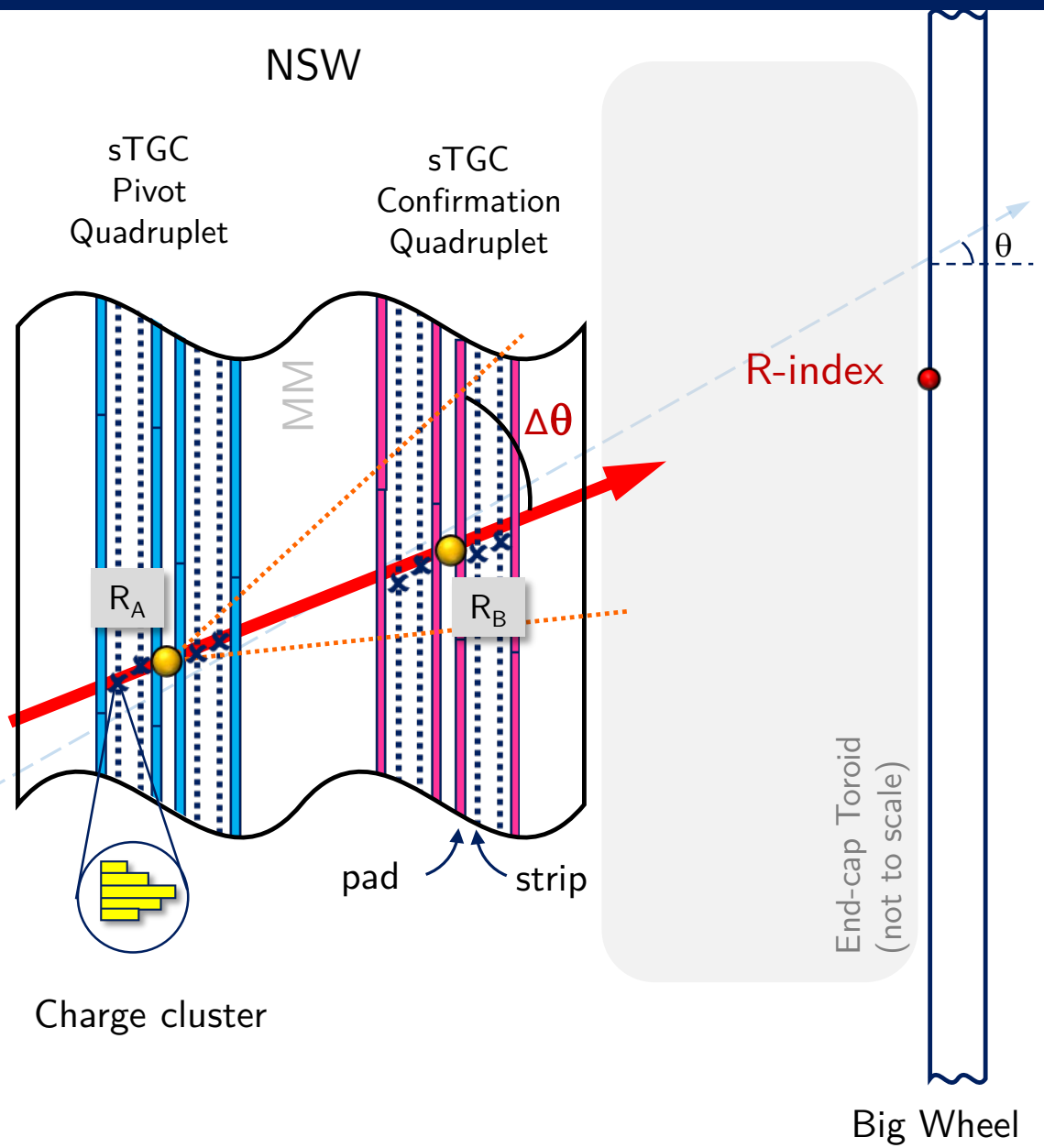
Trigger Data Serializer (TDS): strips or pads trigger data preparation, strip-pad match

Router: aggregates data from active TDS

sTGC Trigger Algorithm

Algorithm Principles

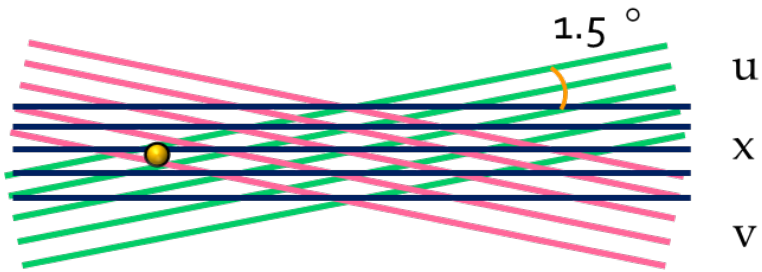
- Layer centroid calculated using good clusters (3-5 strips) and added with offset to reflect cluster global position
- Two quadruplet centroids calculated to define the segment pointing ($\Delta\theta$)
- R-index calculated based on pivot quad. centroid and segment pointing
- ϕ-index directly available as pad trigger tower ϕ-ID



MM Trigger Algorithms

MM Trigger Scheme

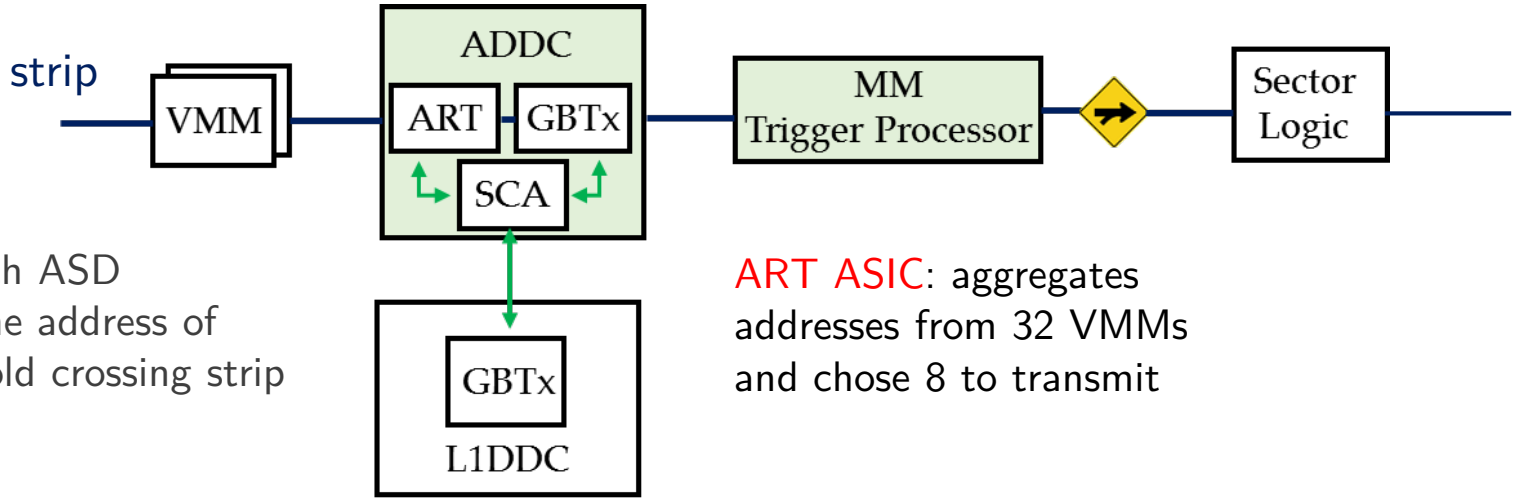
MM strip arrangement



x: horizontal strip (2 plans per quad.)
u,v: stereo strip (1 each per quad.)

Data Arriving at MM Trigger Processor:

- Up to 64 strip addresses per detector plane (strip pitch 0.4 mm)

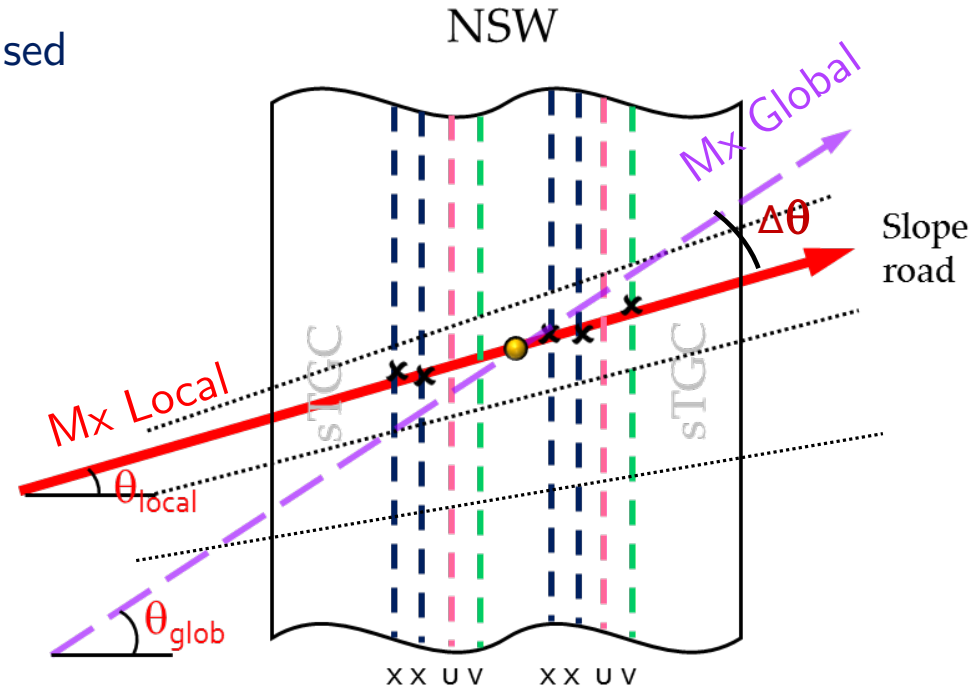


VMM: 64–ch ASD providing the address of first threshold crossing strip in an event

ART ASIC: aggregates addresses from 32 VMMs and chose 8 to transmit

MM Trigger Algorithms (Con't)

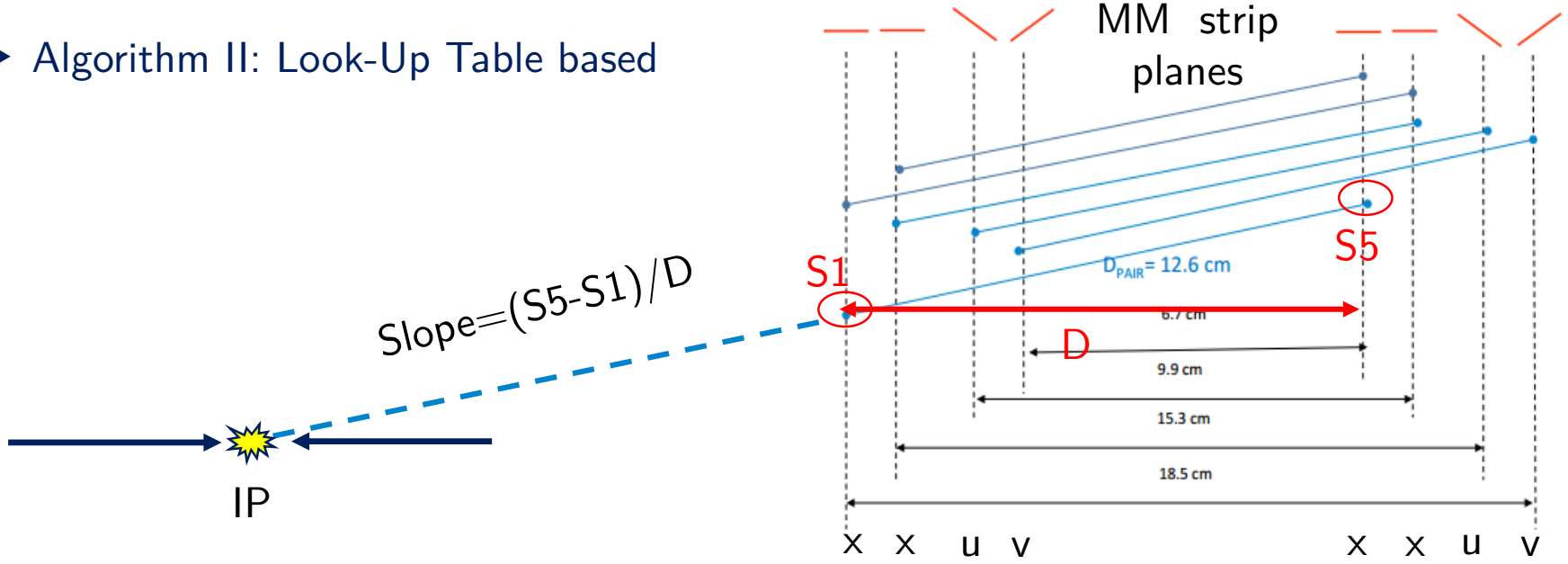
- Algorithm I (Baseline design): Fitting-based
  - Convert hits to slopes and bin into slope roads
  - Define a track candidate as multi-layer coincidence within a slope road
  - Calculate global and local slopes
  - Determine $\Delta\theta$ using global and local slopes of horizontal plane
  - Derive RoI projected on Big Wheel (R, ϕ-index): using global slopes of horizontal and stereo planes



- Global slope: average of x/u/v slopes
- Local slope: least square fit of x plane slopes (n=2,3,4)

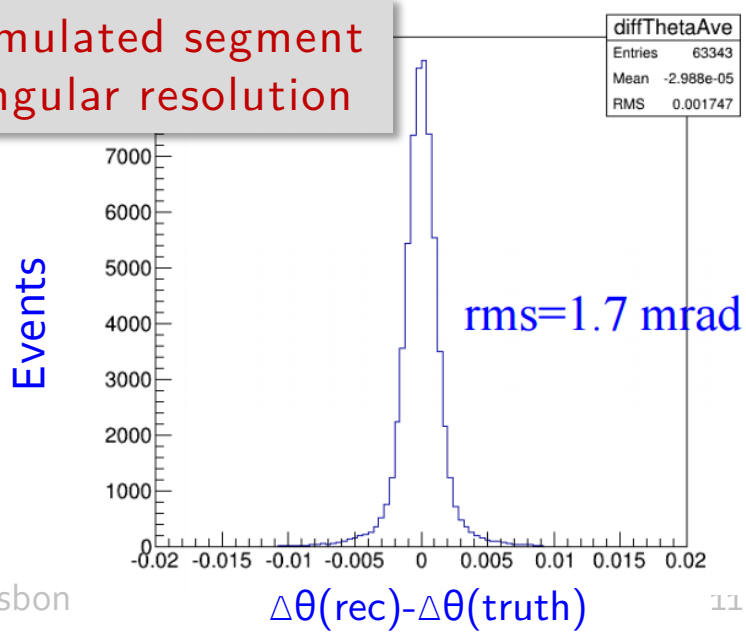
MM Trigger Algorithms (Con't)

- Algorithm II: Look-Up Table based



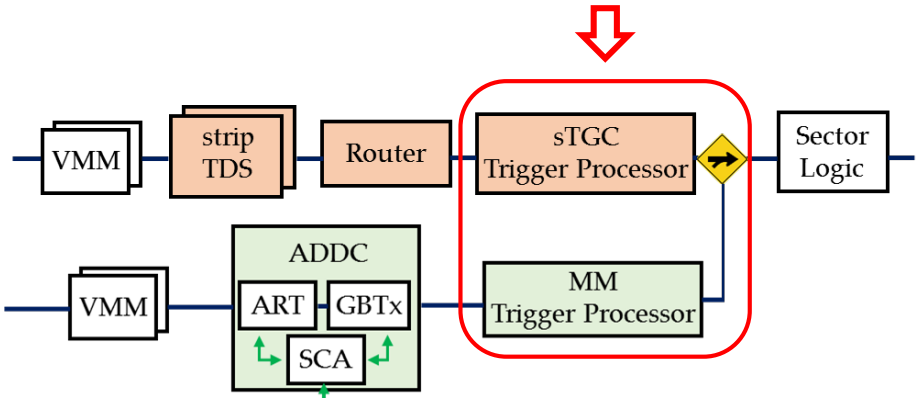
- Convert hits to slopes in 6 layer pairs using LUT (LUT instructs hit pairing and translates strip address difference into slope)
- Match of slopes in multiple layer pairs defines a track candidate
- Average slopes of horizontal and stereo layer pairs used to calculated RoI and $\triangle\theta$

Simulated segment angular resolution

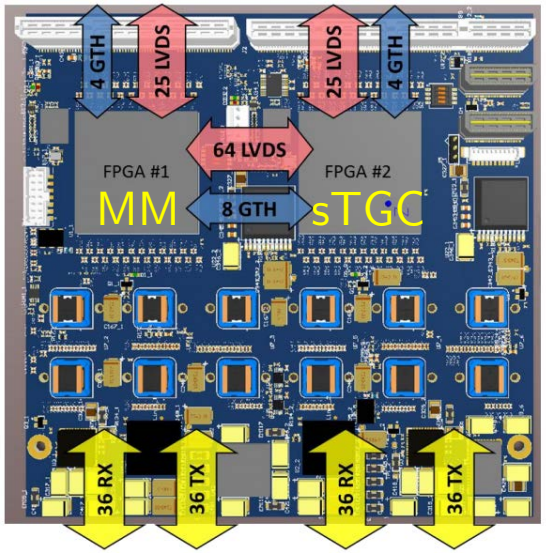


Trigger Processor Hardware Platform

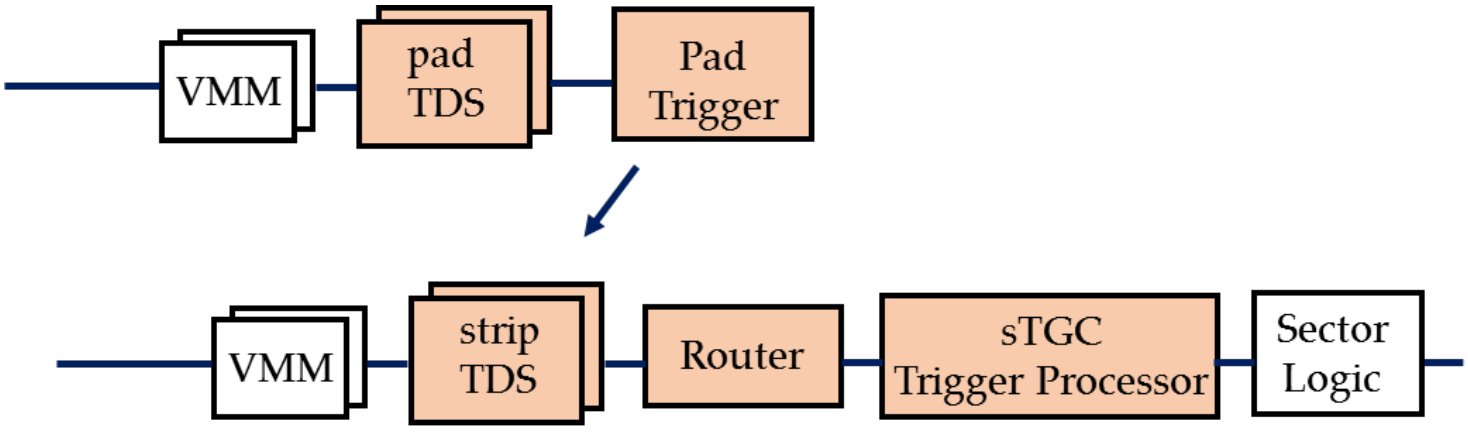
- MM & sTGC trigger processor to be implemented on FPGA-based ATCA Mezzanine Cards
- Baseline: adopt ATCA Mezzanine card developed for Scalable Readout System* (SRS) platform
- 1 Mezzanine card for 1 NSW sector: 2 FPGAs, one for MM/sTGC trigger processor
- Mezzanine card main specification:
  - 32 input fibers (MM/sTGC)
  - 14 output fibers @ 6.4 Gbps+
  - Fast low latency link between MM and sTGC processors for lateral communication
- 1 ATCA carrier card hosts 2 Mezzanine cards (NSW sectors)



ATCA Mezzanine Card on SRS Platform



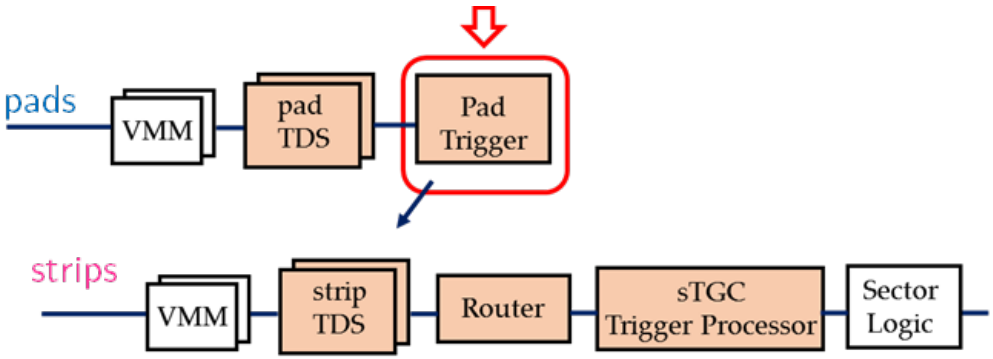
*S. Martoiu, et al., JINST 8.03 (2013): C03015.



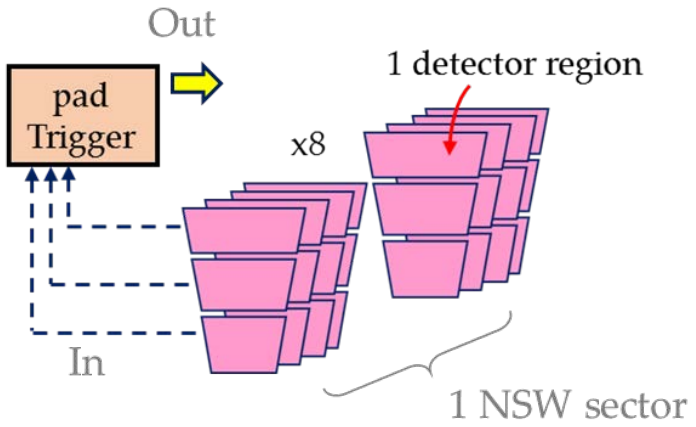
Part II (A): Trigger Electronics for sTGC System

sTGC Pad Trigger Board

- Functionality: Two 3 out of 4 pad coincidences per BC to form pad trigger road (tag BCID, define strip band to be read out)



- Main specifications:
  - 1 board per sector
  - Send up to 3 trigger candidates per sector per BC
  - Readout logic: send pad hit info after L1A for monitoring.



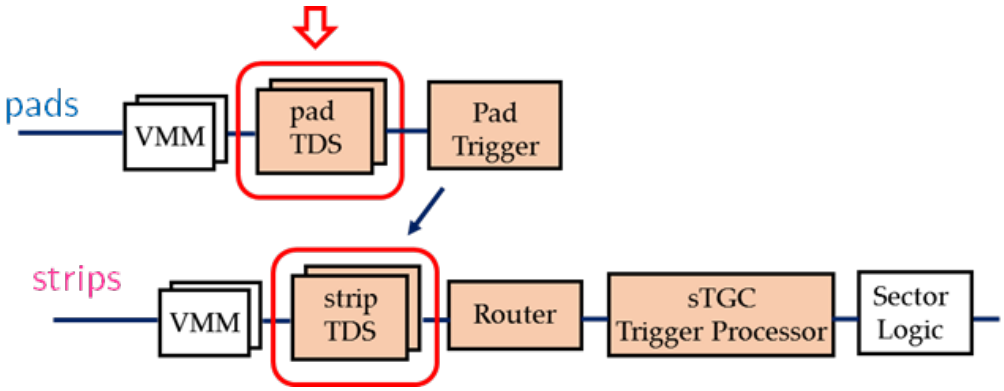
- Output to strip-TDS
  - D0: (640 Mbps) :12 bit BCID
  - D1: (640 Mbps): 8 bit Band-ID + 5-bit ϕ-ID
  - Clock: 320 MHz
  - Frame: indicates start/stop of valid trigger data transfer

Common to all strip-TDS per FEB

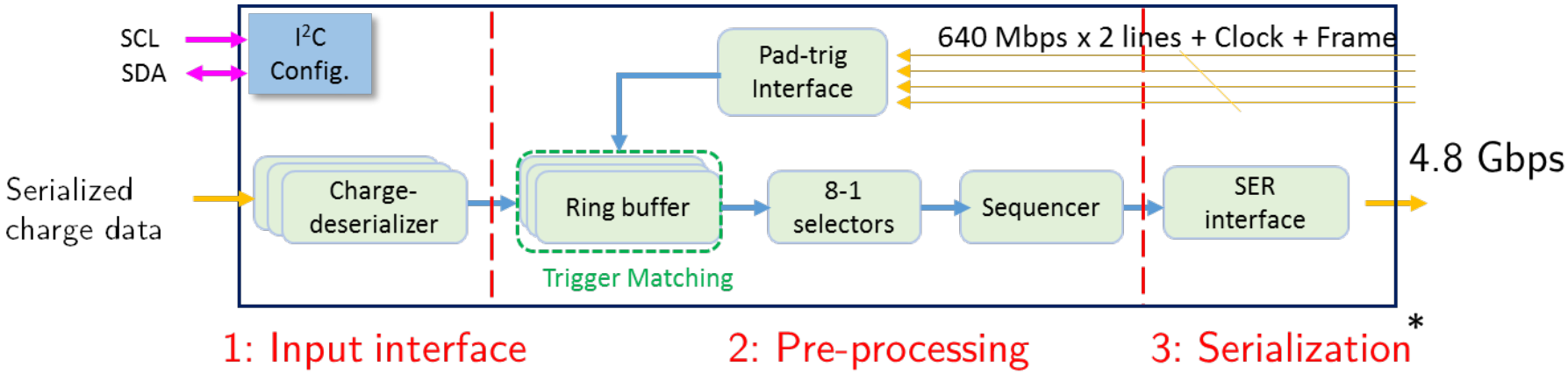
Unique to each strip-TDS

sTGC Trigger Data Serializer (TDS) ASIC

- Main specifications:
  - Two modes: strip/pad mode
  - 128 chan. w/ individual programmable delay (pad-mode only)
  - Output data rate: 4.8 Gbps
  - Rad. tolerant (logic needs to incorporate SEU protection)



- Strip-TDS block diagram

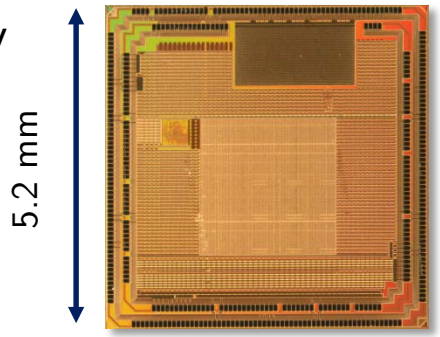


* Serializer is based on CERN GBT design with significant modification

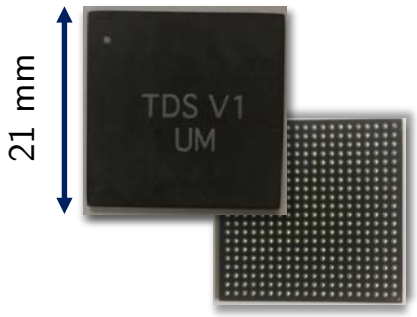
sTGC Trigger Data Serializer (TDS) ASIC

- 1st prototype: TDSv1
  - IBM 8RF-DM 323, 130 nm CMOS, 1.5 V
  - BGA Package: 20 x 20, 1 mm pitch
  - Core processing logic verified. Excellent Serializer performance.

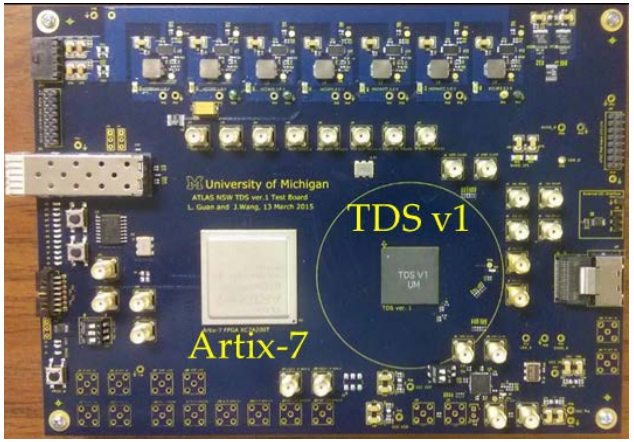
TDS v1 Silicon Die



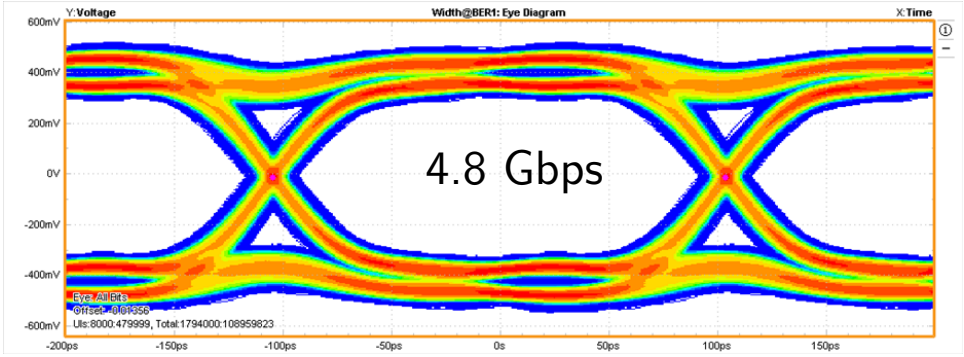
Chip Package



TDS v1 Test Board



Serializer Eye diagram from packaged TDS

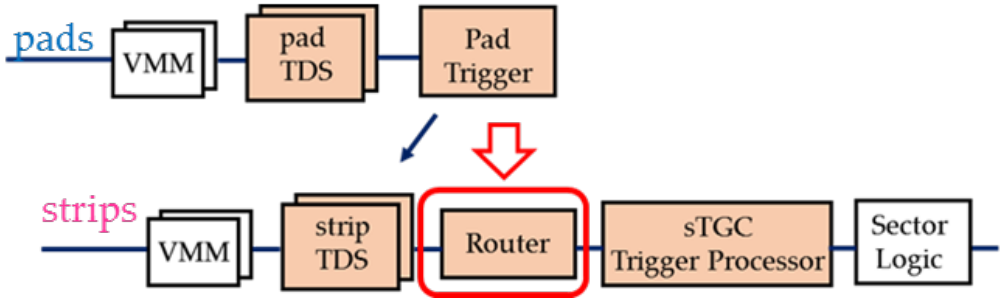


- Total jitter @ (BER 10^{-12}): 33.2 ps

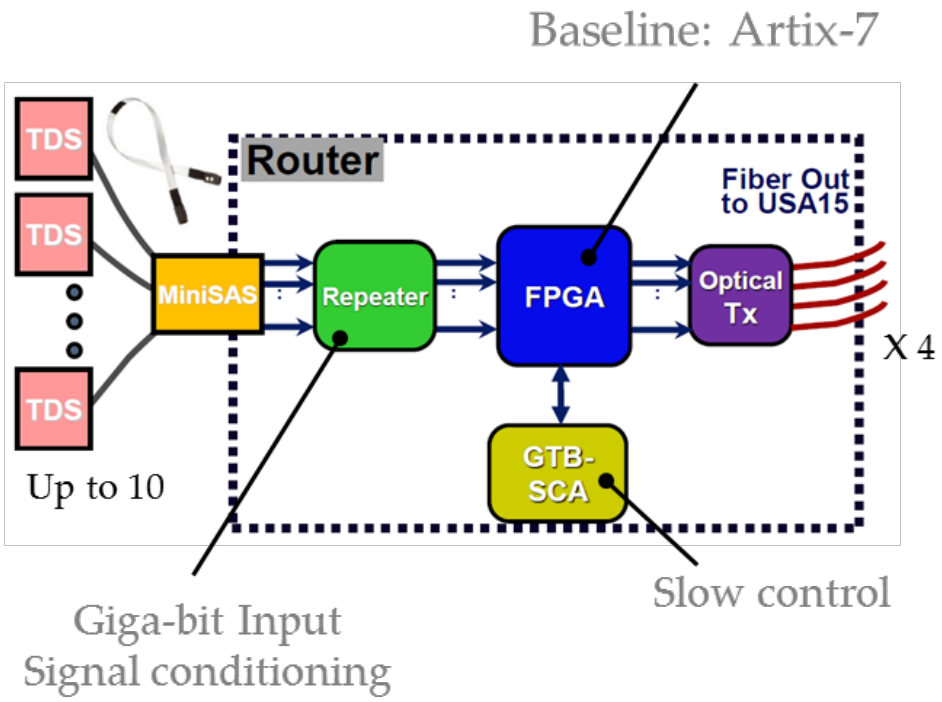
- Status: 2nd (close to final) prototype design under post layout simulation
  - Mainly implement: TMR design for critical logics; modification to logic for communicating with peripheral electronics; programmable delay (3.125 ns step) for pad inputs

sTGC Router

- Functionality: Collect data packets from active TDSs and transmit data to trigger processor

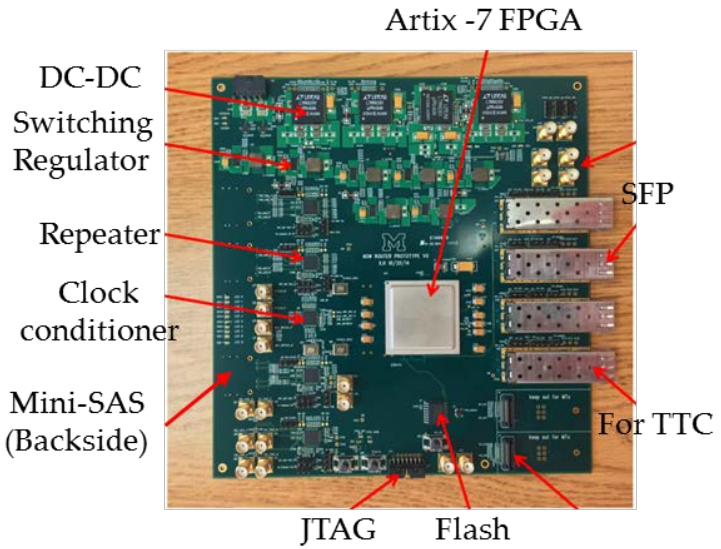


- Main specifications:
  - 1 board per detector layer per sector
  - Input: from up to 10 strip-TDSs per plane, each at 4.8 Gbps
  - Output: 4 fibers (Up to 6.4 Gbps per link with baseline FPGA)
  - Require low and fixed latency



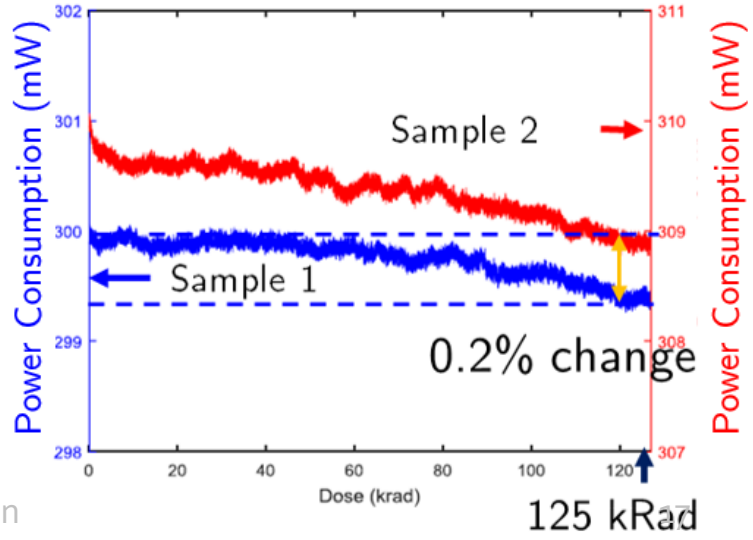
sTGC Router

- 1st Prototype
  - Firmware: recognize active input before receiving entire data frame and set-up routing
  - Link between TDS and Router demonstrated
  - Latency study: ~ 106 ns (TDS Tx + 5-m cable + Router Rx & Switching Logic)

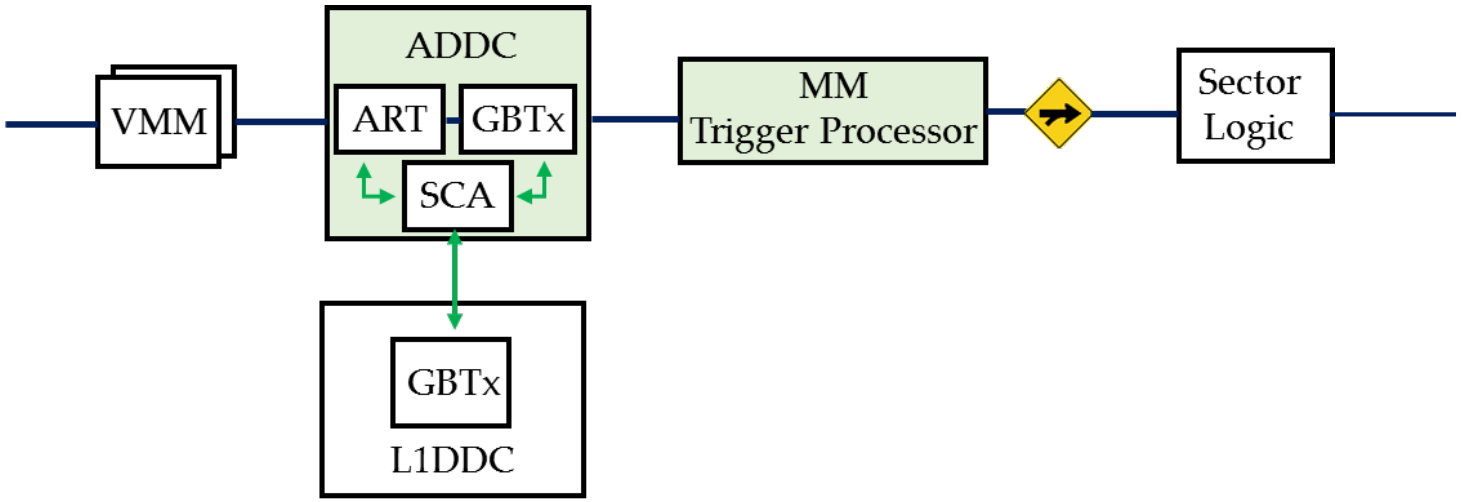


- Verification of parts radiation tolerance
  - Repeater survived 125+ krad dose (40 x simulated dose rate at NSW rim in 10-yr LHC environment)

TID test for 2 repeater (TI DS100BR410) samples



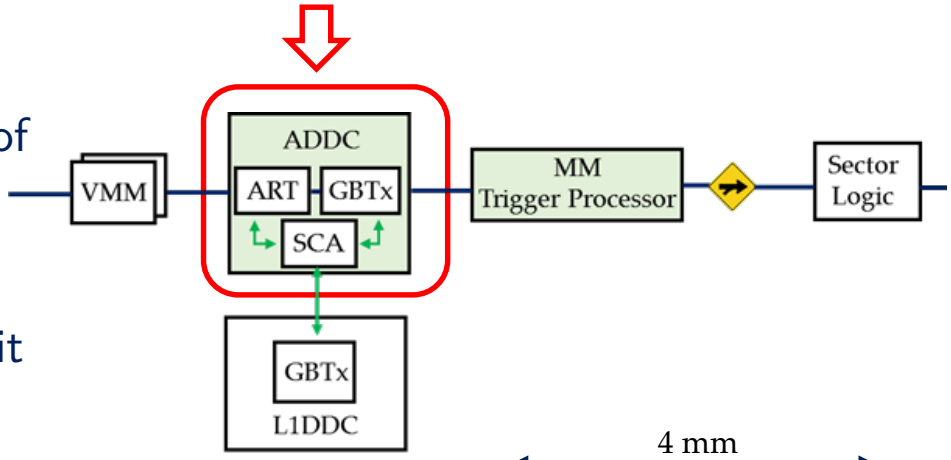
- Status: 2nd prototype under design (implement GBT-SCA, new power scheme etc.)



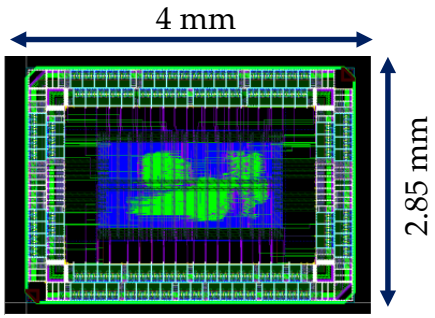
Part II (B): Trigger Electronics for Micromegas System

ART ASIC and ART Data Driver Card (ADDC)

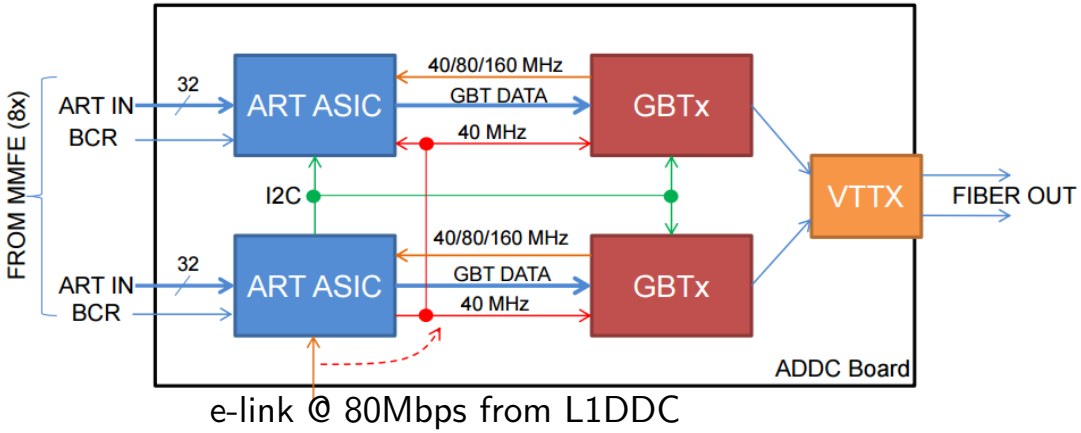
- Address in Real Time (ART): an VMM ASD output mode providing the address of first threshold-crossing strip in an event
- ART ASIC: aggregates addresses from 32 VMMs and choses up to 8 hits to transmit
- ADDC (4 per layer): incorporate 2 ART, GBTx and transmit data using optical link (CERN VTTx)



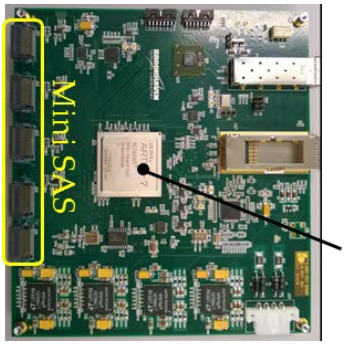
Lay out of 1st ART Prototype



Connection on ADDC



ADDC 1st Prototype

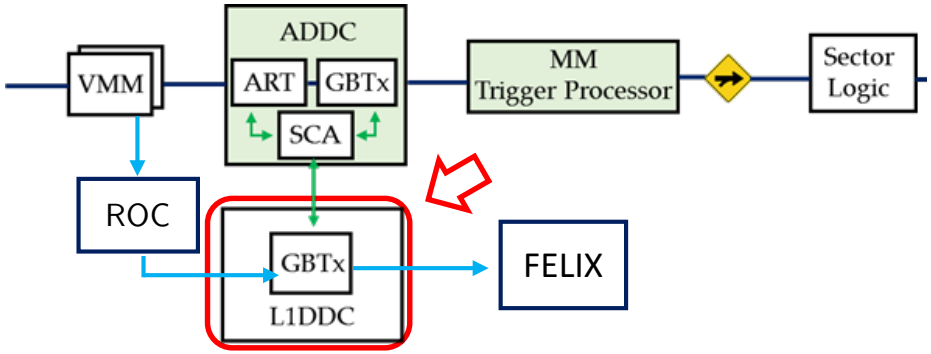


Artix-7 FPGA: ART Emulator

L1 Data Driver Card (L1DDC)

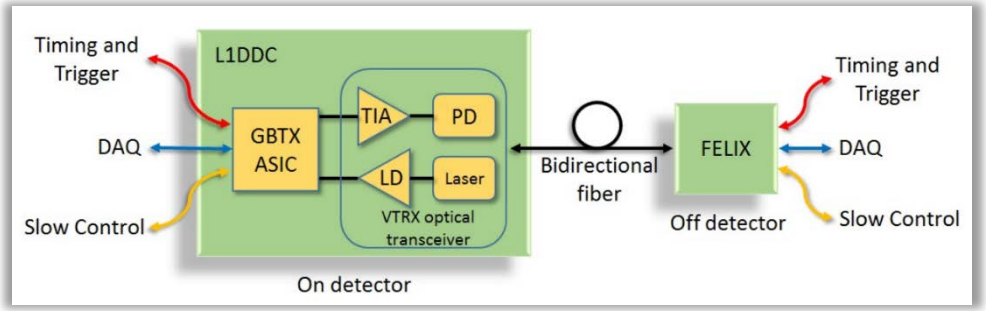
- ReadOut Controller (ROC): a companion ASIC to store hit data from VMMs until L1A. Merge L1A data from up to 8 VMMs and interface with GBTx

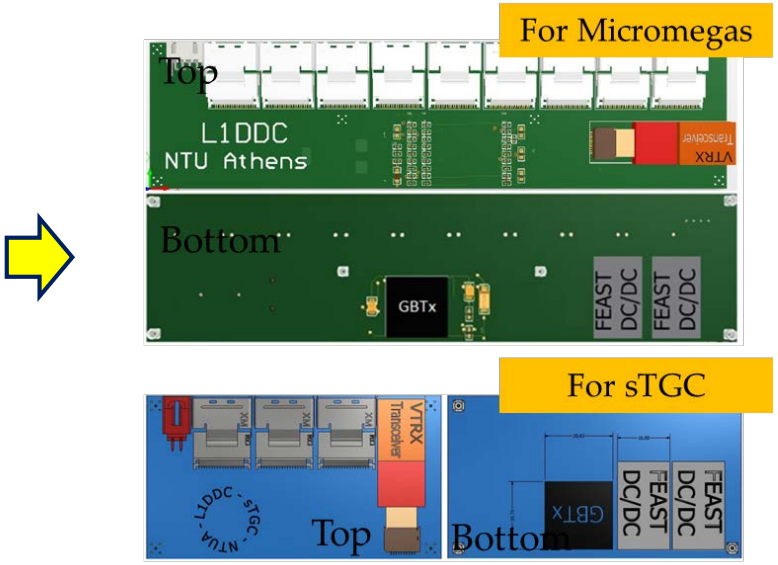
  See R. Coliban, "Design of the NSW Read-Out Controller ASIC" in poster session



L1 Readout Path

- L1DDC: Aggregates L1 readout data from FEBs and drive them to FELIX; Also used for config./monitoring and TTC distribution





- Different layout for sTGC and MM: different space constraint and connectivity needs

L1 Data Driver Card (L1DDC)

- Key components

GBTx ASIC

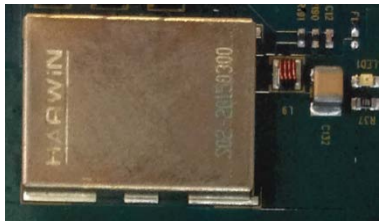
400 pin 0.8 pitch BGA

- Rad. hard* interface between front-end electronics and optical link
- bidirectional "e-link" with 80/160/320 Mbps program. rates
- Bandwidth: 4.8 Gbps

* P. Leitao, et al. JINST 10.01 (2015): C01038.

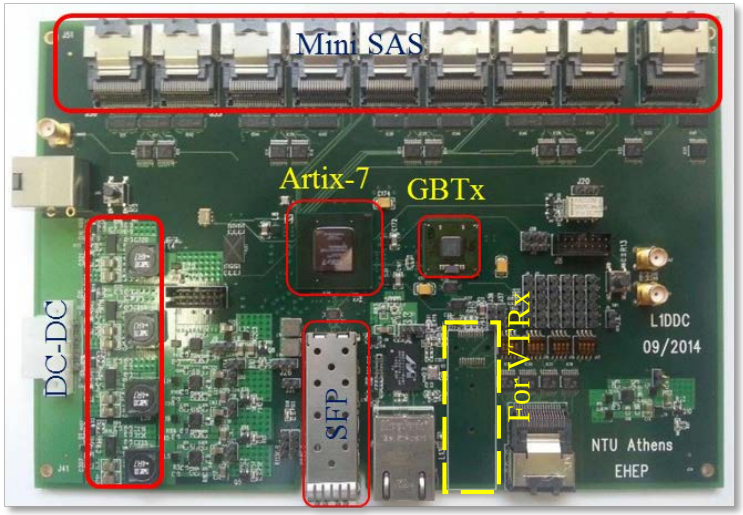
VTRx: Versatile TransReceiver

DC-DC: CERN FEAST



See R. Edgar "Low Voltage Power for the ATLAS New Small Wheel Muon Detector" in poster session

- 1st Prototype
  - Implemented with GBTx, VTRx
  - Link with mini-SAS+Twinax Cable verified: error free @ 320 Mbps
  - GBTx configuration firmware developed

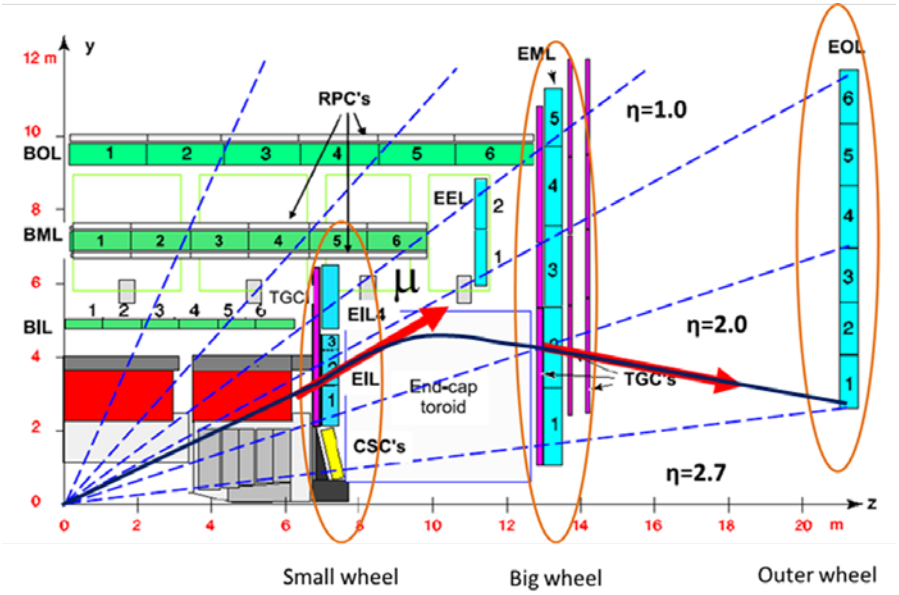


Conclusions and Outlook

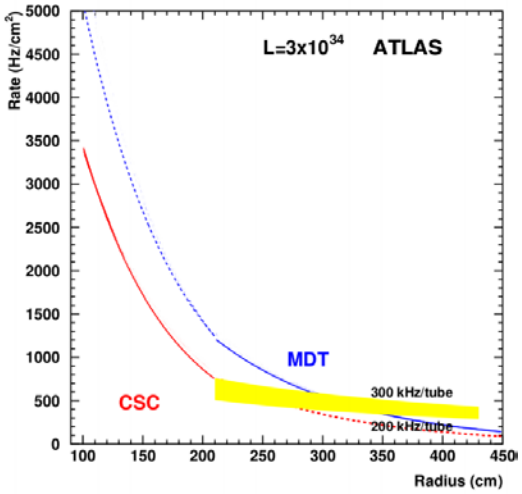
- The New Small Wheel Upgrade is necessary for ATLAS to improve the Level-1 trigger in order to maintain crucial physics program in high luminosity environment.
- The complex trigger electronics system will be designed to achieve precise on-line muon segment measurements in the forward region of the Muon Spectrometer to discriminate against high-rate backgrounds.
- Separate trigger algorithms for two sub-detector systems (MM & sTGC) have been developed, taking account of substantial readout, geometry differences
- Significant effort have been made in the design of various trigger electronics in order to be fitted within the tight latency budget.
- A vertical slice is under preparation and planned to integrate all NSW electronics.

Thank you for your attention!

Spares

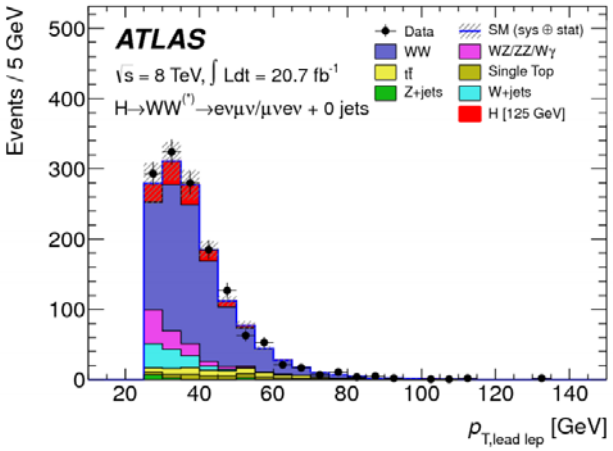


Extrapolated Rate at L=3x10^{34} cm^{-2}s^{-1} and √s=7 TeV

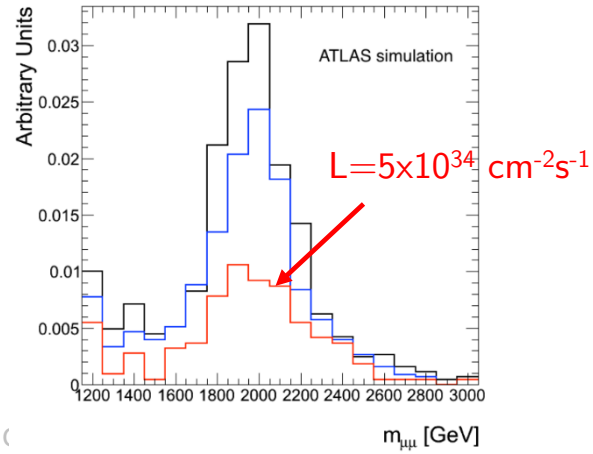


Reference: T. Kawamoto et al., NSW TDR (https://cds.cern.ch/record/1552862?ln=en)

Leading lepton p_T in H→WW→lνlν

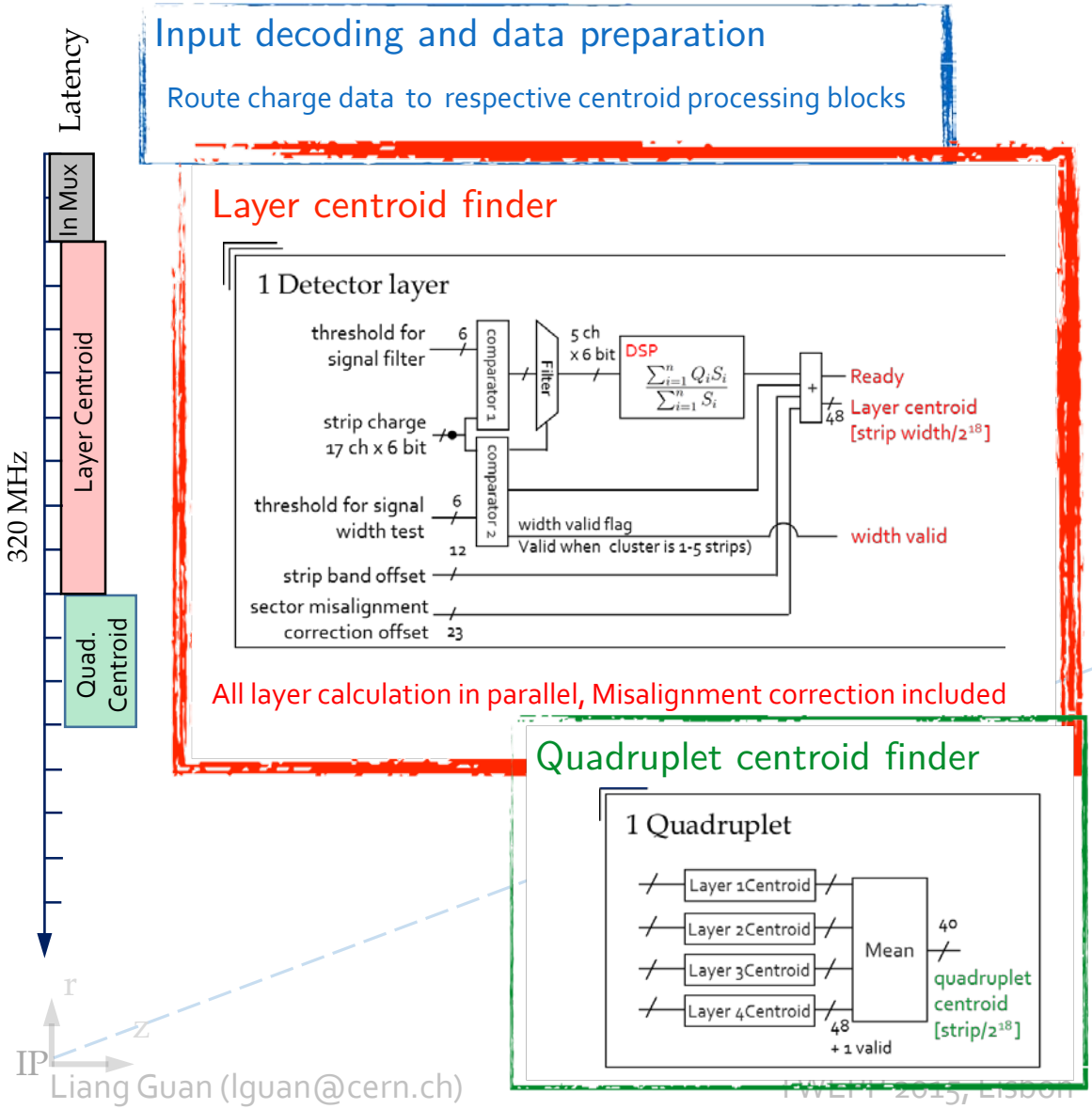


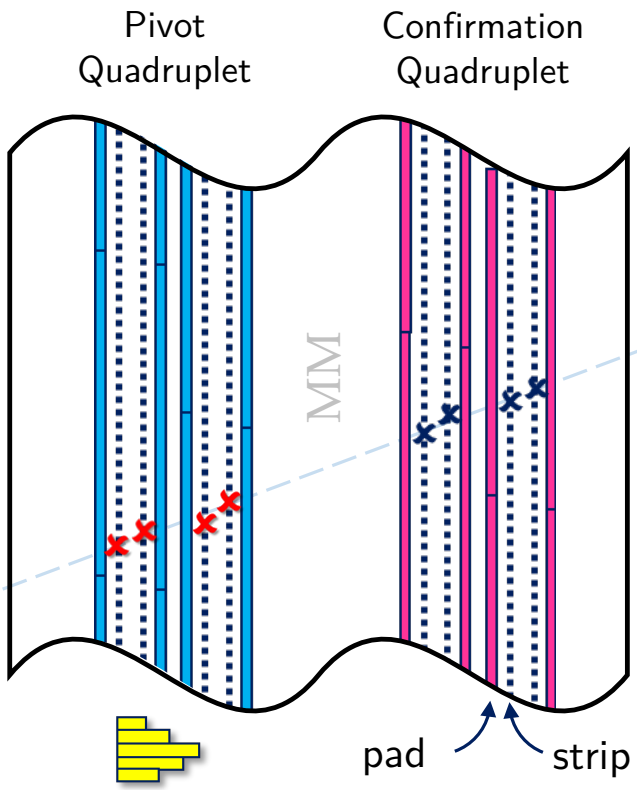
μμ mass distribution for simulated Z'→mm



Spares

- sTGC trigger algorithm (details)





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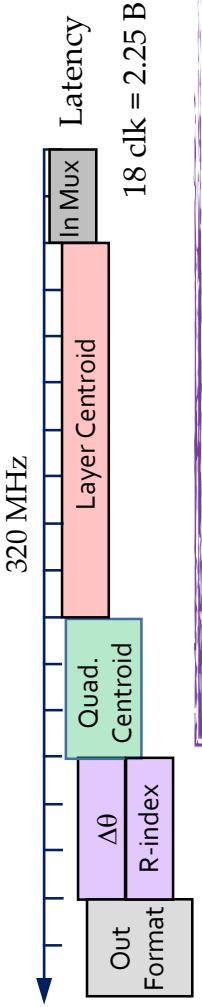
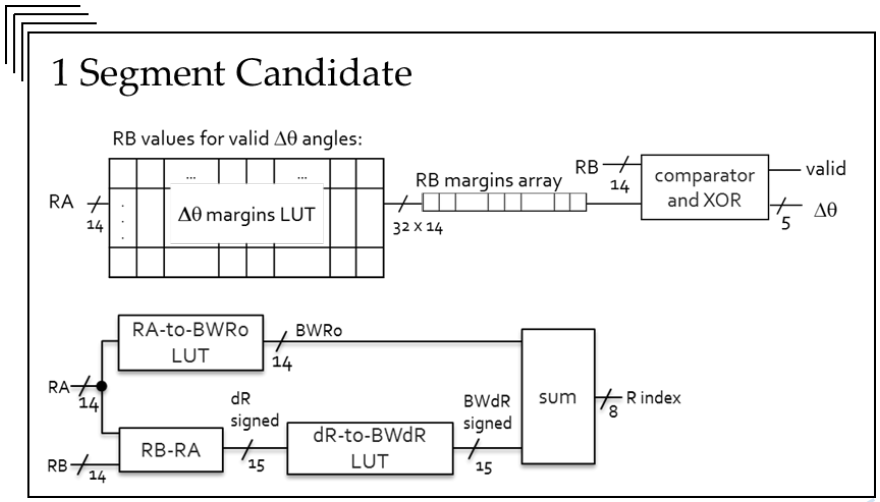


Δθ and R-index calculation

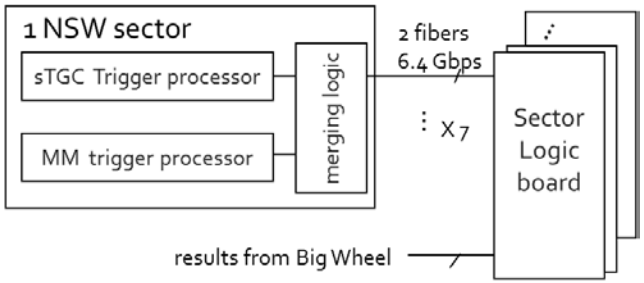


Δθ= angular between NSW segment and infinite momentum track

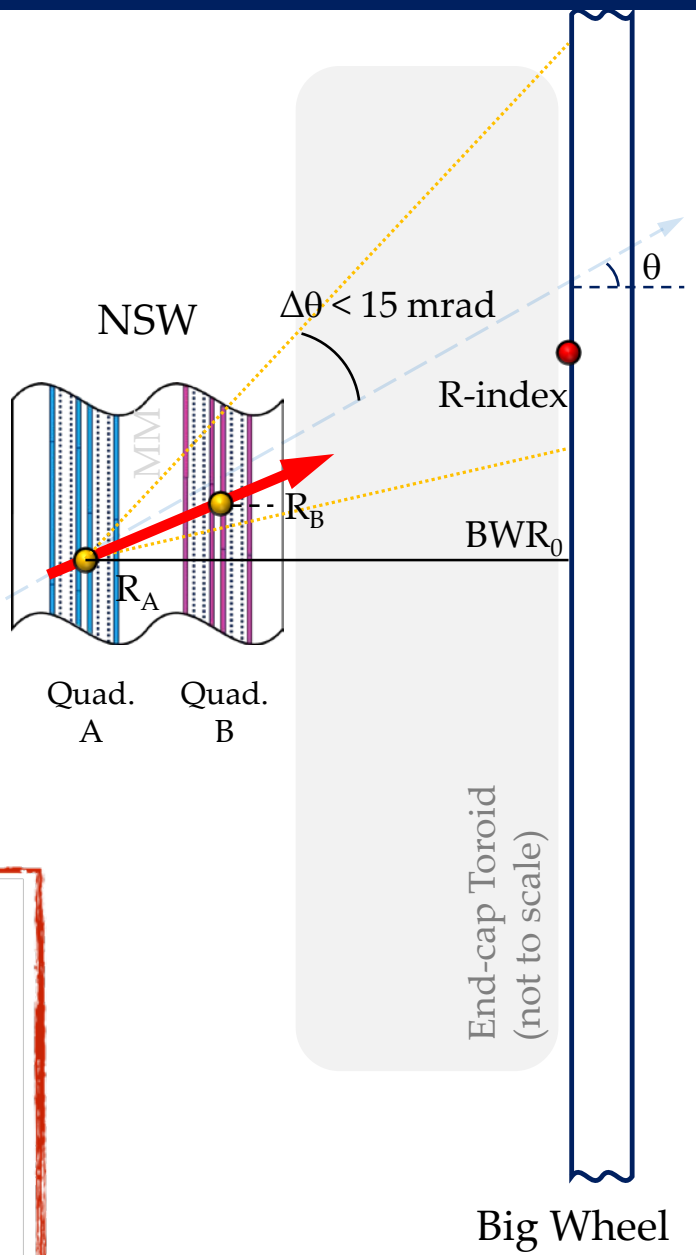
R-index= Radial mapping of NSW segment on BW

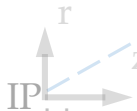
Φ-index = Azimuthal mapping of NSW segment on BW (pad trigger Φ-ID)

Merging sTGC & MM segments



Remove duplicates, select candidates based on track quality



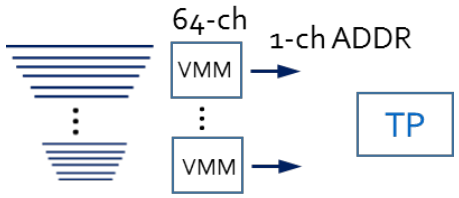


Spares

- MM fitting based trigger algorithm (details)

Input Decoding

- Convert hit strip addresses to slopes

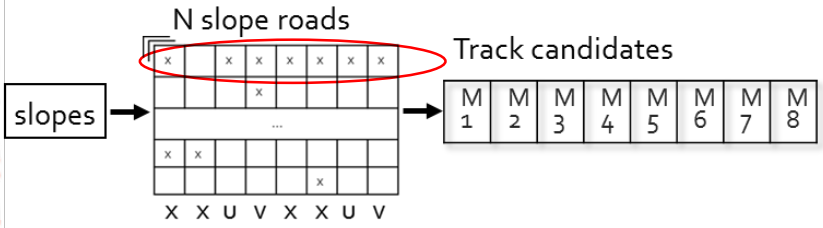


NSW sector misalignment correction could be implemented with slope

3 Clks

3 Clks

Slope finder



- translated hits slopes stored in buffer. (slope, strip address, BC)
- per BC, use LUT to find track candidates with applied N-plane-coincidence threshold

3 Clks

Slope fitter

- Calc Mx Global
- Calc Mu Global
- Calc Mv Global
- Calc Mx Local (Least squares fit of x slopes)
- U,V Slope filter

5 Clks

RoI and Δθ Calc

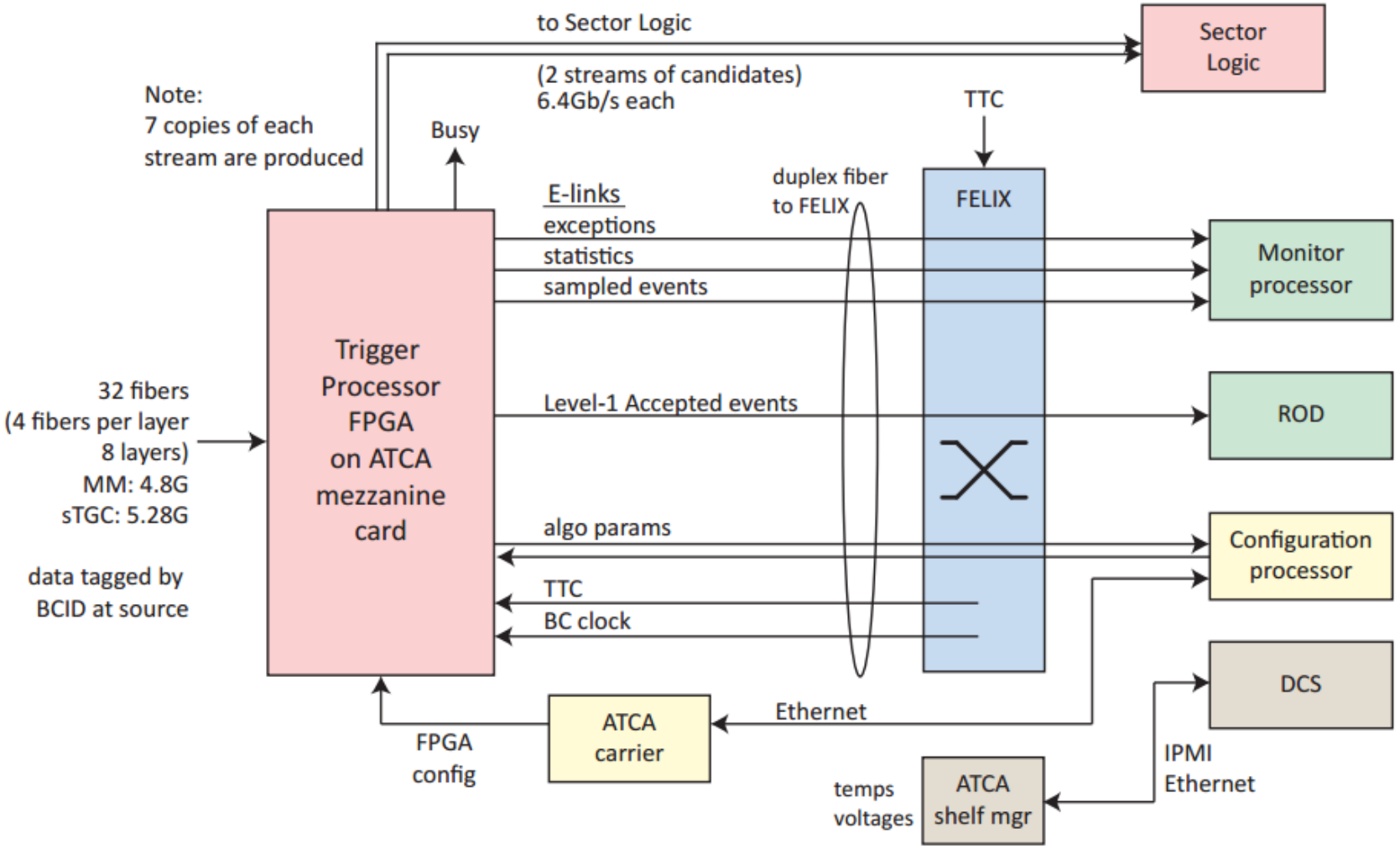
- Calc RoI
  - Mx Global
  - Mu Global
  - Mv Global
- Calc Δθ
  - Mx Global
  - Mx Local

5 Clks

Latency = 19 clks (320 MHz)=2.375 BC

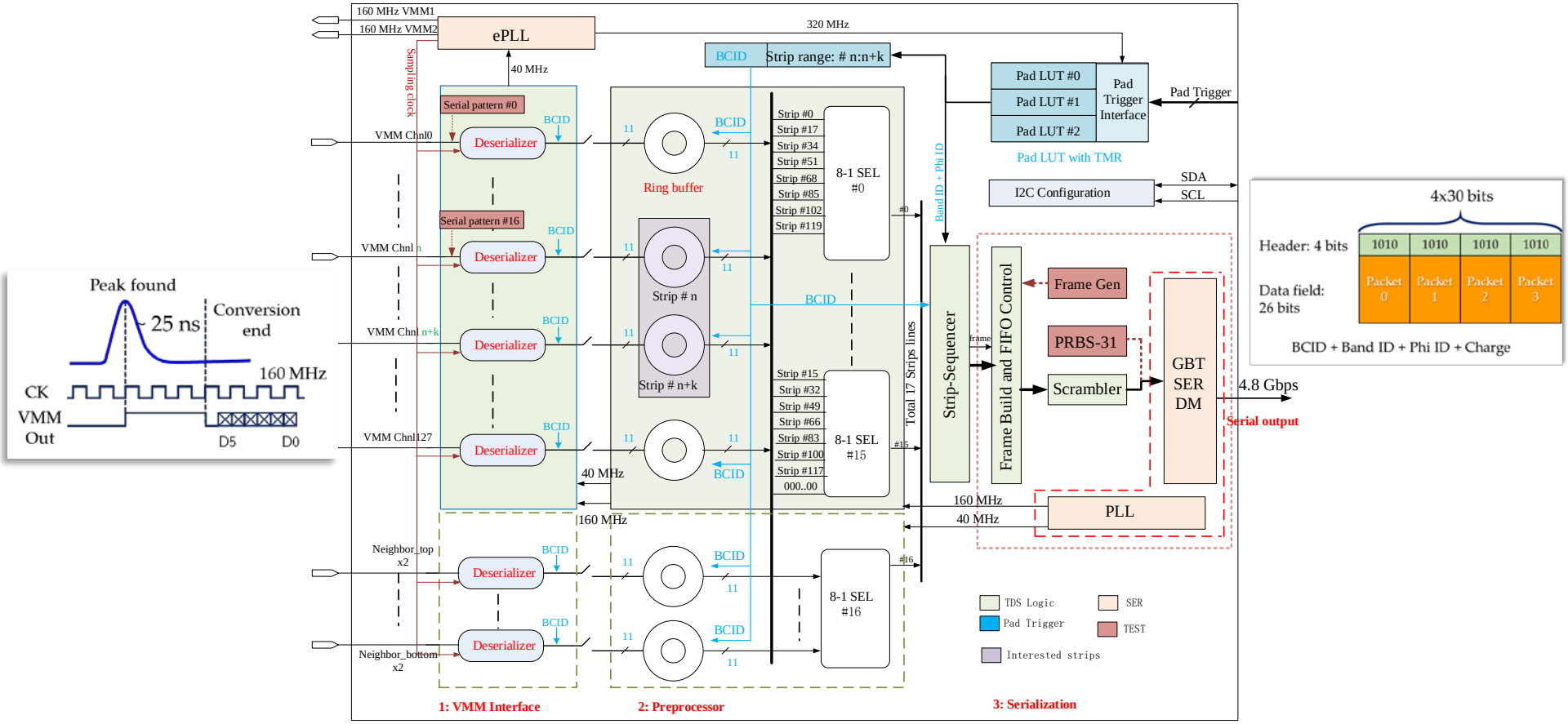
Spares

Trigger Processor context diagram



Spares

Strip-TDS block diagram



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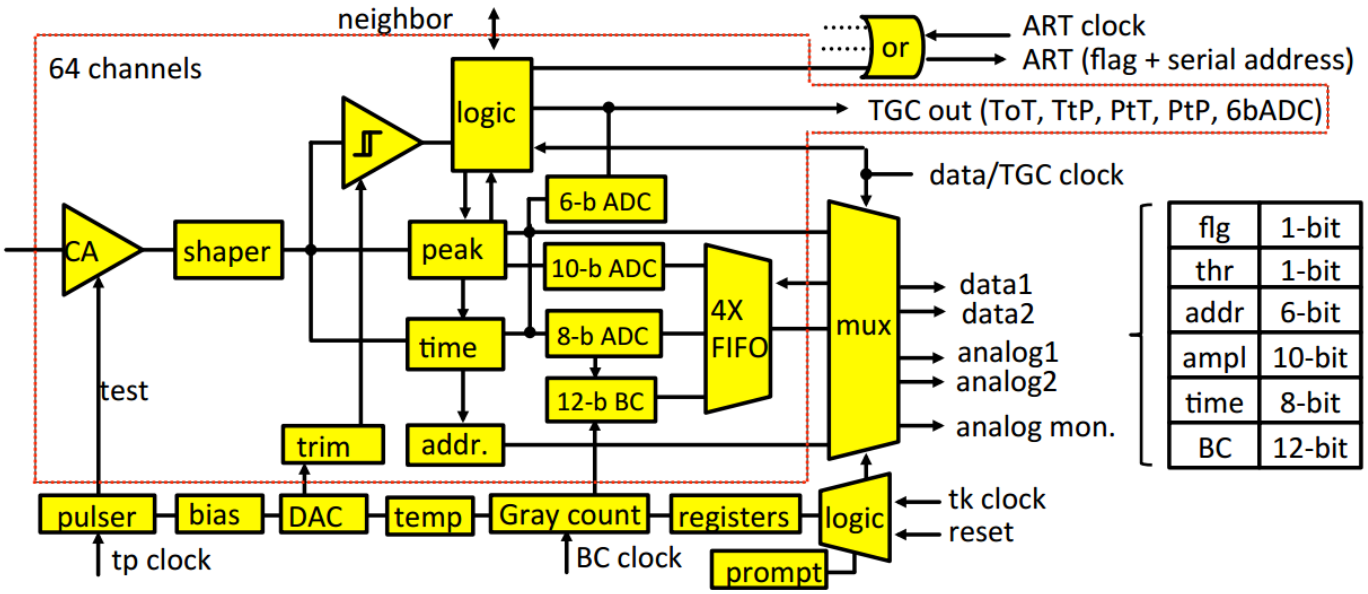
VMM2 Block diagram



6-bit ADC readout timing diagram