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Trigger Algorithms and electronics for the ATLAS Muon NSW Upgrade

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The ATLAS New Small Wheel (NSW), comprising MicroMegas (MMs) and small-strip Thin Gap Chambers (sTGCs), will upgrade the ATLAS muon system for a high background environment. Particularly, the NSW trigger will reduce the rate of fake triggers coming from background tracks in the endcap. We will present an overview of the NSW trigger processor, the sTGC and MM trigger algorithms, and the hardware implementation - an ATCA system with FPGA-based trigger processors. Finally, we will detail the challenges of meeting the low latency requirements of the trigger system and coping with the high background rates of the HL-LHC.

Summary

The ATLAS NSW, made up of MicroMegas (MMs) and small-strip Thin Gap Chambers (sTGCs), is an upgrade to the Small Wheel of the ATLAS endcap muon system (the endcap section closest to the interaction point) that will greatly improve the performance of the muon system in the high background rate environment of the high-luminosity LHC.. The NSW trigger system, in particular, will improve the rejection of fake tracks not originating from the interaction point (often caused by protons generated in the material between the Small Wheel and Big Wheel, the next layer of the muon endcap system). The ultimate goal for the NSW trigger system is to provide track segment candidates to the ATLAS Sector Logic (SL) system, where these candidates will be corroborated with candidates provided by the TGCs in the Big Wheel.

The trigger processors (TPs) are the heart of the NSW trigger system. The MM and sTGC detectors will have separate FPGAs that reside on mezzanine cards in an ATCA hardware platform but implement distinct trigger algorithms unique to their respective detector geometries. The hardware platform must also facilitate fast communication between the MM and sTGC algorithms, as only one combined track candidate can be sent to the SL to be combined with Big Wheel data. Hit data is transmitted from the detector front end readout to the trigger processors via optical fibers by dedicated electronics. The total latency allotted for the full NSW trigger processing chain is 43 LHC bunch crossings (1075 ns). This constraint requires minimizing latency at every step in the transmission and processing chain.

In this talk, we will present an overview of the NSW trigger system and the associated electronics, including the full data path from detector to trigger processor and finally to the sector logic. we will detail the MM and sTGC trigger algorithms and how they are used to effectively eliminate the non-collision background that is present. Finally, we will show the plans for the hardware implementation of the trigger processing chain, focusing on the implementation of the trigger algorithms in FPGAs. We will present preliminary results on tests of the of these implementations, including some of the techniques used to ensure that each step meets its latency requirement.

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