Karlsruhe Institute of Technology

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A Signal Distribution Board for the Timing and Fast Control Master of the CBM Experiment

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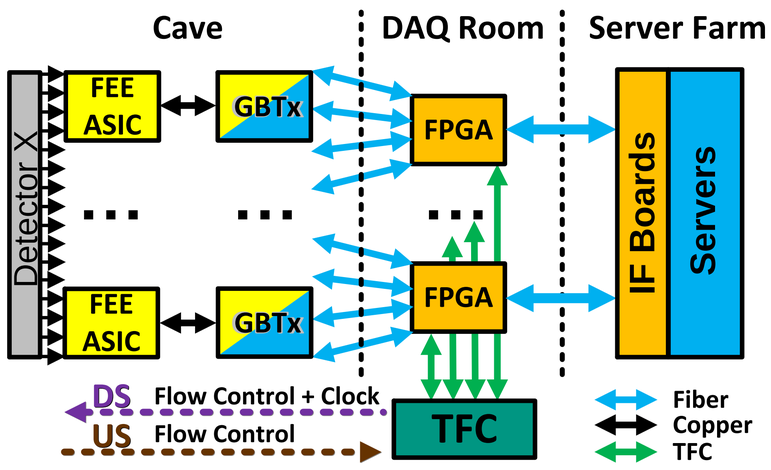
1. The Detector Readout Chain in the CBM Experiment



CBM Readout Chain Block Diagram

Properties:

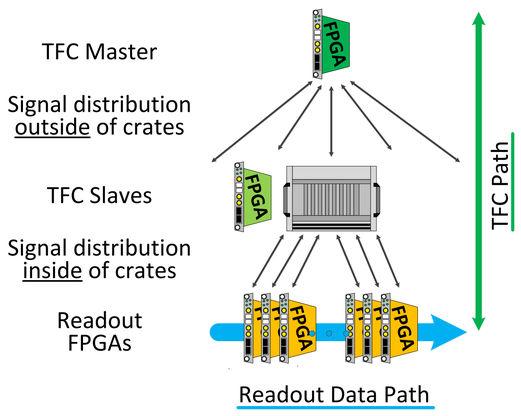
- Distributed Readout Chain with crated FPGA Boards in DAQ Room
- DAQ FPGAs operate GBTx Links
- Frontend Electronics uses Clock derived from GBTx Link as Sampling Clock

Required:

- Phase-locked, High-Quality Clock
- Global Timing Synchronization
- Short, Constant Latency Links to a Central Flow Control System

These Tasks are addressed by the **Timing and Fast-Control System (TFC)**

2. Topology of the TFC System



TFC System Topology

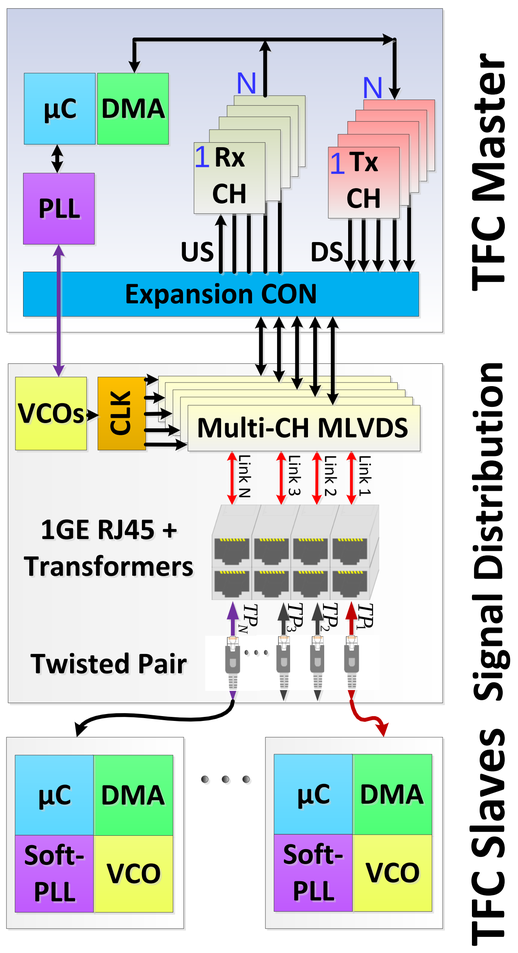
Two-stage TFC System: The Synchronization of hundreds of DAQ FPGA Boards becomes manageable by introducing a middle layer of TFC Slaves.

- Synchronization
  - **Within Crates**
    → Crate Infrastructure
  - **Outside of Crates**
    → Custom Interconnection Concept (~30m maximum distance)

Interfacing Concept Outside of Crates:

- **1:N Master-Slave Network** using **Twisted-pair (TP) Links**

The Concept requires the Design of **TFC Master Interfacing Boards**



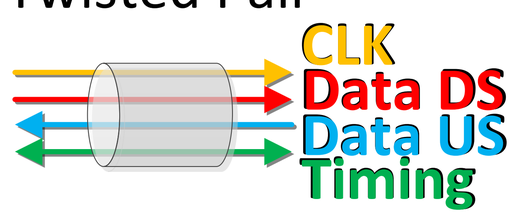
Signal Distribution outside of Crates using Custom IF PCBs

3. TFC Interface using Twisted-pair Cabling

In order to provide a high-quality clock, low, constant latency links, mitigate delay skew issues etc., a **special purpose** is assigned to **each of the four differential pairs** per cable.

- One dedicated **High-Quality Clock** Pair
- **Data Downstream/Upstream** Pairs for Payload Data or **Fast-Control** Transfers
- One **Bidirectional Timing Link** Pair for Node Synchronization

⇒ **Timing Link:** Cable Skew does not contribute to Link Asymmetry



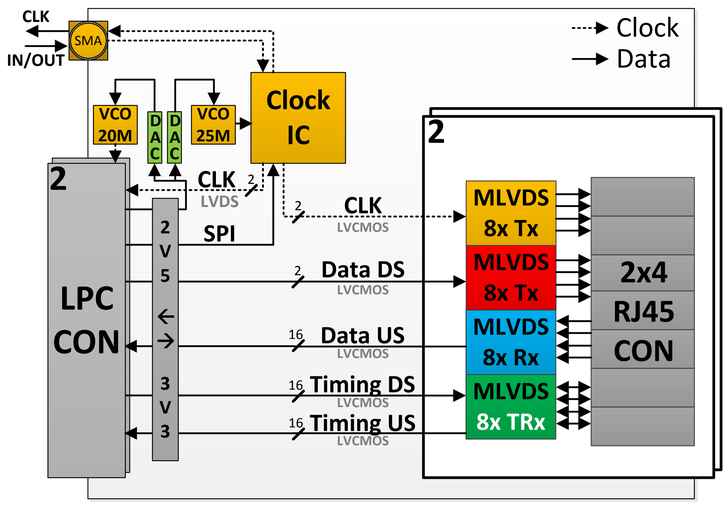
Assignment of Pairs in TP Cable

4. Schematic View and Features of the Prototype Board

General Structure:

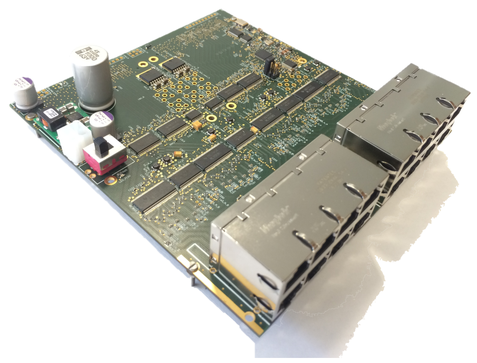
- N Master-Slave Links
  - **1 Gigabit Ethernet** (1GE) **Connectors** with isolation transformers
  - **MLVDS** Buffers & Transceivers
  - ⇒ Larger Swing, less prone to Common-Mode Offsets
- Master Interface: **FMC Connectors**

- **Voltage Controlled Crystal Oscillators** (VCXO)
  - 25MHz VCXO drives Clock IC
  - ⇒ Flexible TFC Master and Link Clocks
  - 20MHz VCXO as Offset Clock
  - ⇒ Digital Dual-Mixer Time Difference (DDMTD) Measurements



Schematic View of TFC Master Interfacing Board for N=16 Links

5. TFC Master Signal Distribution Board Prototype and initial Tests



Pick&Placed Full-Featured first Prototype Board with 16 Links

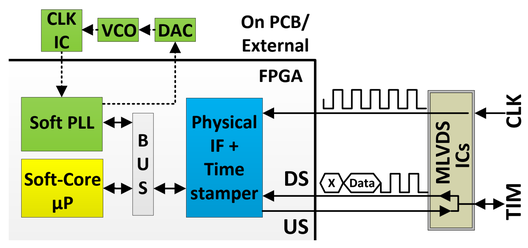
Status of Prototype Testing

- **Fully Functional Clocking**, adjustable for Rapid Prototyping ✓
- **Clock/Data links over TP**, using MLVDS TRx and 1GE Connectors ✓
- **Master Loopback Tests** show **Error-free Transmission**: ✓
  - 30 Meter Cable
  - 10 Minutes Test Duration
  - DC-free Data Patterns
  - 1x 120MHz Clock, 2x 200Mbit/s Data links in opposite directions

6. Envisioned Processing System & Synchronization Procedure

General Processing System:

- Soft-Core Microprocessor and DMA for constant latency transmissions
- Time stamping and Soft-PLL based on approaches used in White Rabbit nodes
- PLL listens to two reference inputs:
  - TP clock for frequency locking
  - TP bidirectional link for phase locking



Synchronization System with separate Clock and Data signals

7. Summary & Outlook

Contributions:

- Twisted-Pair based TFC Master Interface
- **Deterministic Latency Links** through MLVDS-Transceivers known from Telcom.-Crate Backplane Communication
- **Flexible, White Rabbit-based Clocking**
  → Soft-PLL and precise time stamping

Future Work:

- Design of **TFC Slave Interface Boards**
- **Frequency and Phase locking Algorithms** based on White-Rabbit approach
- **TFC Master/Slave Node Integration**
- **Fast Control Message** and/or **Trigger Distribution System**