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A Signal Distribution Board for the Timing and Fast Control Master of the CBM Experiment

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For the CBM experiment a Timing and Fast-Control (TFC) system is being developed. In the detector readout, FPGA-based data processing boards (DPB) are organized in a large number of computing crates. At the crate level, the TFC master is connected to one TFC slave per crate, whereas the DPB AMCs are interconnected by the crates' infrastructure. In this article, an FMC-based signal distribution board is proposed allowing the transmission of a high-quality clock and timing and fast-control data from and to connected TFC slaves at distances of about 30 meters using twisted-pair cables.

Summary

The CBM detector readout system currently being developed is based on self-triggered frontend electronics which is connected to preprocessing DPBs through the rad-hard GBTx ASICs. In this structure, it is important to provide a high quality, frequency locked clock to the DPBs, operating the optical downstream GBTx links from which the frontend derives the system clock, and enable timing synchronization. Additionally, means have to be provided to pass messages with low, constant latency from the frontend or DPBs to a central control system.

The TFC system, being associated with these tasks, is integrated into the DPB layer consisting of a large number of mTCA.4 crates equipped with DPB AMCs. Following this structure, the TFC system synchronizes on the level of crates but also the DPBs inside the crates itself.

For the link external to crates, a signal distribution board was designed which is capable of providing a high quality clock and data channels for timing synchronization and fast-control message transmission to a multitude of TFC slaves being the TFC controllers of individual crates.

The proposed board provides an interface for connecting the TFC master FPGA, requiring normal I/Os only, to the one-to-N signal distribution network (first revision: N=16), where the TFC slave AMCs are interfaced through RTM boards.

Twisted-pair data center cables are used for the TFC link, offering a reduced delay skew between the four differential pairs of one cable (˜4ns typical per 100m) compared to standard Ethernet cables.

For the transmission of TFC signals over distances of about 30 meters inside the facility's control room, multipoint low voltage differential signaling (M-LVDS) transceivers were selected, which offer an enhanced differential swing and allow half-duplex transmission over a shared line. The M-LVDS multi-channel transceivers are interfaced on the PCB to the twisted-pair cables using Gigabit Ethernet connectors with integrated isolation transformers.

Here, one differential pair is assigned for transmitting a high quality clock (frequency locking of slaves' oscillators). Pairs two and three provide means to exchange fast control information between master and slaves. The timing synchronization of the slaves to the master is performed using the single remaining differential pair in bidirectional half-duplex mode thus removing the influence of the cables' delay skew from the timing link's asymmetry calculation.

Besides the components for physical level transmission, the board offers a highly flexible IC for generating the clock signals to be transmitted over the M-LVDS clock channels and a tunable 20 MHz oscillator. The TFC master FPGA is interfaced through two FMC connectors which also one of the generated clocks and the oscil-

lator's signal is connected to. Hereby, a time-stamping procedure is supported being similar to the approach applied in White Rabbit nodes.
In summary, the proposed board provides means to use a general purpose FPGA board as a high-fanout TFC master to synchronize a distributed network of slaves at medium distances, offering a versatile clocking for precise time-stamping.

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