PACIFIC: The readout ASIC for the SciFi Tracker planned for the upgrade of the LHCb detector

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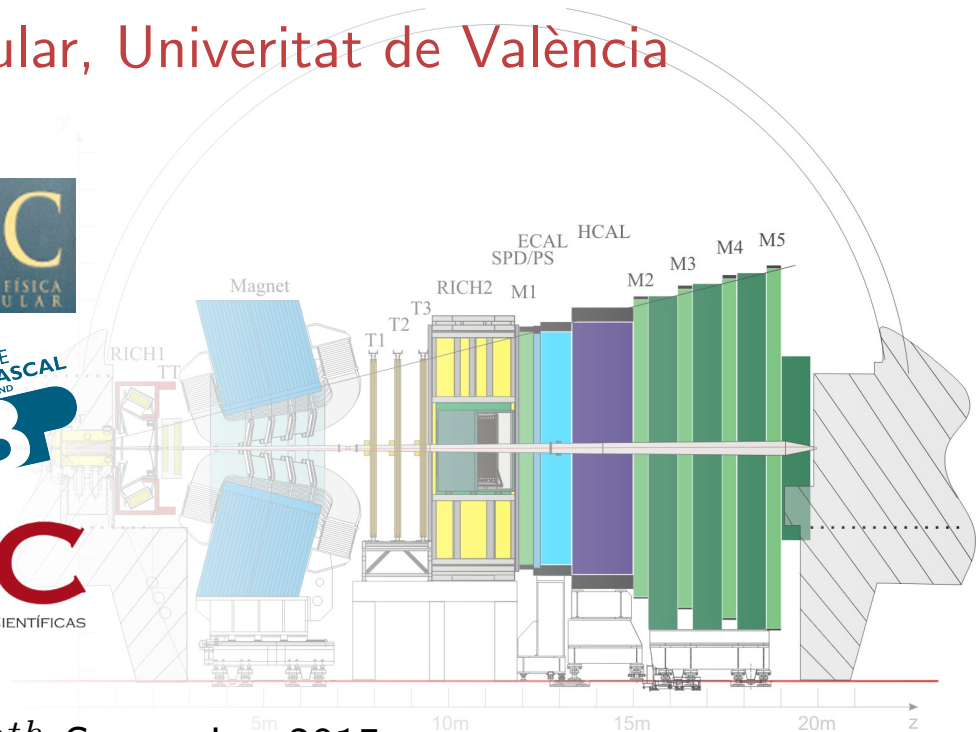
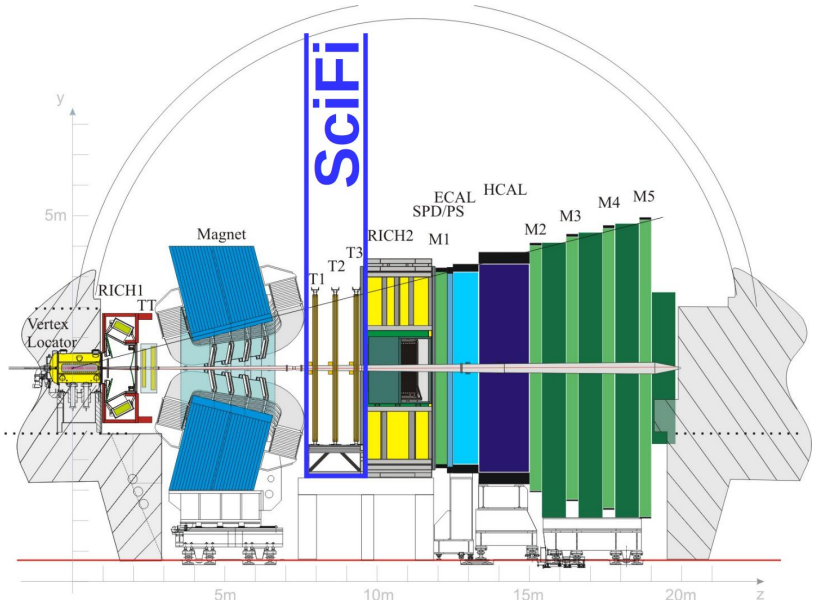


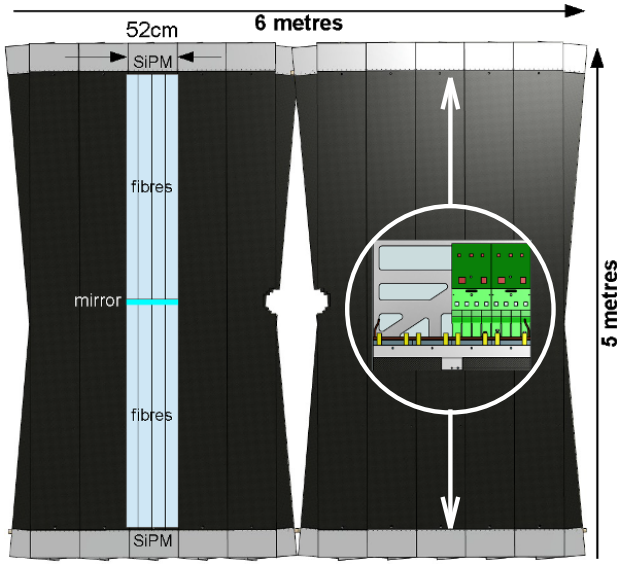
TWEPP - Lisbon - 30^{th} September 2015

Outline

LHCb

- Physics measurements limited by 1 MHz hardware trigger.
- Upgrade: increased luminosity, 40 MHz trigger at FE electronics.
- New detector proposed for T1-T3 the Scintillating Fibre Tracker.

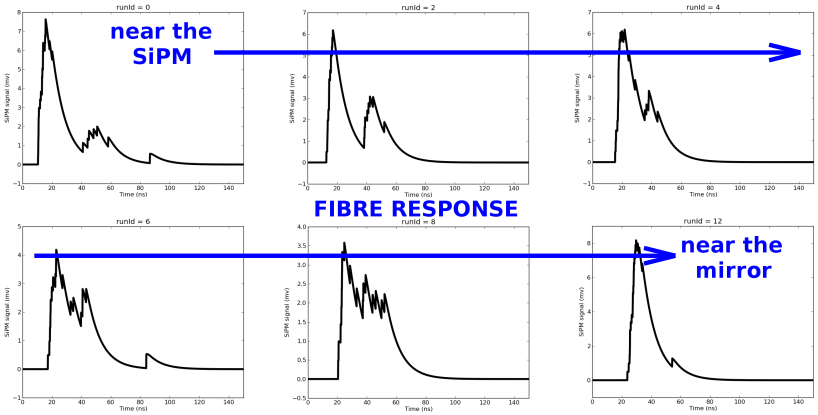


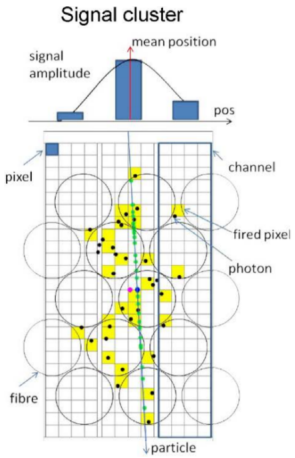


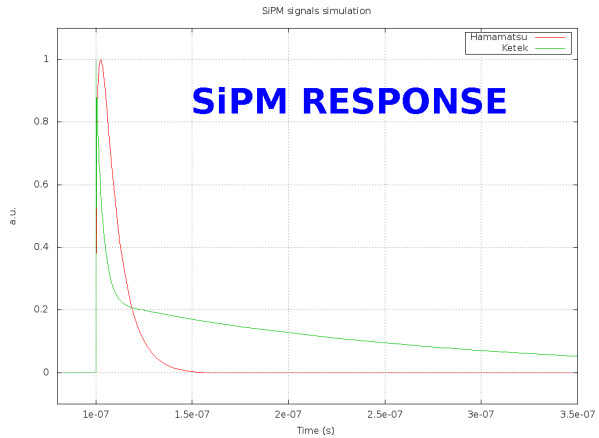
- 3 stations x 4 planes (x-u-v-x).
- 12 modules per plane.
- 6 layer fibre mats (mirrored).
- 8x2.5 m long mats per module.
- 2 ROB at top and bottom with 16 SiPMs and FE electronics.

SciFi

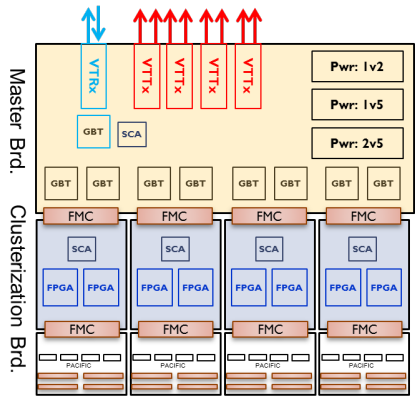
- ⌀250 µm scintillating fibres with 128 channel SiPM array.
- Fibre signal shape and arrival time depend on hit position.
- Multiple SiPM channels triggered ⇒ post-process needed.
- SiPM signal has a long tail ⇒ shaping required.







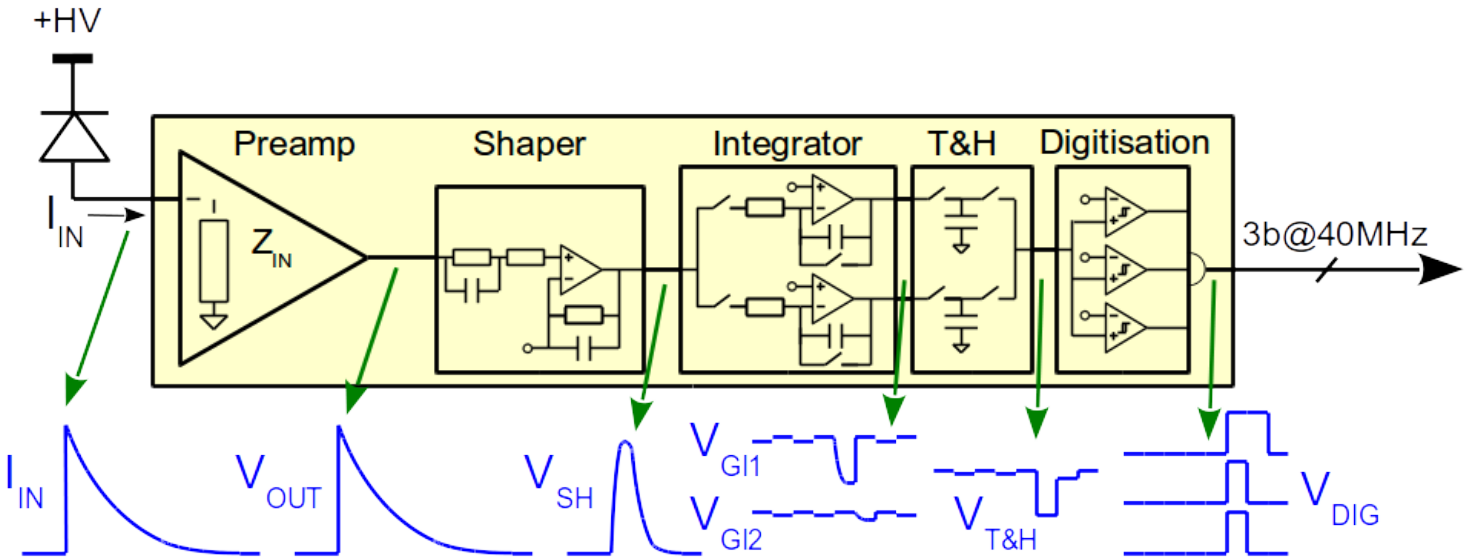
- Front-end electronics with modular design.
  (further discussed in parallel talk by H. Chanal)
  - PACIFIC provides non-linear digital readout.
  - Clusterization algorithm reduces throughput.
  - Master board: communications and power.



Specifications

- CMOS 130 nm process, migrating from IBM to TSMC.
- **64 channel** readout matching SiPM die granularity.
- Input voltage adjustable on a channel basis.
- Low input impedance for **direct anode connection**.
- Single photoelectron detection capability.
- SiPM tail cancelation to **minimize spillover**.
- Interleaved integrator system to **avoid dead time**.
- Configurable non-linear digital output delivered at 40 MHz.
- Power consumption below 500 mW $\Rightarrow$ **8mW/channel**.
- Supply voltage of 1.2 V in the core and 1.5 V in the pad ring.

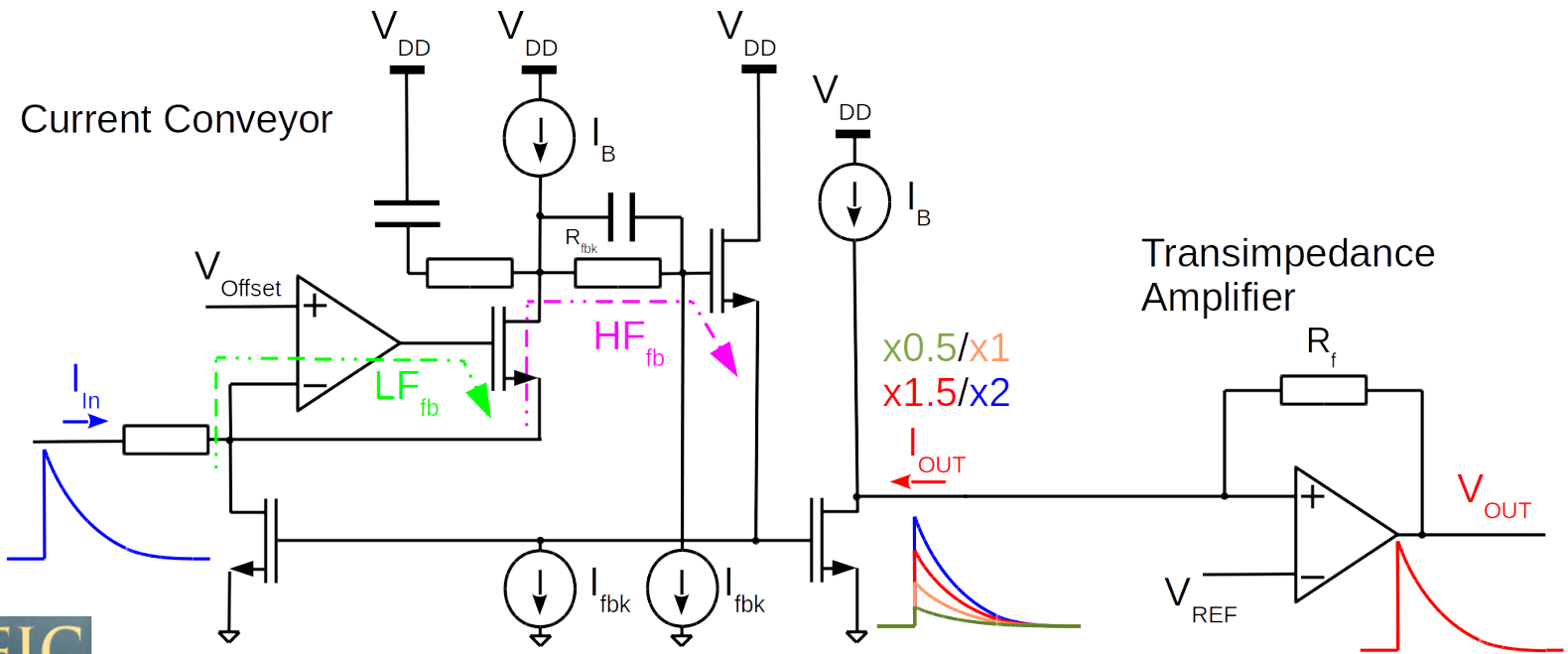
Processing Chain



- Preamp: current input with voltage control and gain selection.
- Shaper: fast double pole-zero cancellation, both adjustable.
- Integrator: dual gated scheme maximizing charge collection.
- Digitizer: non-linear flash ADC with configurable thresholds.
- Output encoded in 2 b and two channels serialized at 160 MHz.
- Additionally, common bias references and I^2C slow control.

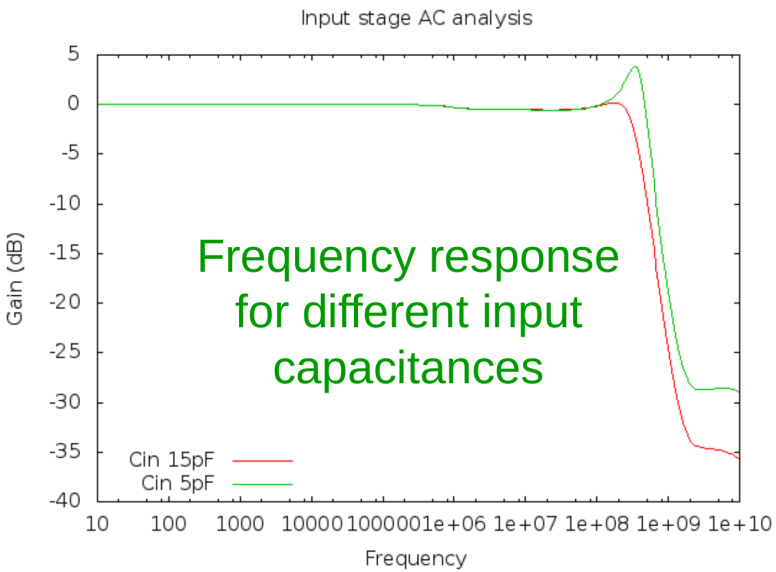
Preamplifier

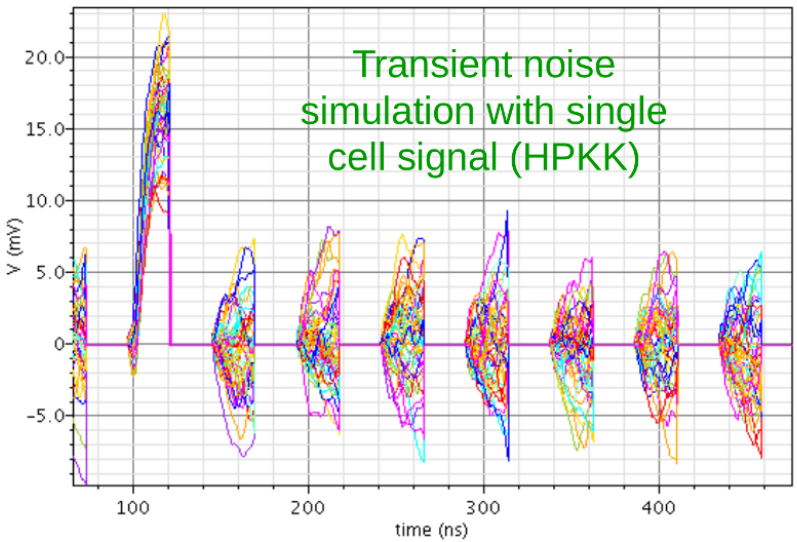
- Current conveyor:
  - HF_{fb} keeps input impedance constant.
  - LF_{fb} controls input DC voltage.
  - Output mirror with 4 selectable gains.
- Transimpedance amplifier:
  - Current to voltage signal conversion.
  - Control conveyor output voltage.



Preamplifier

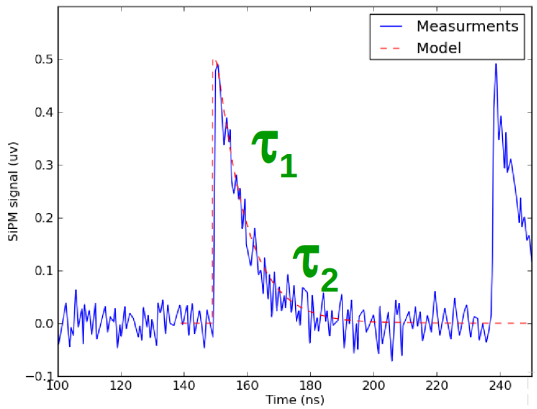
- High bandwidth (250 MHz).
- Low input impedance ($< 50\,\Omega$).
- Input DC voltage control (700 mV range).
- Single photoelectron resolution.
- Wide dynamic range (5 mA low gain).
- Low power consumption (< 2 mW).

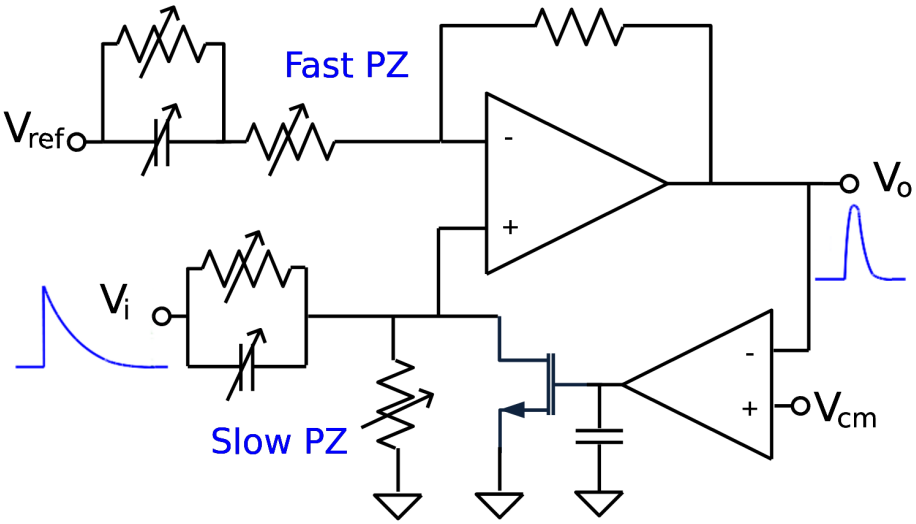




Shaper

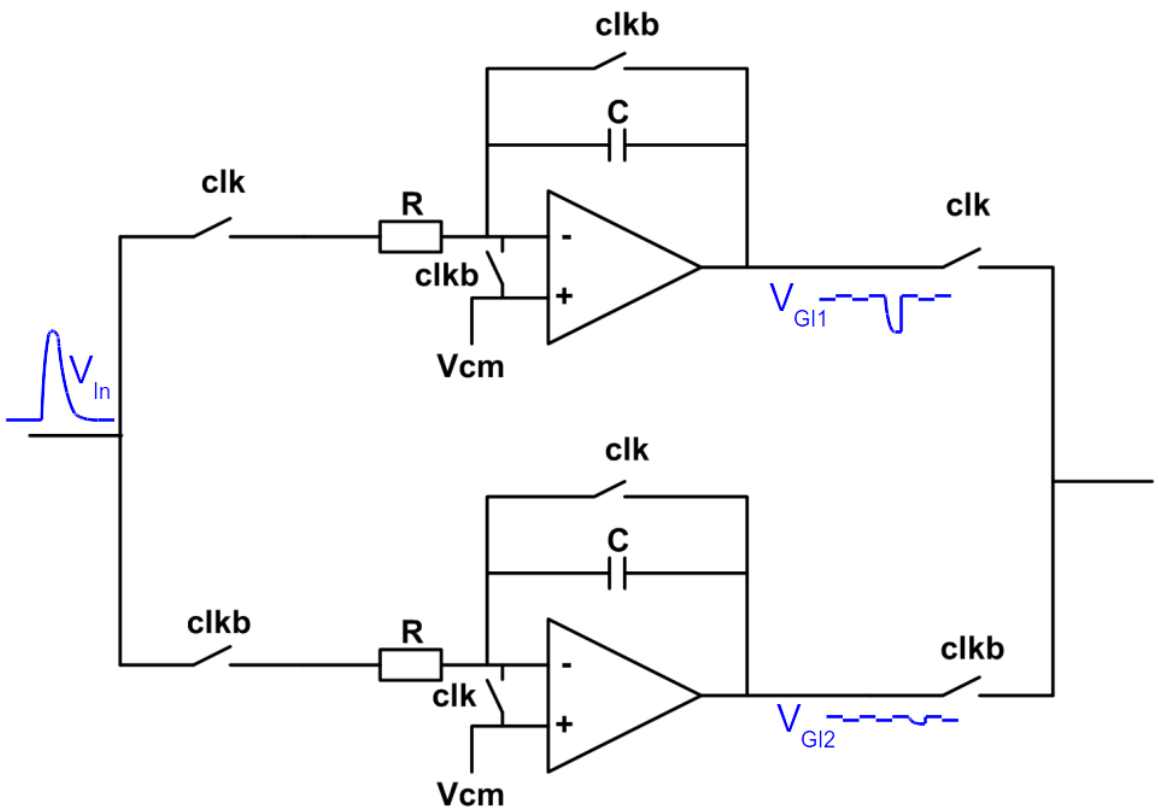
- PZ cancellation: pole cuts signal tail, zero removes undershoot.
- SiPM signal tail can be modeled as a double exponential, the main goal is to cancel slower time constant (10 ns shaping).
- OTA based closed loop shaper with configurable poles and zeros.
  - First PZ cancels τ_2 (SiPM capacitance and quenching resistor).
  - Second PZ cancels τ_1 (trace parasitics and input impedance).
- A DC feedback loop controls the quiescent output voltage (critical for integration).





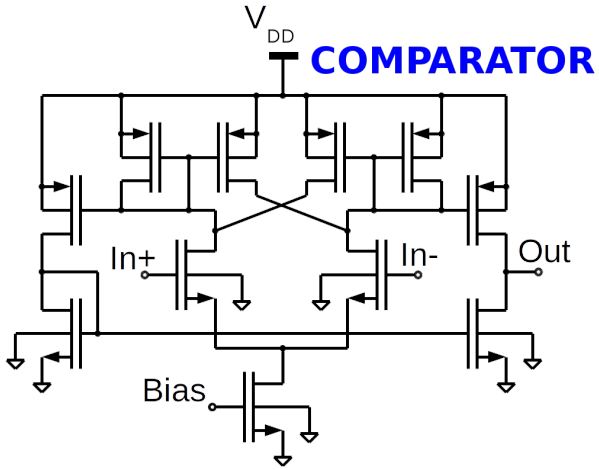
Integrator

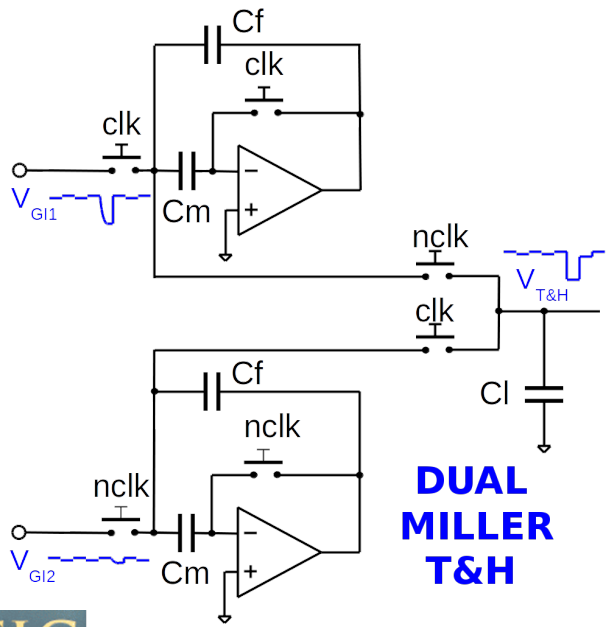
- Classic integrator architecture.
- Two interleaved gated integratorsto avoid dead times.
- Synchronization with digitizer required.
- Based on classic Miller OTA.

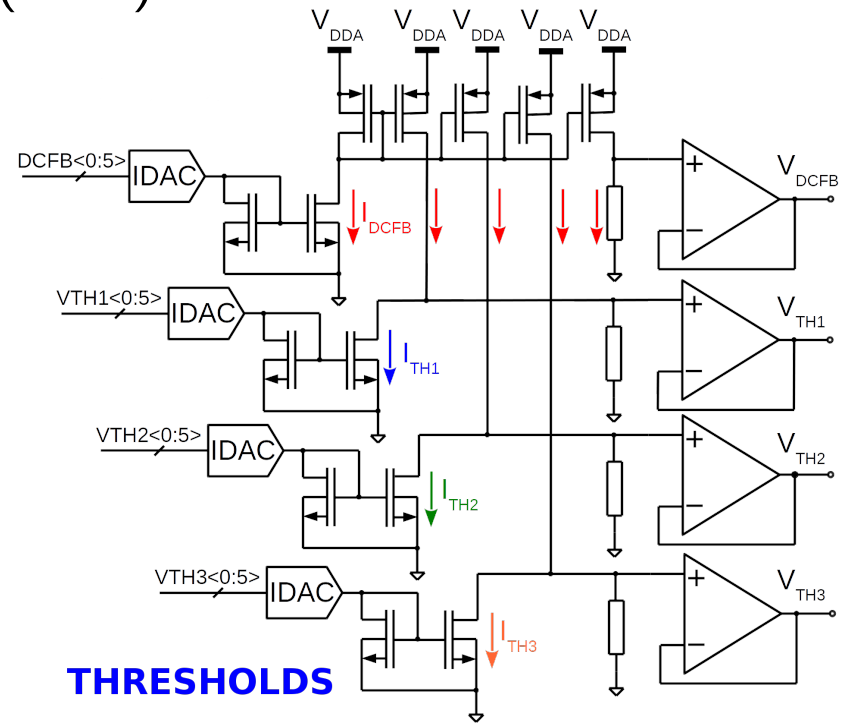


Digitizer

- Dual Miller track and hold merges the two subchannels.
- Comparator with 10 mV hysteresis and 20 mV to 850 mV dynamic range.
- Thresholds derived from DC reference, 6 b (7 b) resolution for TH2/3 (TH1).

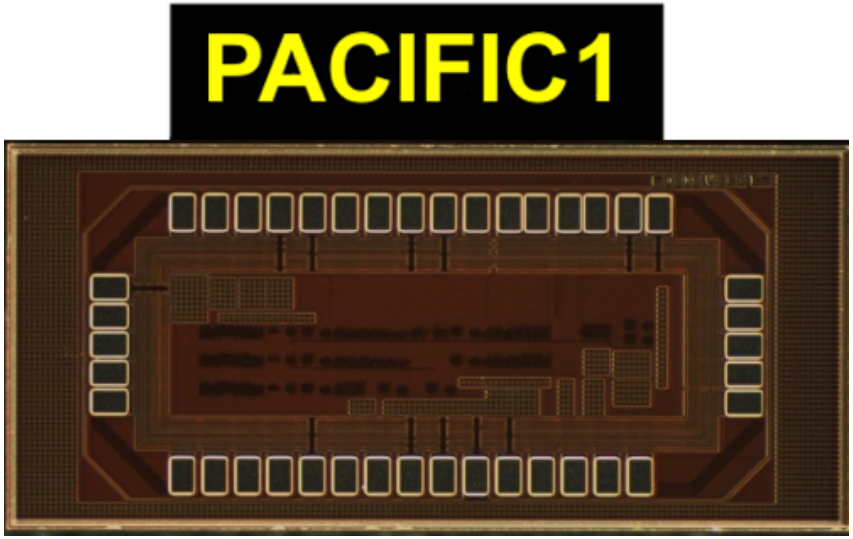


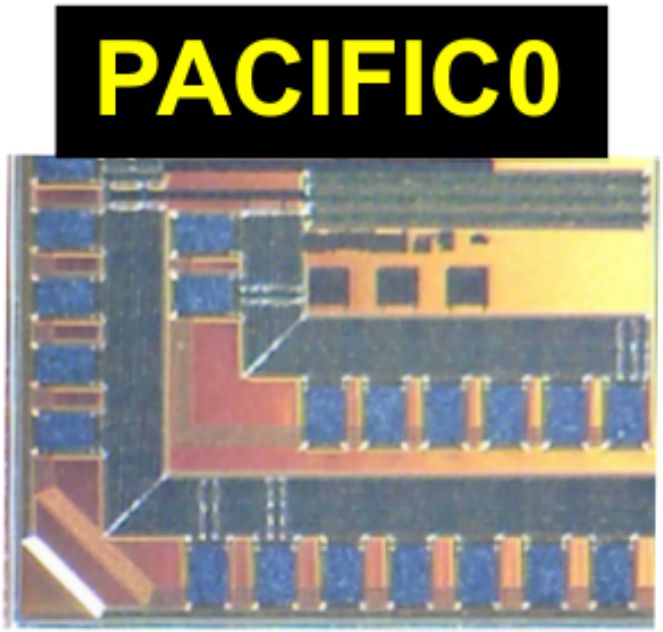




PACIFICr0 and PACIFICr1

- PACIFICr0:
  - May 2013.
  - IBM 130 nm.
  - Fix gain current conveyor.
  - Migrated from AMS 350 nm BiCMOS.

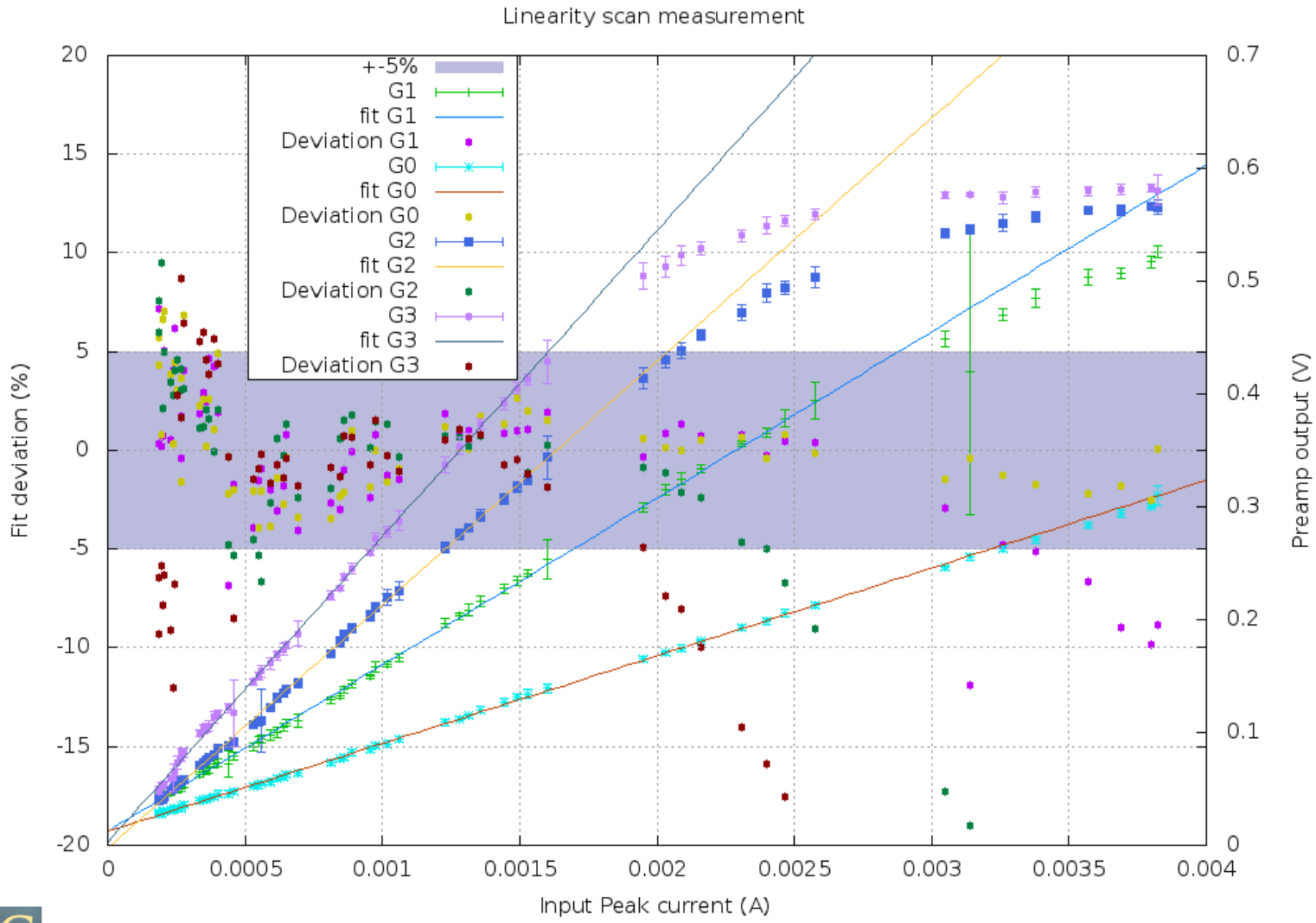




- PACIFICr1:
  - November 2013.
  - IBM 130 nm.
  - Full analog FE plus test blocks
  - Analog external bias
  - Independent GI output.

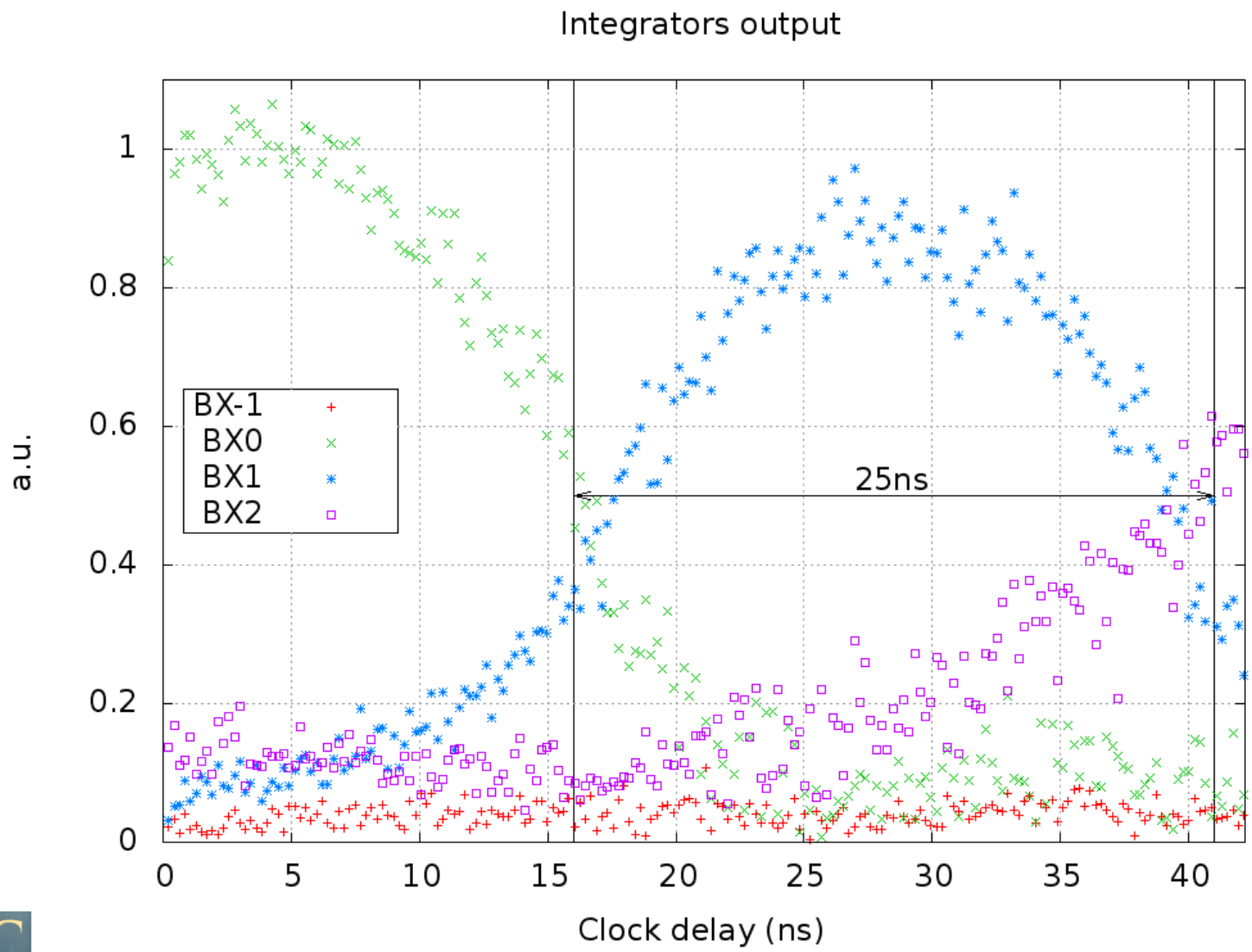
PACIFICr1 Results

- Good Preamplifier linearity over full designed dynamic range.



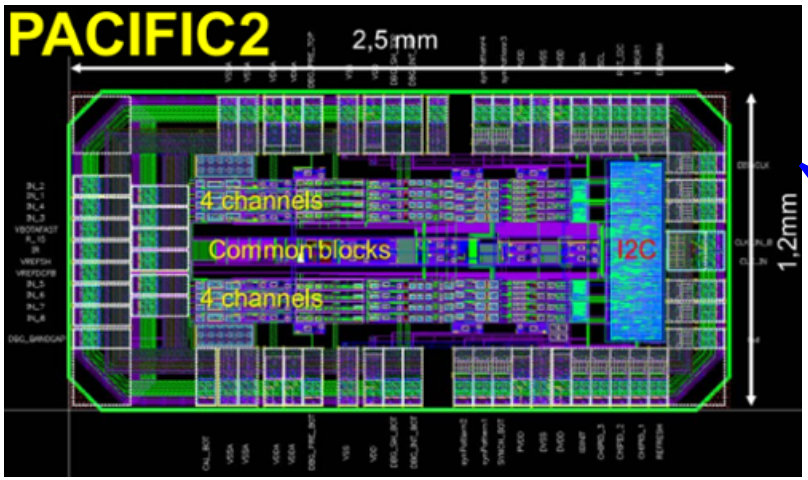
PACIFICr1 Results

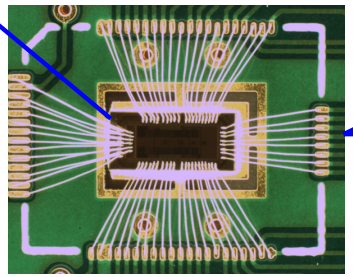
- Integrator output time alignment for 10 PE, pulse fits clock period.

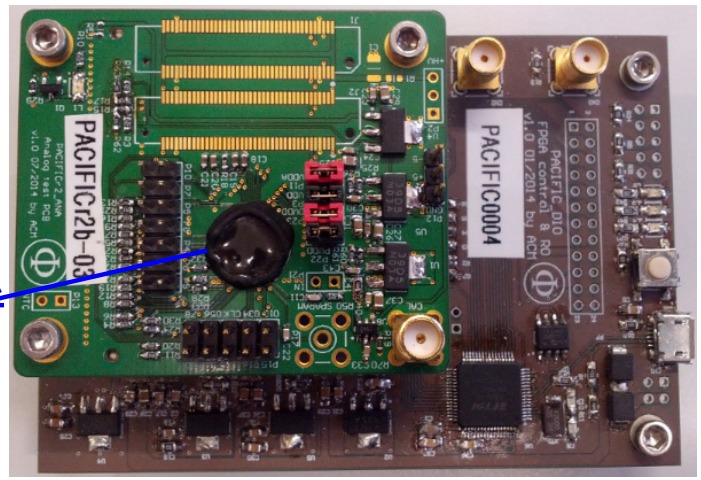


PACIFICr2

- Eight fully functional channels with digital output.
- Block debug analog outputs selectable on channel basis (Preamplifier, Shaper and Track & Hold).
- Integrated common bias references and clock distribution.
- Configuration through I2C slave and registers.
- Lower threshold with 6 b resolution but half dynamic range.
- Three units mounted on test setup similar to PACIFICr1.

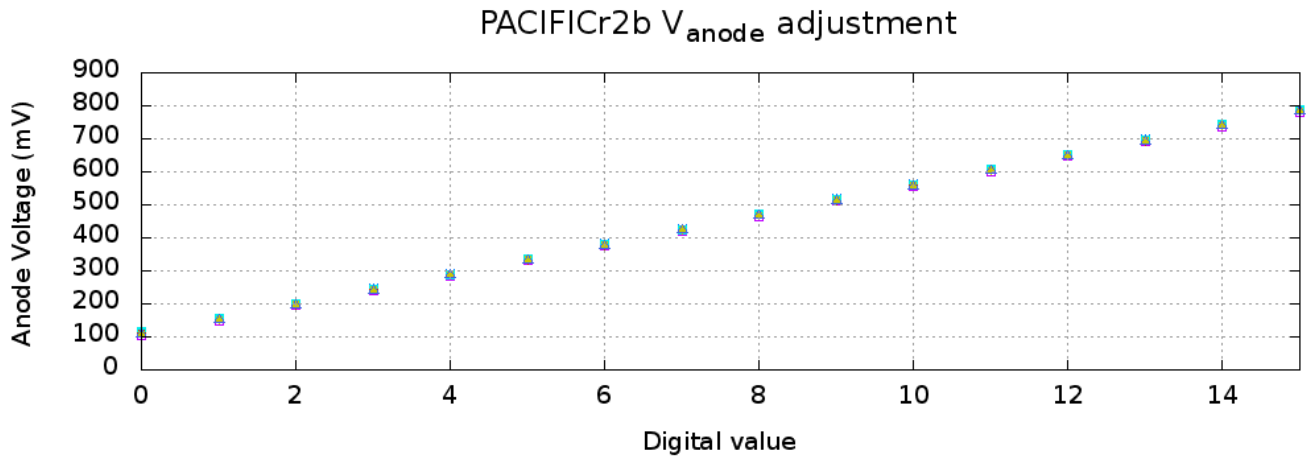


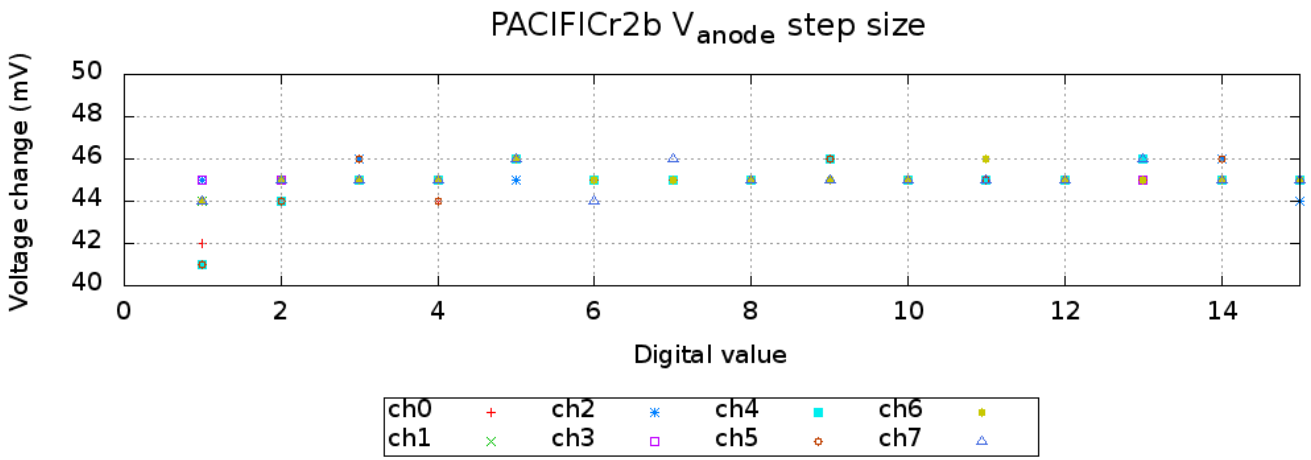




PACIFICr2: Power and Bias

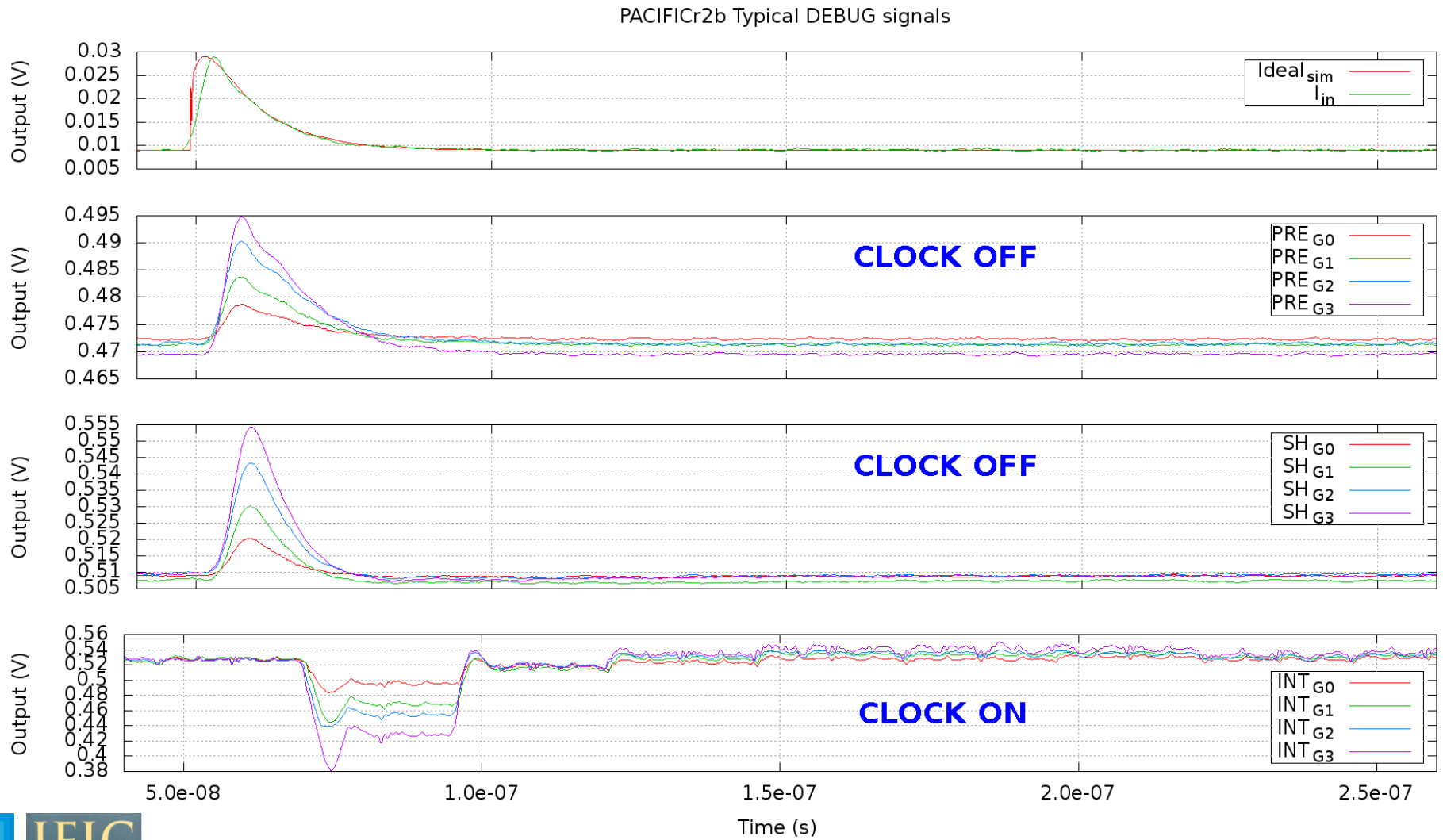
- Power consumption **6.42 mW/ch**, within specifications.
- Bias voltage slightly low due to bandgap inaccuracy.
- Fairly linear input voltage control, step fits simulations.





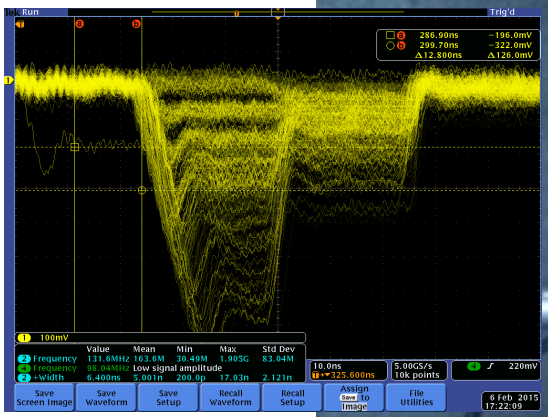
PACIFICr2: Analog Signals

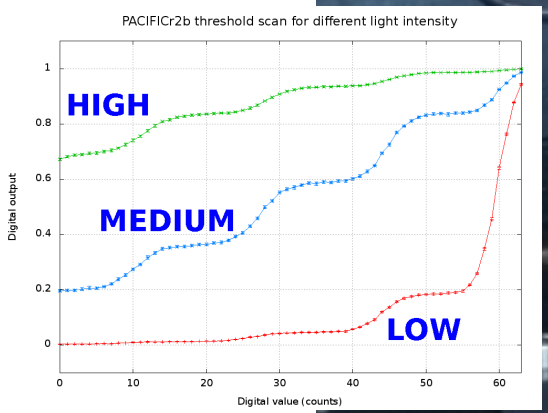
- Debug outputs response to modeled SiPM signal (avg 32).

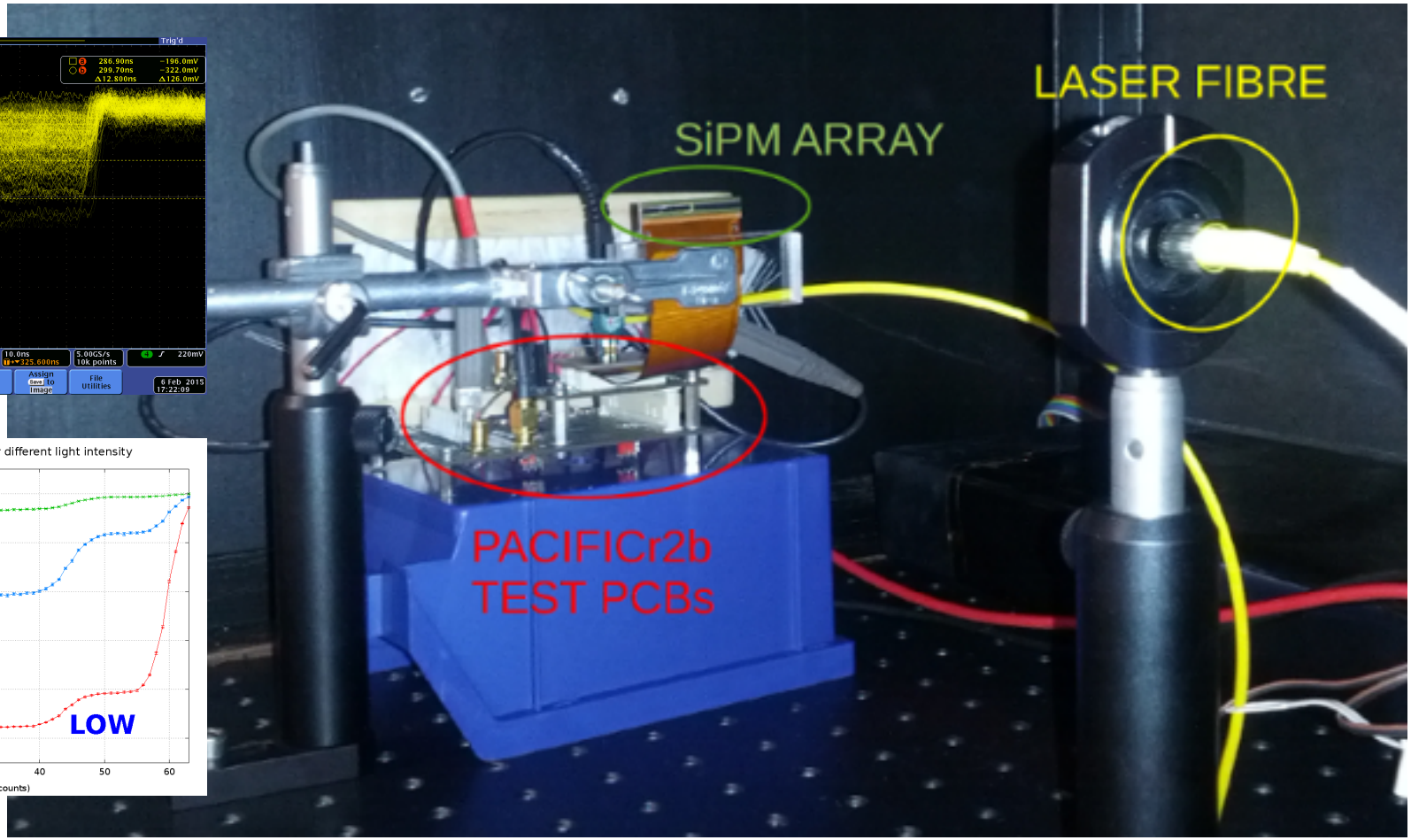


PACIFICr2: Light Injection

- Readout of 2014 Hamamatsu sensor synchronized with light source.
- Blue picosecond diode laser pulsed directly on the SiPM channel.
- Shaper designed for previous version, thus spillover and undershoot.

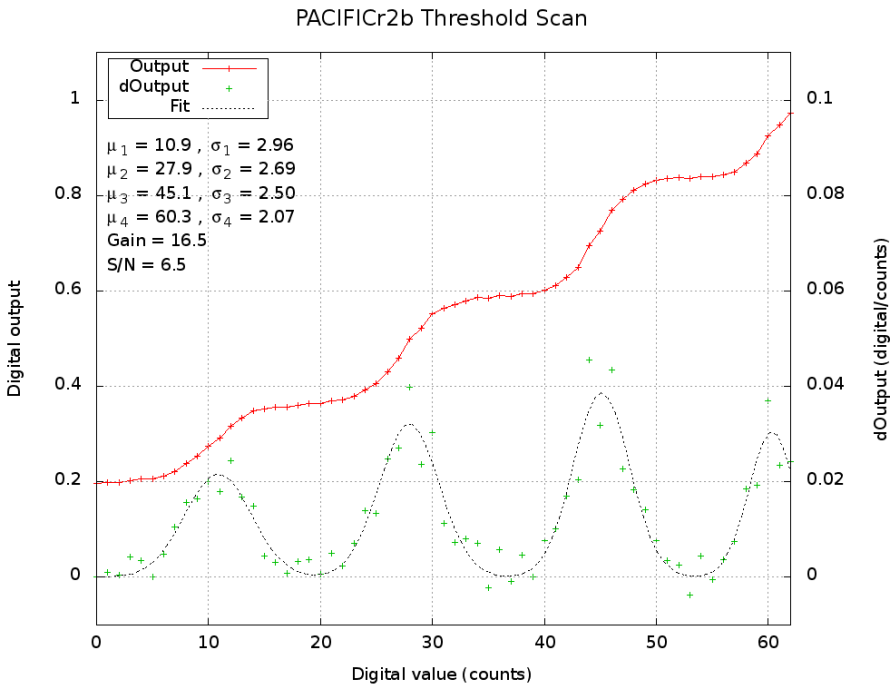






PACIFICr2: Sensor Gain

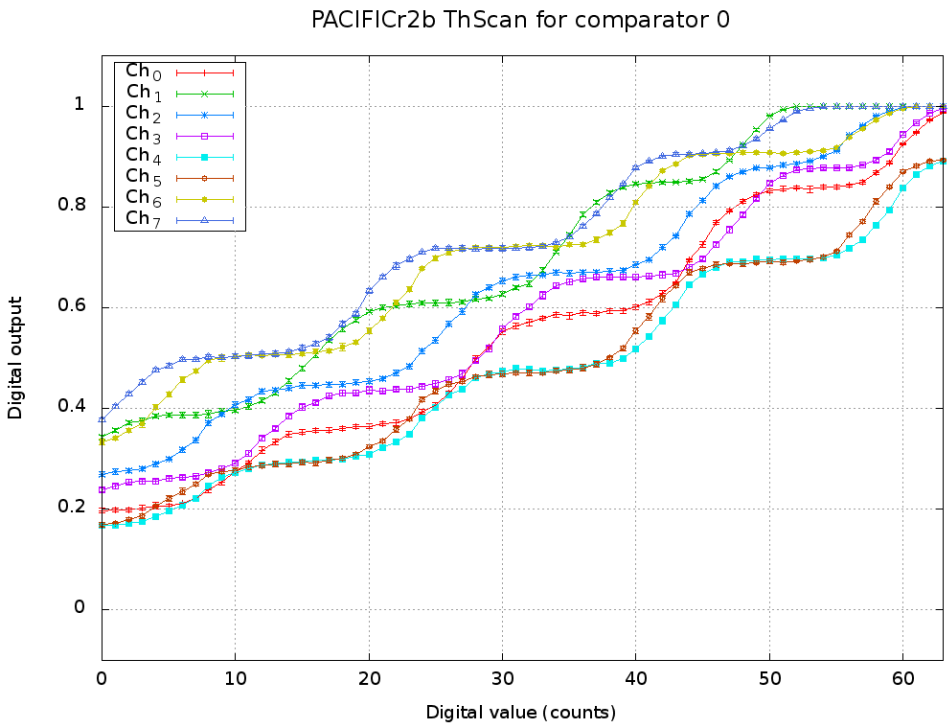
- Individual photons are observable in threshold scan.
- Scan derivative provides measurement of sensor gain (gap between peaks).
- Full chip evaluated at different overvoltage, PACIFICr2 slightly increases 10 % gain variation intrinsic to the sensor.

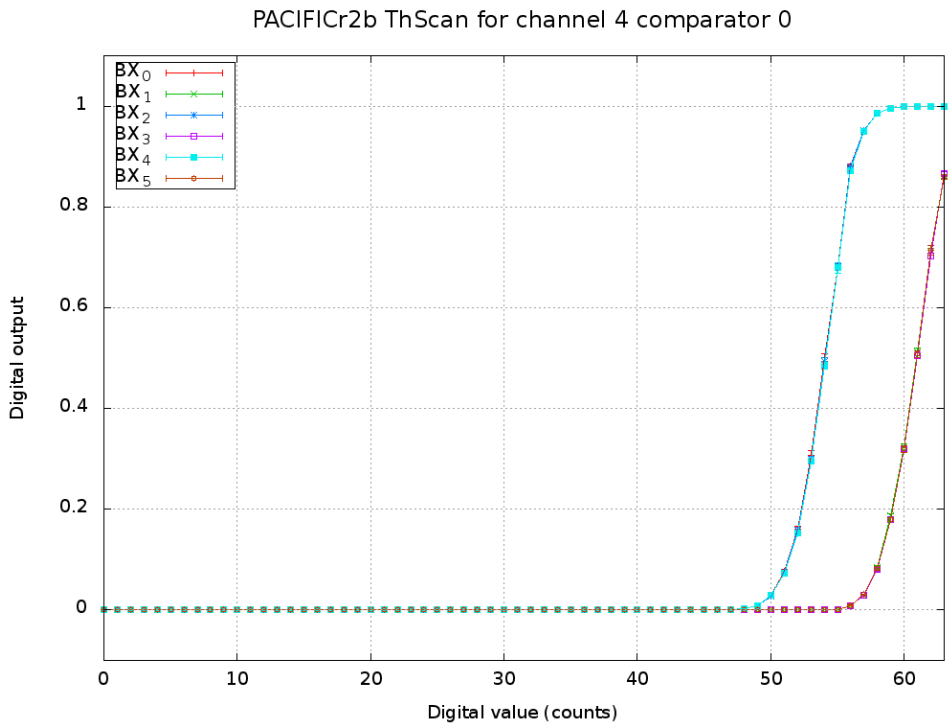


	@3V OverVoltage		@3V5 OverVoltage	
Ch	**Gain**	**Variation %**	**Gain**	**Variation %**
0	16.5	0.2	18.9	-1.8
1	15.6	-5.3	19.2	-0.2
2	16.1	-2.3	18.2	-5.5
3	15.8	-4.1	18.3	-4.9
4	17.2	4.4	20.3	5.5
5	17.4	5.6	20.6	7
6	17.4	5.6	20.3	5.5
7	15.8	-4.1	18.2	-4.9
μ	16.48		19.25	

PACIFICr2: Offset Mismatch

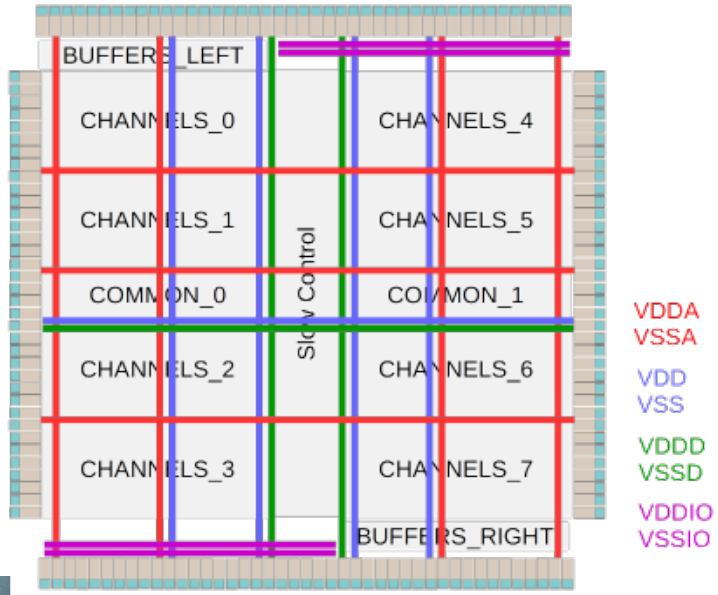
- Offset variation observed at the output of the integrator.
- Spread among channels accounts for slightly less than 1PE.
- Mismatch between channel integrators also close to 1PE.
- Single photoelectron detection cannot be assured.

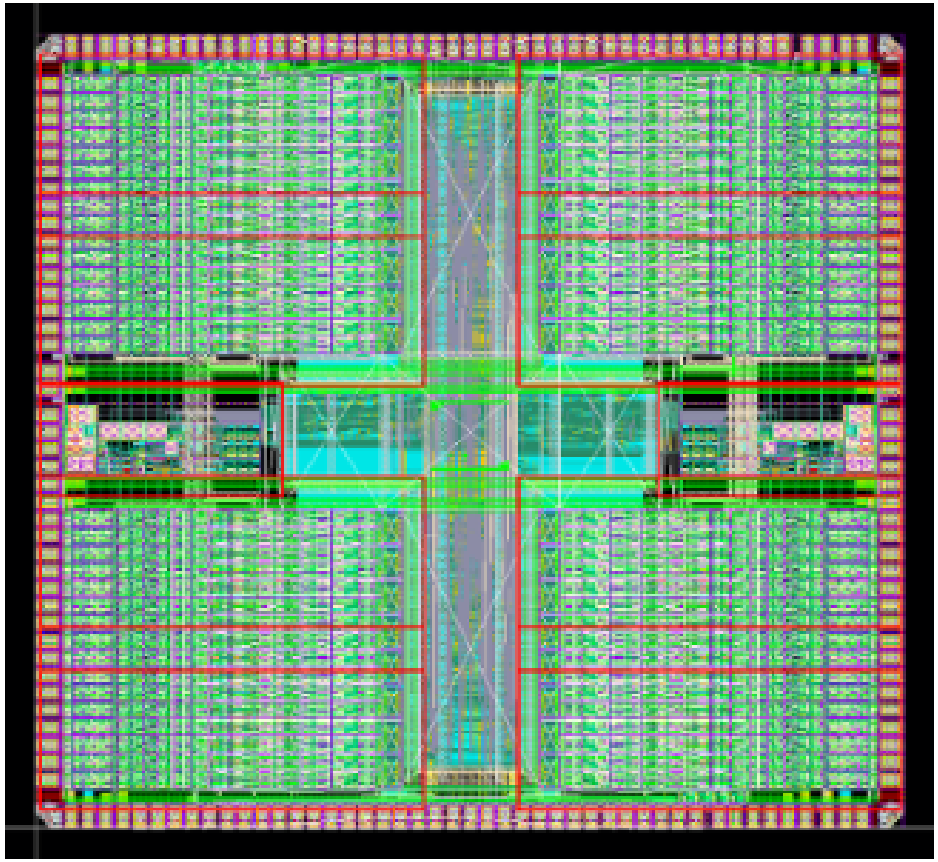




PACIFICr3

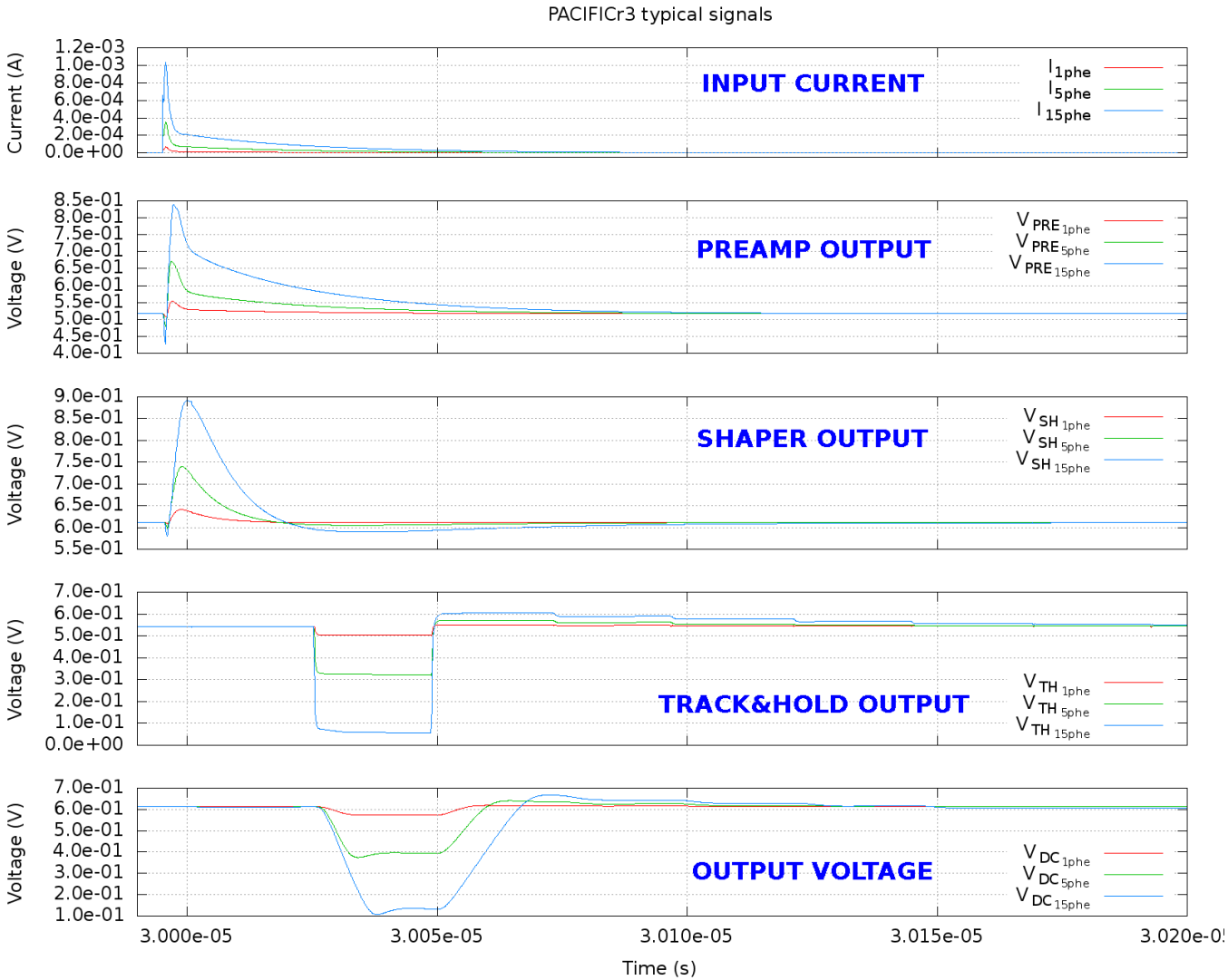
- PACIFICr3 will be first fully usable prototype.
- Migration to TSMC 130 nm tech. required full layout redesign.
- Channels pitch changed to 80μm, staggered pads are removed.
- Digital on top integration.
- New two sided floorplan.
- Size 4000 $\times$ 3650=14.6 mm^2.
- Returned on September 16th.





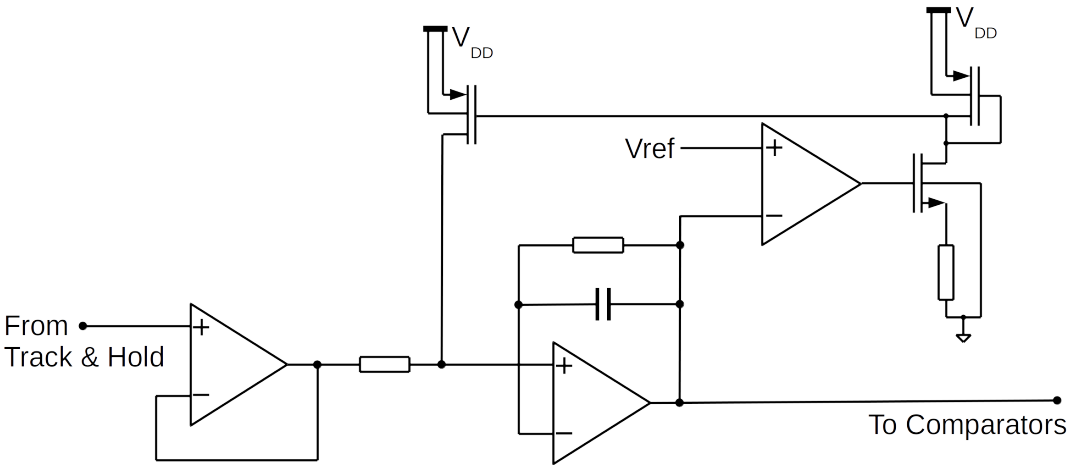
PACIFICr3: Analog Signals

- Full extracted simulations yield similar response after migration.

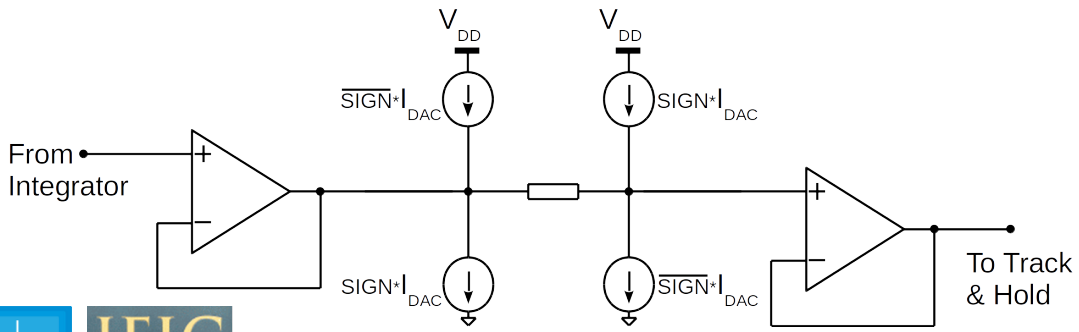


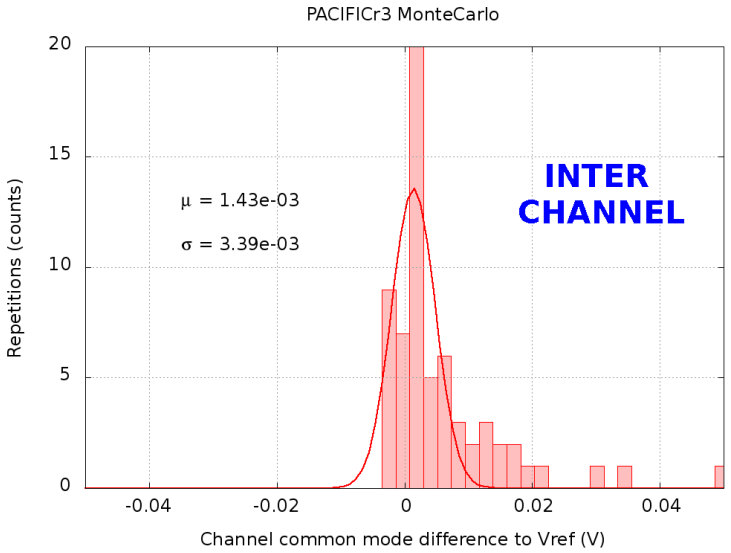
PACIFICr3: Offset Correction

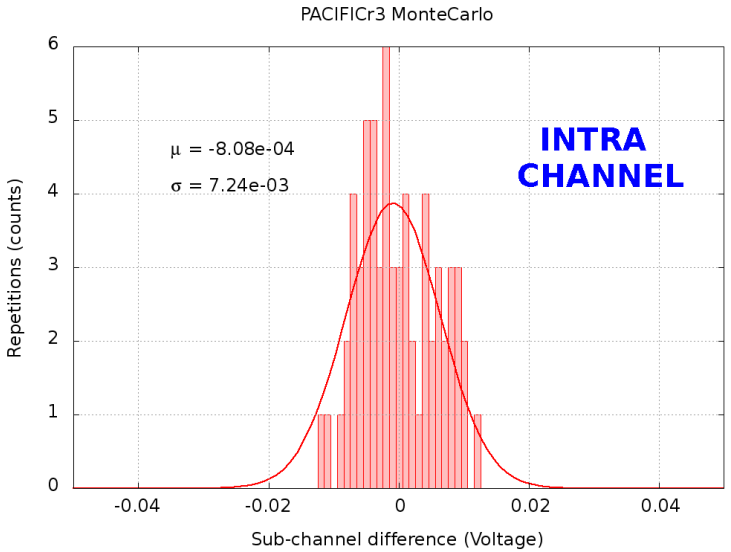
- Closed loop T&H output DC correction.
- Inter-channel spread reduced to ¼PE.
- Intra-channel mismatch still over ½PE.



- Current injection intra-channel correction.
- Controlled by 6 bit DAC plus sign bit.







Outlook

- PACIFIC is a readout ASIC for fast scintillating fiber trackers with SiPM sensors.
  - Current input with direct SiPM anode connection.
  - Fast PZ cancellation shaping for tail suppression.
  - Gated integrator damps statistical fluctuations.
  - Non-linear 2 bit digital output.
  - Highly configurable operation optimizing timing and sensitivity.
- Channel architecture has been fully validated.
- No loss of performance in simulation due to migration to TSMC 130 nm, test in progress.
- Upon results project moves on to production phase.

Acknowledgements:
Blake D. Leverington, Fred Blanc, Wilco Vink, Guido Haefeli,
Zhirui Xu and many colleagues of SciFi project

Thanks a lot for your attention!