A New Amplifier Shaper Discriminator for the Readout of the MDT Drift tubes in the ATLAS Muon Spectrometer in IBM 130 nm Technology

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History: The ASD in Agilent 500 nm technology *)

1997 -2003 development of the chip (8-channels)
2004 production of 50k packaged chips
→ test of threshold spread among the 8 channels/ASD leads to 3 categories of quality (< 12, <16, <20 mV)
2005 → rad-tol tests up to 1 Mrad: no failures
→ the lvds-driver allows for undefined logic levels → hangups in the TDC !

2007-15 → reliable operation in „edge mode“
→ very low failure rate of ASDs

*) MDT-ASD *User's Manual* ATL-MUON-2002-003, rev. 2.1
Y. Arai et al., *ATLAS Muon Drift Tube electr.*, 2008 *JINST* **3** P09001

Functional diagram of the ASD

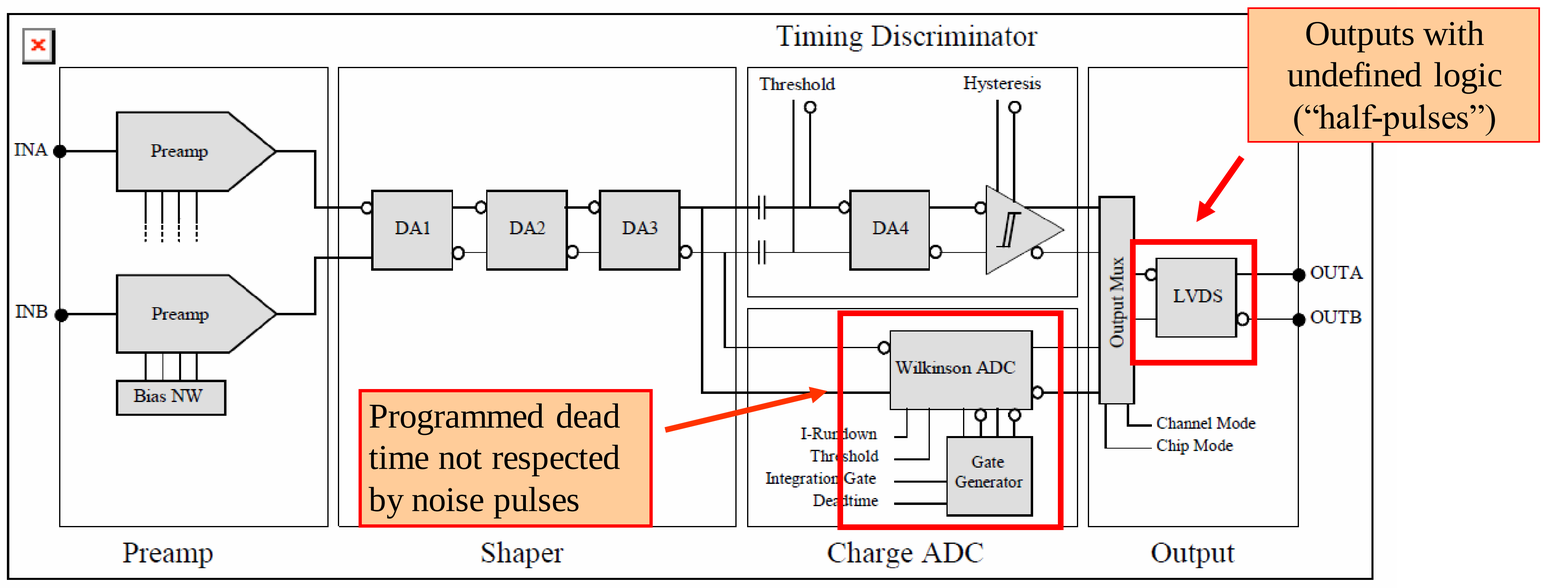


Figure 2. MDT-ASD channel block diagram

50k New ASDs needed for the Phase-II Upgrade of the Muon Spectrometer

- The Agilent technology is no more available. Go to new design in IBM 130 nm, supported by CERN
- Design aims:
  → match the "good" properties of the Agilent chip
  → fix the lvds driver problem to be able to use "pair mode", allowing a factor of 2 higher hit rates at the HL-LHC

New ASD in IBM 130 nm technology

2008 prototype of the analog part of a 4-chan. vs.
→ good matching of shape and gain (1,5%)
→ peaking time ~ 25ns instead of ~15 ns
2010 new version, incl. digital part (4 channels)
→ peaking time still > 15 ns
→ functional problems with Wilkinson AD
2013 cooperation MPI and Univ. Milano
→ modif. to reduce parasitic capacitances
→ redesign of Wilkinson and lvds driver
→ pre-tapeout tests: SPICE, PLX, LVS, PVT
2014 submission of new chip in november
2015 chips returned in febr. 2015, tests in april-september (still ongoing)

Verify chip performance

First use SPICE simulation, then, after layout, Post Layout eXtracted simulation (PLX) to check on the following parameters:

- Peaking time vs. Input charge
- Peak output volt. vs. Input charge
- Frequency response
- Transient noise

} Pre-amp, DA1, DA2, DA3

- Wilkinson discharge time vs. Input charge
- DISCR delay
- Serial interface and DACs

For all parameters:
check dependence on Process, Voltage and Temperature (PVT)

E.g.: PLX vs. SPICE simul. of peak time

ASDW Channel Layout Activity.
Post-Layout Simulations. Transient Simulation with QIN=5fC.

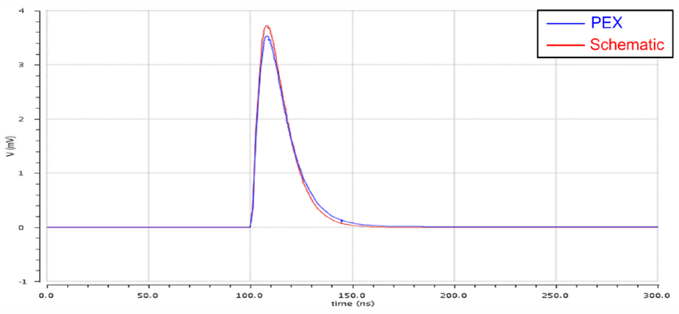
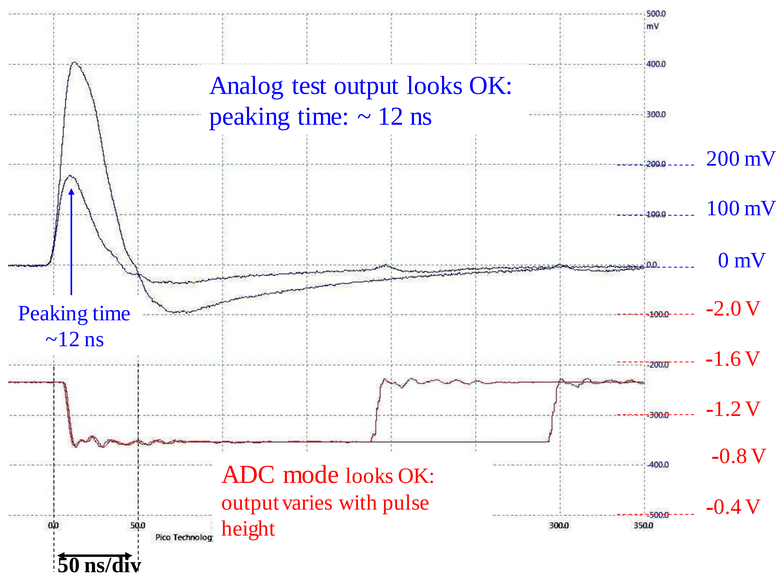


Fig. 4 – CSPreamp Output Voltage with QIN=5fC.

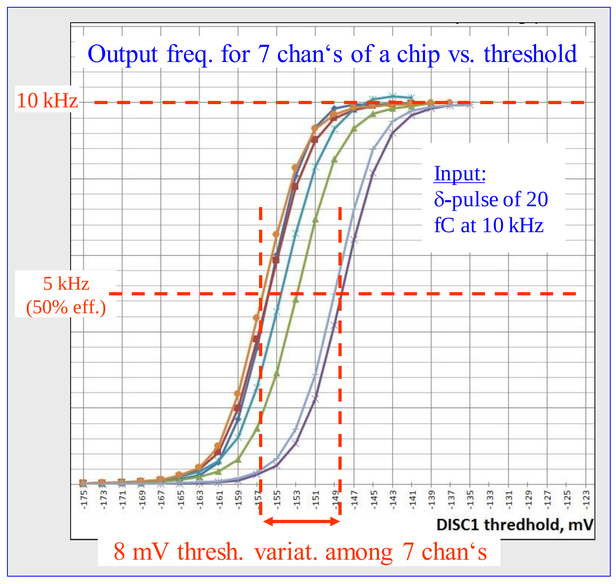
PARAMETERS	SCHEMATIC	PEX
Noise (in-Band Integrated)	547u	635.3u
Vdd1 Current Consumption	-4.173m	-4.236m
Preamp_peaking_time	8.529n	8.084n
DA1_peaking_time	9.404n	8.938n
DA3_peaking_time	10.52n	10.57n
Vpeak	3.75mV	3,5mV
PREAMP Sensitivity	0.74mV/fC	0.7mV/fC

Good match between Spice and Post-Layout Simulation (PEX), which takes e.g. stray capacitances into account.

First results testing the ASD vs. 4

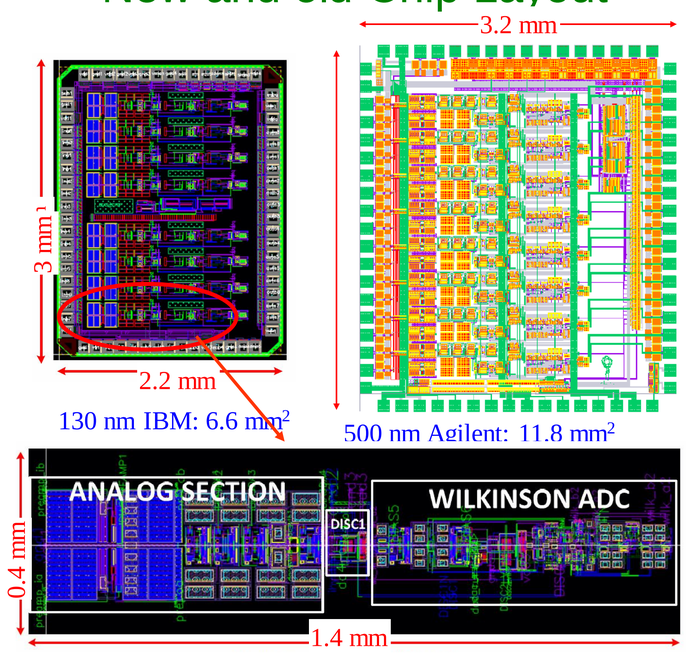


Threshold Scan of the ASD vs. 4

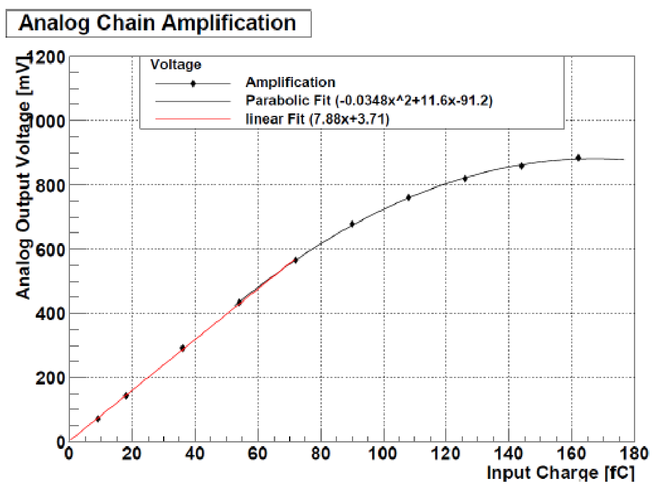


NB: ch. #7 (with analog output!) is off-scale by 30 mV

New and old Chip Layout



Range of linearity up to ~ 90 fC



Design aims for next submission:

- remove coupling from Discr. to Input
- improve ADC uniformity (pulse length vs. charge)
- improve dead-time uniformity
- fix some errors in the JTAG coding
- go for next submission in nov/dec
- go for production maturity by 2017
- chip to be used for new MDT readout electronics of the Muon Drift Tubes in Phase-II of the HL-LHC

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