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Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT Chambers at the HL-LHC

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The Phase-II Upgrade of the ATLAS Muon Detector requires new electronics for MDT drift tubes. The first processing stage, the channel Amplifier-Shaper-Discriminator (ASD), determines the performance of the read-out for crucial parameters like time resolution, gain uniformity, efficiency and noise rejection. An 8-channel ASD chip, using the IBM 130 nm CMOS 8RF-DM technology, has been designed, produced and tested. The area of the chip is 2.2 * 2.9 mm2 size. We present results of detailed measurements as well as a comparision with simulation results of the chip behaviour at three different levels of detail.

Summary

The HL-LHC at CERN will operate at peak luminosities of a factor 5 –7.5 beyond the nominal value of 10^{34} cm^{-2} s^{-1}. The high luminosity is a challenge for the readout system of the MDT chambers in the ATLAS Muon Spectrometer in two respects. Higher hit rates, mainly due to increased cavern background, drive data transmission to the rear end electronics to the limit of available bandwidth. In addition, the new operating parameters of the L1 trigger –latency up to 60 μs and trigger rates up to 400 kHz - call for a replacement of the entire readout chain of the MDT chambers.

The most critical element in the readout chain is the first stage, Amplifier with Shaper and Discriminator (ASD), as e.g. signal risetime, signal-to-noise performance and threshold uniformity among channels are decisive for system parameters like spatial resolution of the track coordinates and tracking efficiency.

To cope with this requirements, a chip was developed in the IBM 130nm CMOS 8RF-DM technology. The design contains a preamplifier, three shaping stages and a discriminator. In addition, a Wilkinson ADC is implemented measuring the charge inside a predefined integration window of about 15 ns, which is an approximate measure of the amplitude of the initial signal triggering the discriminator. The ADC information allows for a slewing correction to be applied to the time of threshold crossing (measurement of the drift time) and is useful for monitoring the stability of the gas gain and other operational parameters over extended periods. The size of this 8-channel chip is 2.2 x 2,9 mm2.

We present measurements of crucial performance parameters of the chip like signal rise time, signal-to-noise, uniformity of signal gain and threshold among the 8 channels. The hysteresis of the discriminator is presented as well as the linearity of the ADC w.r.t. the incoming signal. The measured quantities are compared to the results of detailed simulation work done before the submission of the chip. The critical influence of stray capacitances on the peaking time of the signal is discussed in more detail, demonstrating how details of the preamplifier layout may be decisive for the perfomance of the final chip.

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