Contribution ID: **87** Type: **Poster**

Design of the NSW Read Out Controller ASIC

Tuesday, 29 September 2015 16:41 (1 minute)

Part of the New Small Wheel ATLAS Phase-1 Upgrade, the Read Out Controller ASIC will aggregate, process and format the data generated by the VMM front-end chips. The ASIC has a flexible architecture designed to optimize the data bandwidth usage for Micromegas and sTGC detectors and for different NSW regions with different hit rates. The ROC will concentrate the Level-0 data streams from up to 8 VMMs, will filter the data based on the Level-1 BCID and transmit the data to FELIX using up to four GBT E-Links, each capable of 320 Mbps data transmission.

Summary

The ATLAS NSW detector uses two detector technologies, Micromegas and sTGC, for a combination of triggering and precision tracking functions in the Inner End-Cap region of the ATLAS detector. For the readout path, the two detectors will use the same building blocks, the VMM front-end chip and a readout companion ASIC, the Read Out Controller (ROC) chip. The latter is designed to aggregate, process and format data generated by the front-end ASIC, removing the complexity of Level-1 data selection from the already complex mixed-mode front-end chip. The ROC chip is one of the first readout ASICs to use the new CERN GBT architecture for data transmission and reception of TTC information. It sends data to the downstream readout system via "E-links", low speed serial electrical links that are aggregated onto a 5Gb/s fiber by the CERN GBT chipset.

The two detector technologies have different segmentations and different topologies, while the hit rate varies by more than one order of magnitude across the area of the NSW detector. The ROC chip employs a flexible architecture which gives the possibility to optimize the usage of available data bandwidth across the system. In hot regions, the ROC is connected to a small number of front-end chips while sending output on fast E-Links. For the coldest regions the data collected from more front-end chips is transmitted via a single low speed link.

The chip consists of 8 VMM Capture blocks and 4 Sub-Readout Controllers (SROC) interconnected via a configurable crossbar. The VMM Capture module receives data packets from the front-end chip corresponding to the first level of trigger, via a 640 Mbps double data rate serial interface, using 8b/10b encoding. The data is deserialized, comma-aligned, decoded and stored in a local FIFO.

The sub-ROC modules access the FIFOs of a configurable number of VMM Capture modules via the crossbar. For Phase-2 operation of LHC, the sub-ROC will use the Level-1 BCID information to filter the corresponding data packets, eliminating at the same time old data. The data packets are merged and reformatted, before being sent over an E-Link to a GBT chip. Each of the four E-Links of the four sub-ROC modules can be configured to transmit data at 80, 160 or 320 Mbps. The data sent over E-links is 8b/10b encoded.

In addition to the readout functions, the ASIC decodes the TTC information from an incoming E-Link and distributes clock and other TTC signals to the front-end chips. For this purpose, the ASIC will integrate the ePLL IP core from the CERN GBT framework.

The design of the ROC ASIC uses triple redundant SEU mitigation techniques on the configuration and control circuitry, while on the data flow single-bit parity checking is used to signal the unlikely event of data corruption. The ASIC is designed and will be fabricated in a 130 nm commercial CMOS technology.

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Session Classification: Poster

Track Classification: ASICs