A CMOS 0.18 µm 600 MHz clock multiplier PLL and a pseudo-LVDS Driver for the high speed data transmission for the ALICE Inner Tracking System front-end chip.

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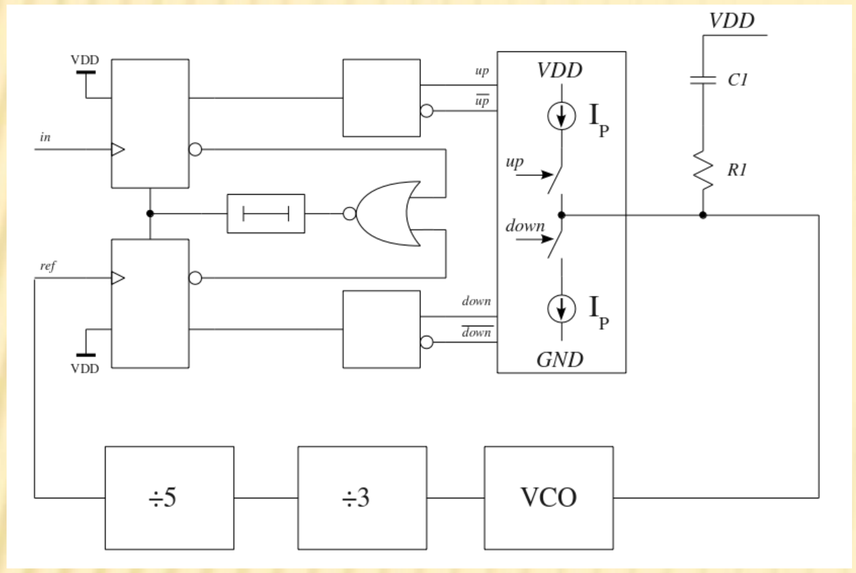
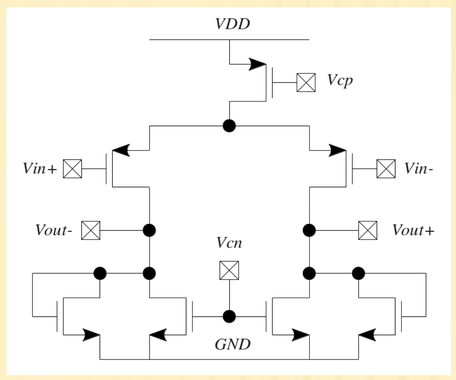
The upgrade for the ALICE Inner Tracking System (ITS) foresees to fully replace the present ITS with a new one entirely based on monolithic active pixel sensors [1], covering 10 m^2 with 12.5G pixels. The CMOS sensor chip containing about 500 000 pixels measures 3 ×1.5 cm^2 and needs to transmit the data at 1.2 Gb/sec for the 3 inner layers, and at 400 Mb/s for the outer layers. This required the design of a data transmission unit with PLL, serialiser and a pseudo-LVDS driver. In this poster we report on the design and measurements of both PLL and LVDS driver which were submitted on a small test chip. The PLL provides a 600 MHz clock from the 40 MHz LHC clock. 1.2 Gb/s is achieved using Double Data Rate. A charge pump PLL with a clock multiplication factor of 15 has been designed.



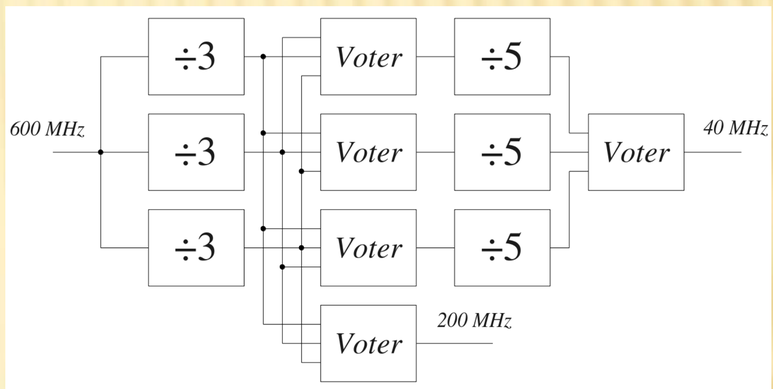
[1] http://iopscience.iop.org/1748-0221/8/12/C12041

VCO



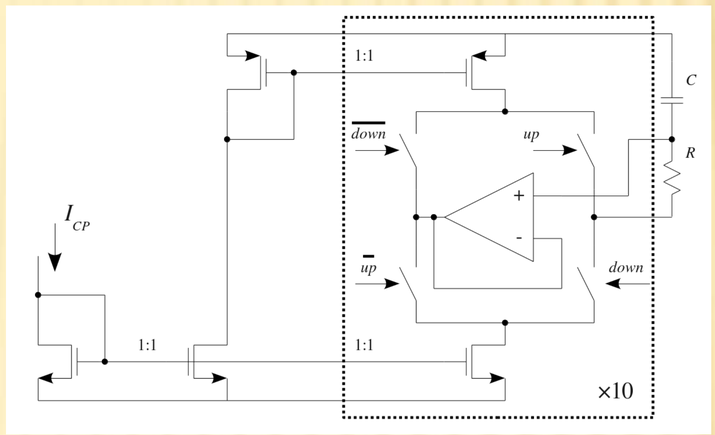
N. of stages : 4
Power : 15.34 mW
Tuning range : 450-750 MHz

DIVIDER BY 15



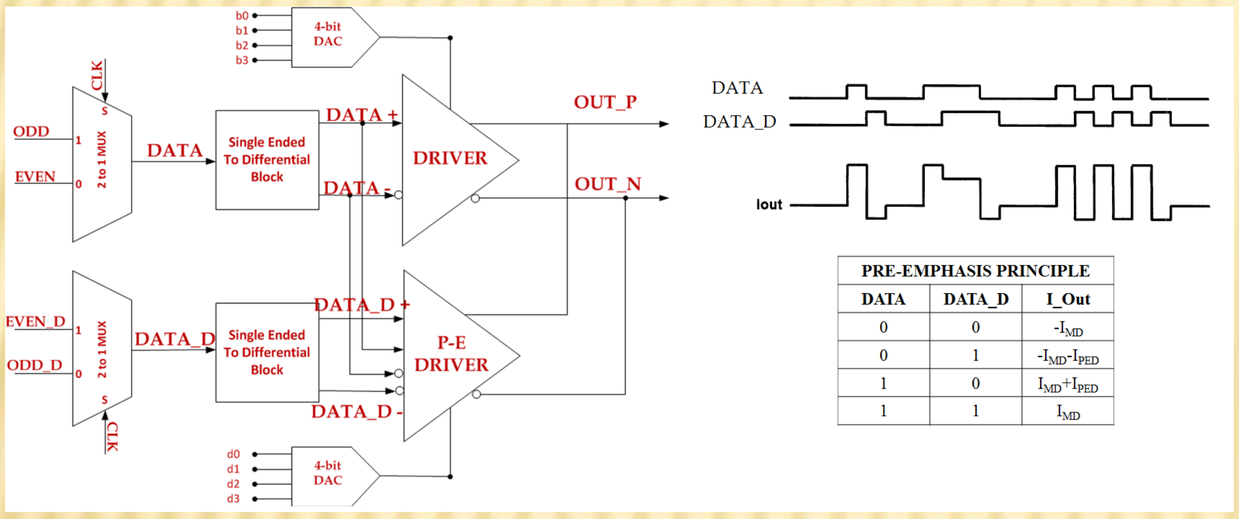
The two dividers are SEU protected.

Charge Pump



To reduce static phase error:

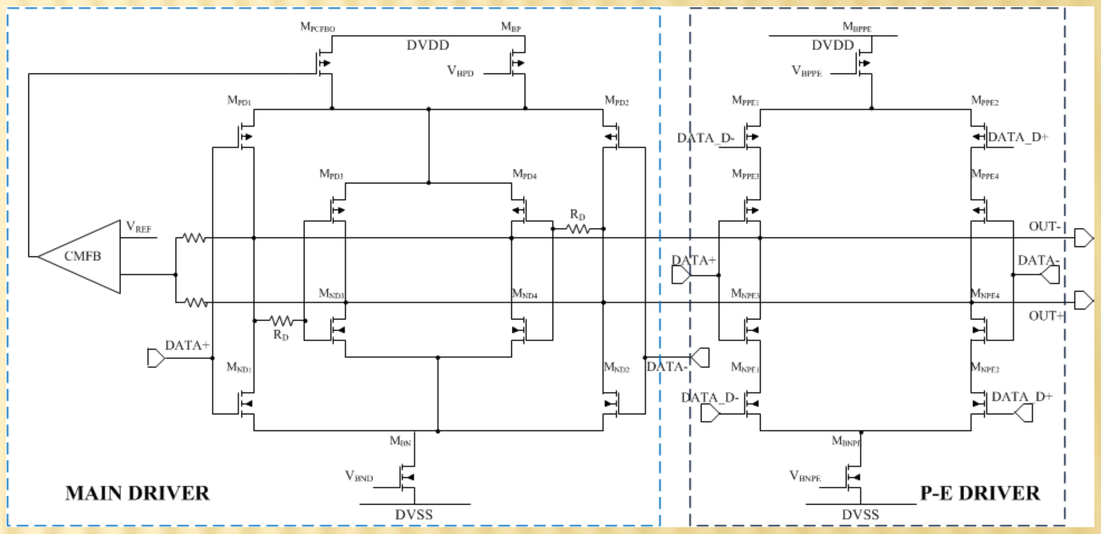
- High output impedance transistors
- Unity Gain Amplifier feedback for voltage drain equalization



PRE-EMPHASIS PRINCIPLE		
DATA	DATA_D	I_Out
0	0	$-I_{MD}$
0	1	$-I_{MD}-I_{PED}$
1	0	$I_{MD}+I_{PED}$
1	1	I_{MD}

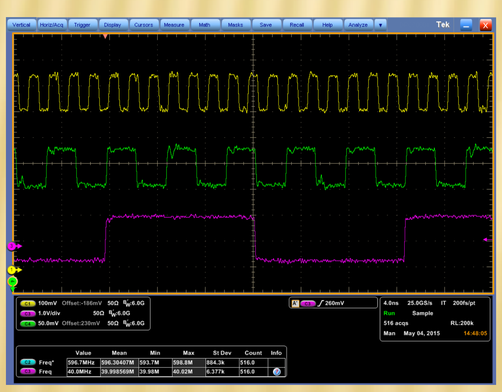
This pseudo-LVDS driver consists of

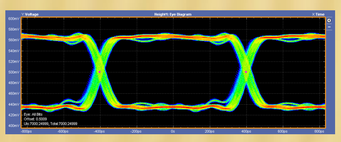
- Two multiplexer for the selection of the data streams coming from a serializer.
- Two blocks which gives the two phases of the output multiplexers signal (DATA+ , DATA – and the same delayed streams DATA_+ and DATA_D-);
- A main driver (MD) which works in current steering mode;
- An ancillary pre-emphasis (PED) driver which implements a XOR logic. Pre-emphasis will be active only if two consecuitive bits are different.
- Two 4-bit DAC to select the MD and PED currents.

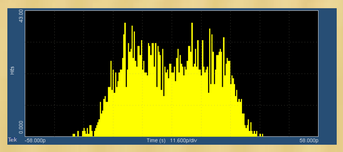


- This driver has to drive a full 5m/6.5m transmission line by working at the target speeds of 1.2 Gb/s/400 Mb/s respectively so that the pre-emphasis technique is mandatory to overcome the RC limitations imposed by the line.
- In order to deal with a 1.8V power supply, the output driver common mode is set to 1.1V.
- The main driver steers a maximum 5 mA of DC current.
- The pre-emphasis gives at maximum 2.5 mA of current and adjusts the local value of the current if a bit transition occurs.

600 MHz clock multiplier PLL Test Measurements



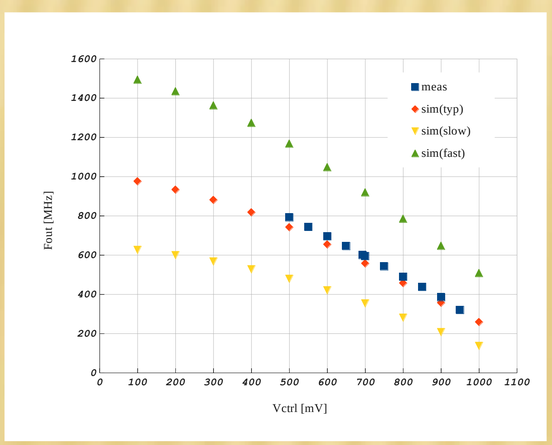




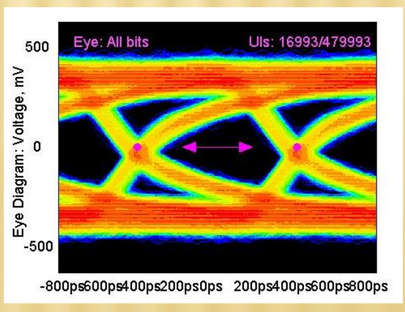
Random Jitter	4.736 ps (r.m.s.)
Periodic Jitter	46.342 ps (pk-pk)

Input frequency : 40 MHz
Input frequency range : 30 MHz -50 MHz
Main output frequency : 600 MHz (f_{IN} × 15)
Secondary output frequency : 200 MHz (f_{IN} × 5)

	Mean	σ
clock period	1.667 ns	6.8642 ps
clock frequency	600.01 MHz	2.4708 MHz
duty cycle	50.79%	0.0896 %

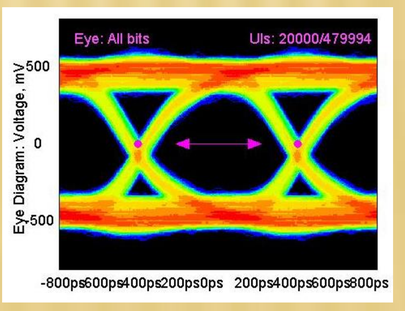


Pseudo-LVDS Test Measurements with a 5m long transmission line

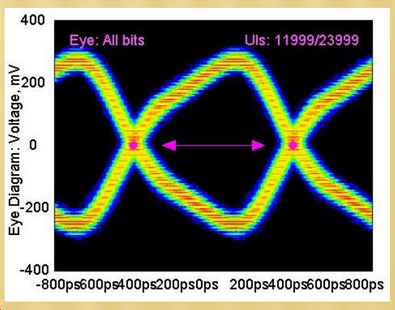


(a) Total Jitter: 0.57 UI

Fig. 1. Test Measurements with a 2^{31}-1 PRBS input signal. The MD steers 4 mA of current at 1.2 Gb/s with: (a) 0% of pre-emphasis; (b) 50% of pre-emphasis.

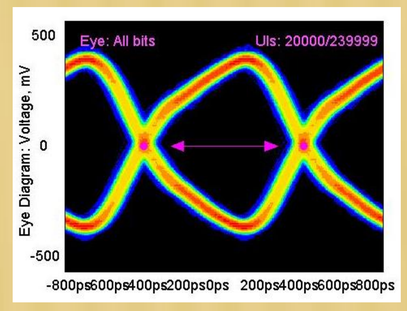


(b) Total Jitter: 0.4 UI



(c) Total Jitter: 0.35 UI

Fig. 2. Test Measurements with a PLL 600 MHz clock input signal. The MD steers 4 mA of current at 1.2 Gb/s with: (c) 0% of pre-emphasis; (d) 50% of pre-emphasis.



(d) Total Jitter: 0.30 UI