Contribution ID: **85** Type: **Poster**

A CMOS 0.18 µm 600 MHz clock multiplier PLL and a pseudo-LVDS Driver for the high speed data transmission for the ALICE Inner Tracking System front-end chip.

Tuesday, 29 September 2015 16:39 (1 minute)

This work presents two essential components for the high speed data transmission of the ALICE inner detector front-end chip. The PLL multiplies the 40 MHz input clock in order to obtain the 600 MHz clock for the 1.2 Gb/s Double Data Rate serializer and a 200 MHz output for the 400 Mb/s driver. The pseudo-LVDS driver transmits the data from the pixel chip with a limited number of signal lines. It drives a 5m-6.5m differential transmission line by steering a maximum 5mA at the targeting speeds of 1.2Gb/s. A pre-emphasis technique was adopted to overcome the cables RC limitations. Both circuits are designed in the same CMOS 0.18 µm technology used for the pixel chip.

Summary

Due to the increase of LHC luminosity, the ITS will be upgraded and equipped with 7 layers of Monolithic Active Pixel Sensors (MAPS) in order to increase the pixel granularity. Actually, a size reduction of the pixel chip from the current 50 µm x 425 µm to 28 µm x 28 µm is foreseen. This increase of the granularity together with the increase in luminosity will lead to a corresponding increase of data volume which requires a fast data transmission system for the front-end chip.

The targeting speeds which will not limit the read-out of the full pixel chip are 1.2 Gb/s for the Inner layers and 400 Mb/s for the Outer layers. The pixel chip will be synchronized with the LHC 40 MHz clock . Therefore a PLL is required to provide the 600 MHz clock for the 1.2 Gb/s serial link using Double Data Rate (DDR). A charge pump PLL with a clock multiplication factor of 15 has thus been designed. It is based on a 4 stages ring oscillator which feeds a divider by 3 followed by a divider by 5. Whilst the output of the first divider provides the 200 MHz clock, the output of the second divider is compared with the 40 MHz input clock by a phase-frequency detector (PFD). The PFD in turn controls a charge pump (CP) and a first order RC filter. Both dividers are SEU protected. The PLL bandwidth has been set to the low value of 0.39 MHz in order to filter out the input clock jitter which comes from the low mass aluminum lines for chip interconnections. To reduce the static phase error, the CP current sources have been designed with high impedance transistors and with a unity gain feedback amplifier for drain voltage equalization.

The driver is made up of a main driver and an ancillary pre-emphasis driver since this high speed output will have to drive the full 5m/6.5m transmission line. The pre-emphasis technique has been adopted to overcome the RC limitations of the aluminum cables used to interconnect the chips as well as to drive the full 6.5m transmission line. The driver works in current steering mode providing current to a 100 Ω load resistor. The main driver modulation current ranges between 2 and 5 mA while the pre-emphasis modulation current ranges between 1 and 2.5 mA, so obtaining a 50% pre-emphasis . Both currents are adjustable via two independent 4 bit DACs. The pre-emphasis driver implements a fast XOR logic in order to add o subtract current depending on whether there is a bit transition. While the value of the pre-emphasis current is selectable, the pre-emphasis pulse has a fixed duration of half clock cycle.

The two blocks have been designed in the same 0.18um CMOS Quadruple well technology. A first version of the two circuits was submitted to foundry at the end of the last year and it has been successfully tested. The

full DTU has been submitted in June 2015 both integrated into ALPIDEv3 ASIC and as a separate test chip. In this second version the PLL and the ring oscillator will have an extended tuning capability and a better SEU protection.

Primary authors: LATTUCA, Alessandra (Universita e INFN Torino (IT)); MAZZA, Giovanni (INFN sez. di Torino)

Presenter: LATTUCA, Alessandra (Universita e INFN Torino (IT))

Session Classification: Poster

Track Classification: ASICs