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Design of a Hardware Track Finder (Fast Tracker) for the ATLAS Trigger

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The ATLAS Fast TracKer (FTK) is a custom electronics system that will operate at the full Level-1 accept rate, 100 kHz, to provide high quality tracks as input to the High-Level Trigger. The event reconstruction is performed in hardware, thanks to the massive parallelism of associative memories (AM) and FPGAs. We present the advantages for the physics goals of the ATLAS experiment and the recent results on the design, technological advancements and testing of some of the core components used in the processor.

Summary

The existing three levels ATLAS trigger system is designed to lower the event rate from the nominal bunch crossing rate of 40 MHz to ˜1 kHz for a designed LHC luminosity of 10^{34} cm^{-2} s^{-1}.
When the LHC reaches beyond the design luminosity, the load on the Level-2 trigger system will significantly increase due to both the need for more sophisticated algorithms to suppress background and larger event sizes. The Fast TracKer (FTK) will provide high quality tracks at the beginning of the High-Level Trigger (HLT), exploiting the massive parallelism of Associative Memories (AM) and FPGAs.
An important characteristic of the system is data reduction step by step. The first reduction happens in the FTK input system is ATCA based and composed by the Data Formatter card and the input mezzanines. The input mezzanines equipped with Spartan6 and Artix7 FPGAs cluster the incoming hits from the pixel sensors.The system processes about 800 Gb/s of data on the fly. The Data Formatter hosting a Virtex7 with 80 high-speed links reorganizes data from the Inner Detector into trigger towers that will be later processed by independent engines.
The core pattern recognition algorithm of FTK operates in two stages. In the first stage, the data from 8 of 12 silicon detector layers are used to perform pattern recognition and do the initial track fitting. Pattern recognition is carried out by a dedicated system called the AM which finds track candidates in coarse resolution roads.
The 8-layer fit is carried out by the AUX board that processes silicon detector hits from 3 pixel and 5 strip layers. It sends hits to the adjacent pattern recognition board and receives back candidate roads containing a sufficient number of hits at a maximum rate of 6.4Gbps. For each of these roads, all combinations of 1 hit per layer are fit.. The board is a VME Rear Transition Module (RTM) with six large FPGAs from the Altera Arria V family.

The full track fitting is carried out by the SSB (Second Stage board) a 9U VME board with 6 Xilinx modern FPGAs, and a RTM that provides a fiber interface with the rest of the FTK system. The board receives the 8-layer tracks from the AUX and 4 additional detector hits, with a maximum rate of 6.4Gbps, and performs the full 12 layer track fitting and removes duplicate tracks.
The full list of tracks is sent to the FTK-to-Level2 Interface Crate (FLIC) that organizes the tracks and sends them to memory buffers on the ROS computers where they can be retrieved by the HLT. It is made of two input cards (ATCA blade) and two output cards (ATCA RTM), each with 8 fiber links.
We present the architecture of the FTK system, the results from integration tests at CERN and discuss the expected physics performance in the harsh environment of high pile-up and high luminosities expected for LHC run II and run III.

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