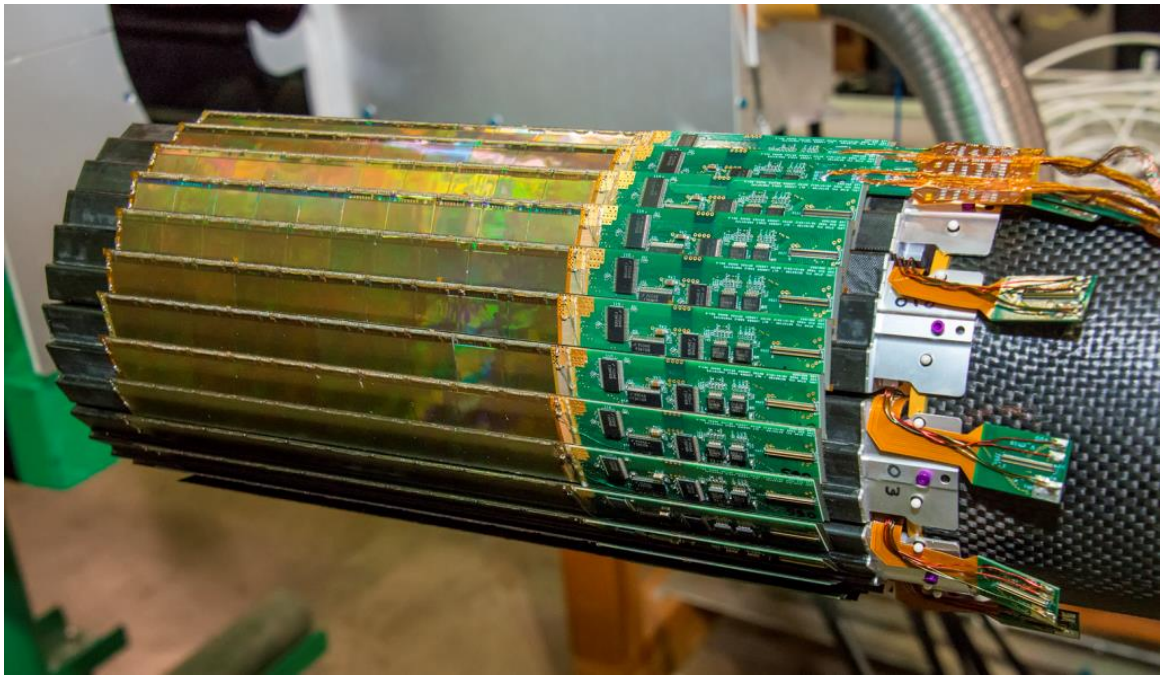
STAR HFT

The STAR Heavy Flavor Tracker
PXL detector readout electronics



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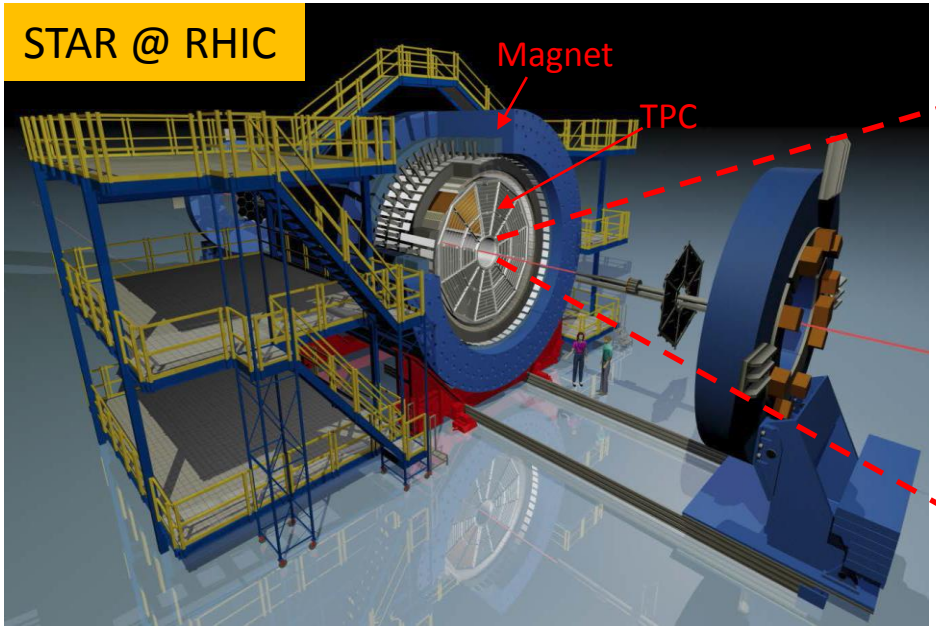
U.S. DEPARTMENT OF ENERGY

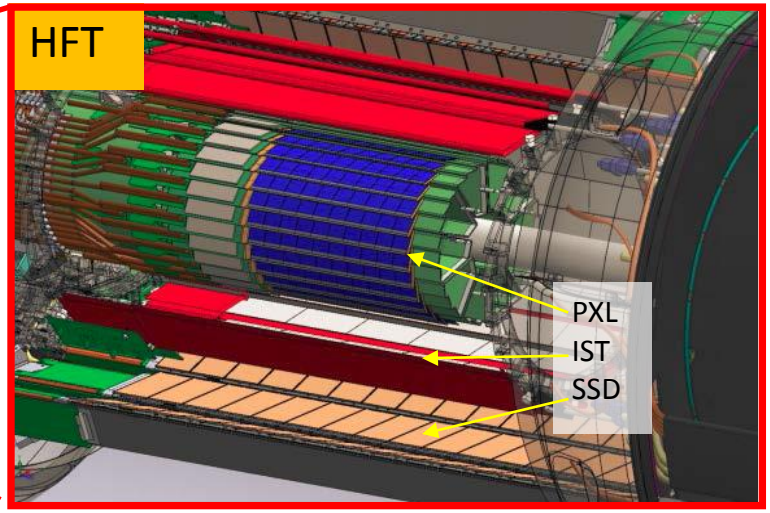
Talk Outline

- Introduction: STAR, HFT, PXL
- Electronics: Hardware
- Electronics: Firmware
- Interfaces: DAQ, USB, Slow Controls
- Summary

Heavy Flavor Tracker @ STAR

STAR HFT





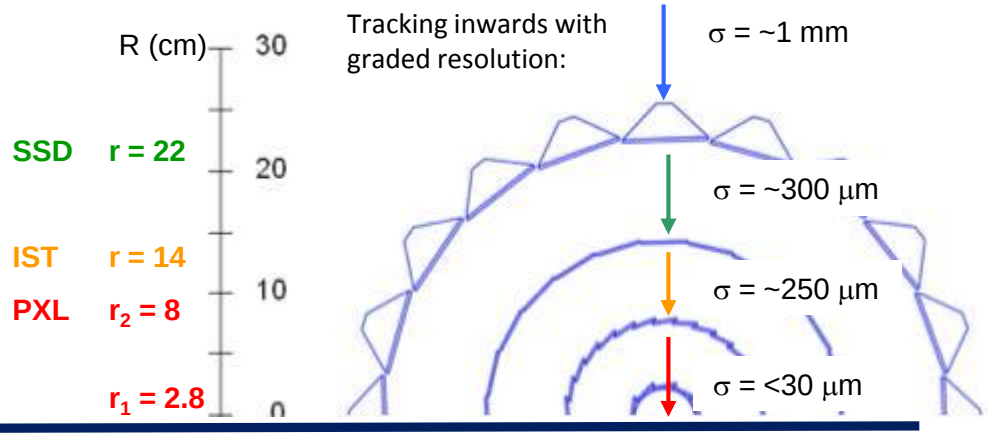
TPC – Time Projection Chamber: main STAR tracking detector

HFT – Heavy Flavor Tracker

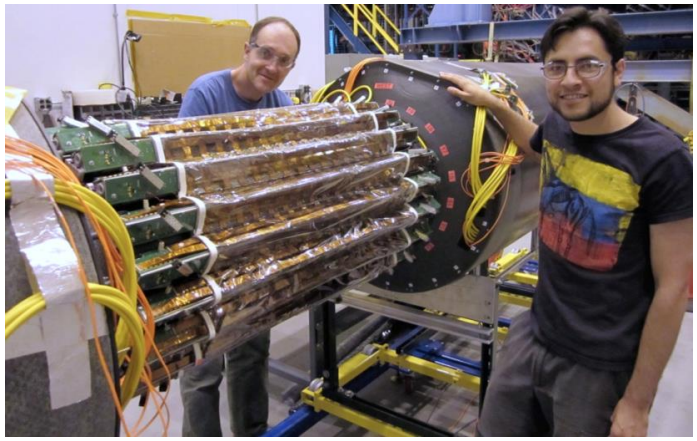
SSD – Silicon Strip Detector

IST – Intermediate Silicon Tracker

PXL – Pixel Detector



HFT Subsystems

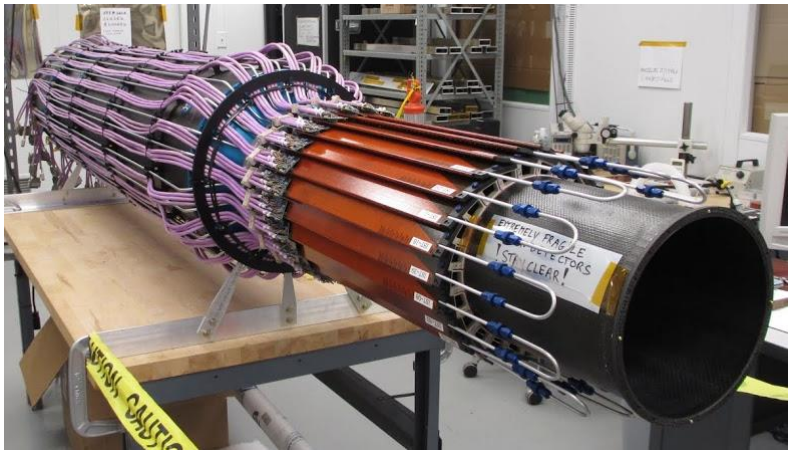


Silicon Strip Detector (SSD)

- Double sided silicon strip modules with 95 µm pitch
- Existing detector with new faster electronics
- Radius: 22 cm

Intermediate Silicon Tracker (ITS)

- Single sided double-metal silicon pad with 600 µm x 6 mm pitch
- Radius: 14 cm

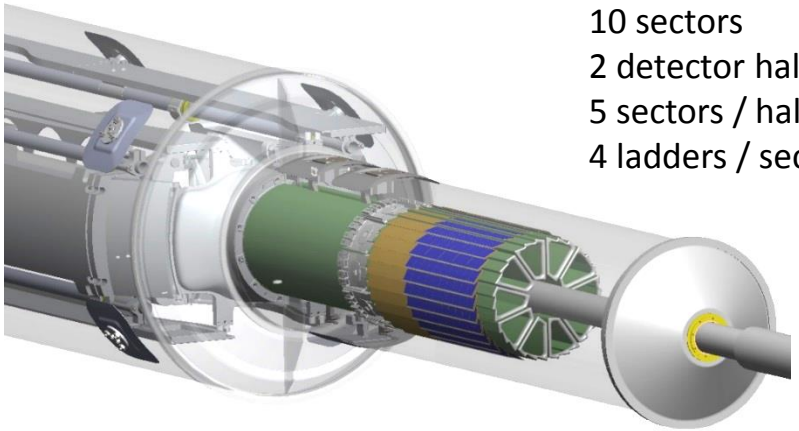


PiXeL detector (PXL)

- MAPS sensors with 20.7 µm pitch pixels
- Radius: 2.8 and 8 cm

First MAPS based vertex detector at a collider experiment

PXL Detector Design

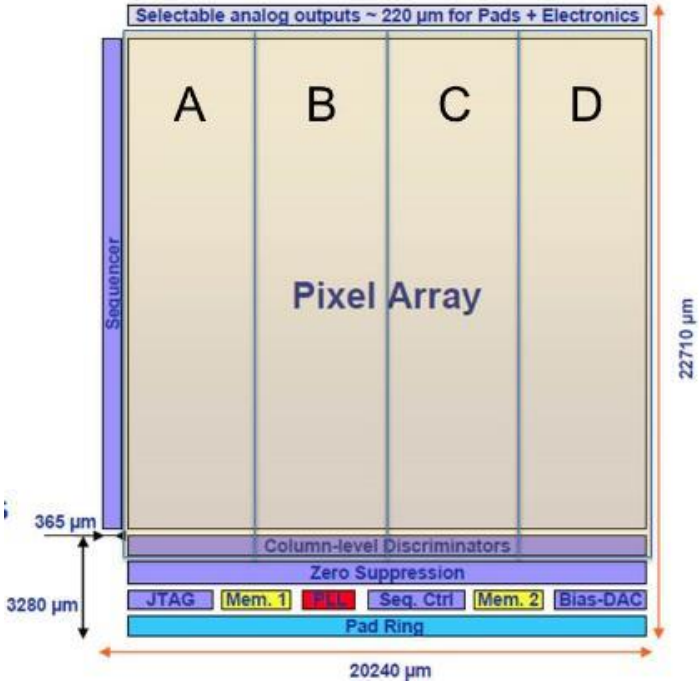


2 layers
10 sectors
2 detector halves
5 sectors / half
4 ladders / sector

Ladder with 10 MAPS sensors (~ 2×2 cm each)

2-layer kapton flex cable with Al traces

MAPS Sensor
"Ultimte-2"



PXL Sensor

- 928 rows * 960 columns =~ 1M pixel
- Rolling shutter, column-parallel readout through end-of-column discriminators
- 185.6 us integration time
- MIP Signal ~ 1000 e^-, S/N ~ 30
- Configuration via JTAG
- In-pixel Correlated Double Sampling (CDS)
- On-chip zero-suppression and run-length encoding on rows (up to 9 hits / row)
- 2 memory banks of 1500 words each for frame readout in ping-pong configuration
- 2 LVDS data outputs @ 160 MHz

Sector Readout Electronics Chain

11 m
(24 AWG TP)

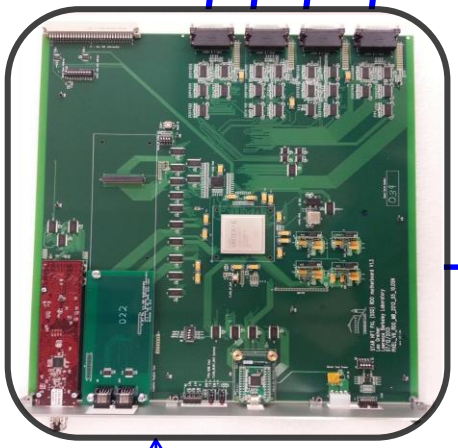
Clk, config,
data

Mass Termination Board
signal buffering + latch-up
protected power

Clock, config,
data, power

2 m (42 AWG TP)

PXL Sector



RDO board
with Xilinx
Virtex-6 FPGA

100 m (fiber optic)

PXL built events

DAQ PC with fiber
link interface board
(ALICE "RORC")

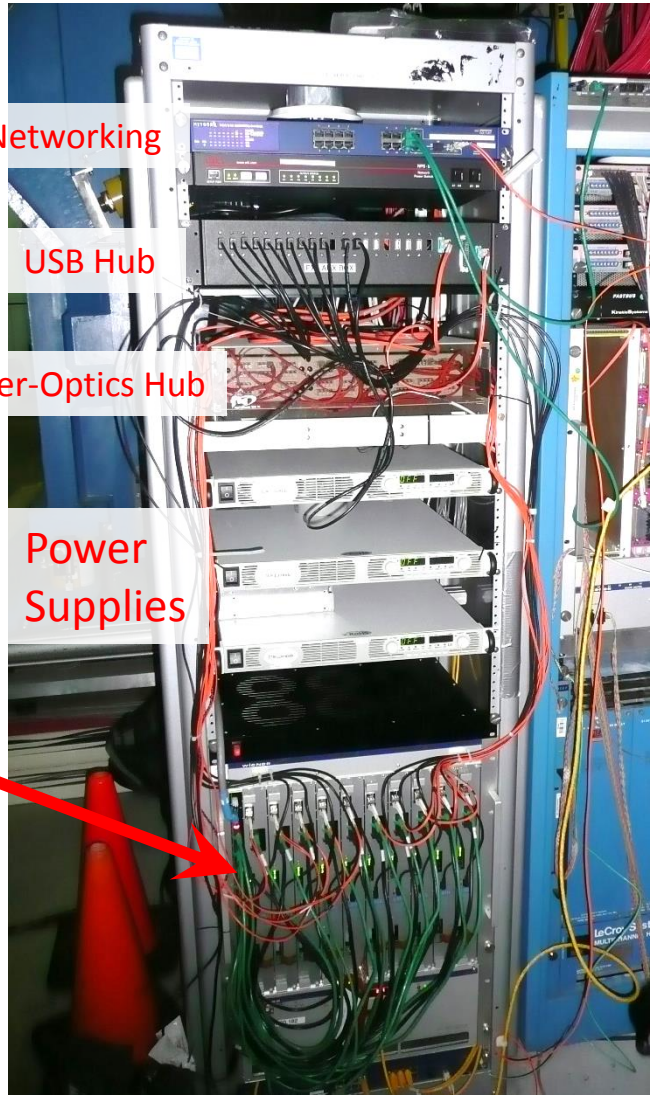
Trigger,
Slow control,
Configuration,
etc.

Existing STAR
infrastructure

Highly parallel system

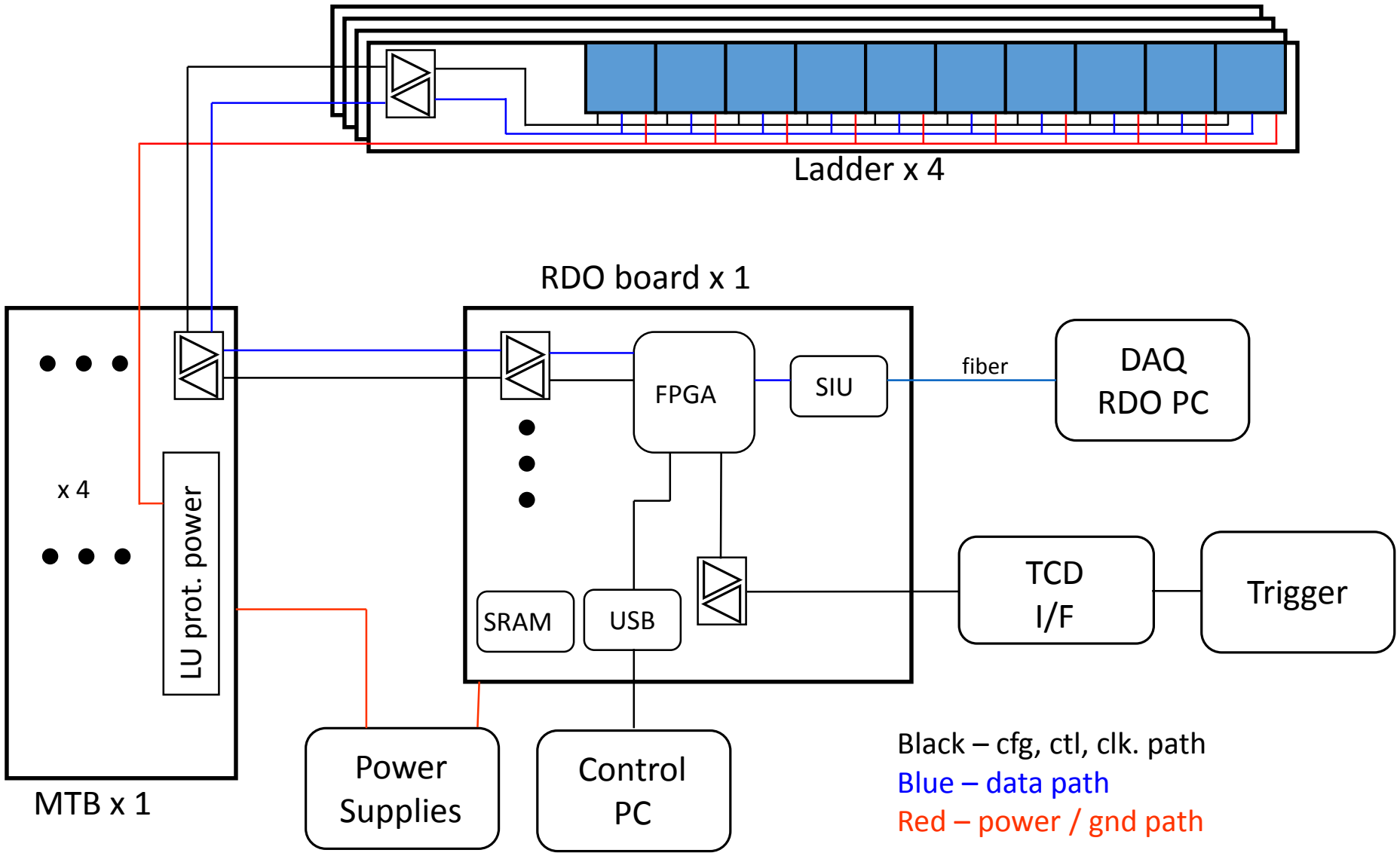
- 4 ladders per sector
- 1 Mass Termination Board (MTB) per sector
- 1 sector per RDO board
- 10 RDO boards total in the PXL system

PXL Readout

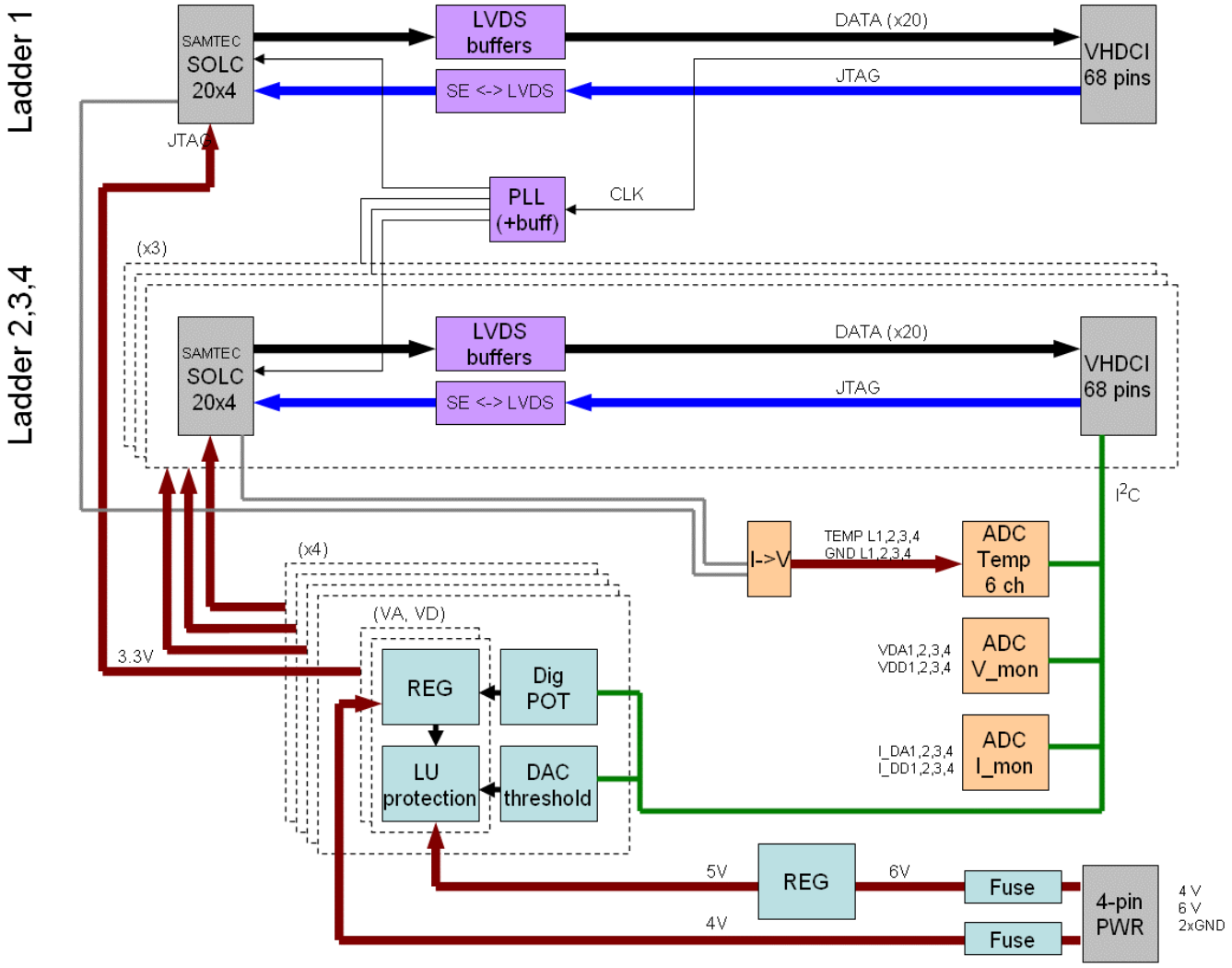


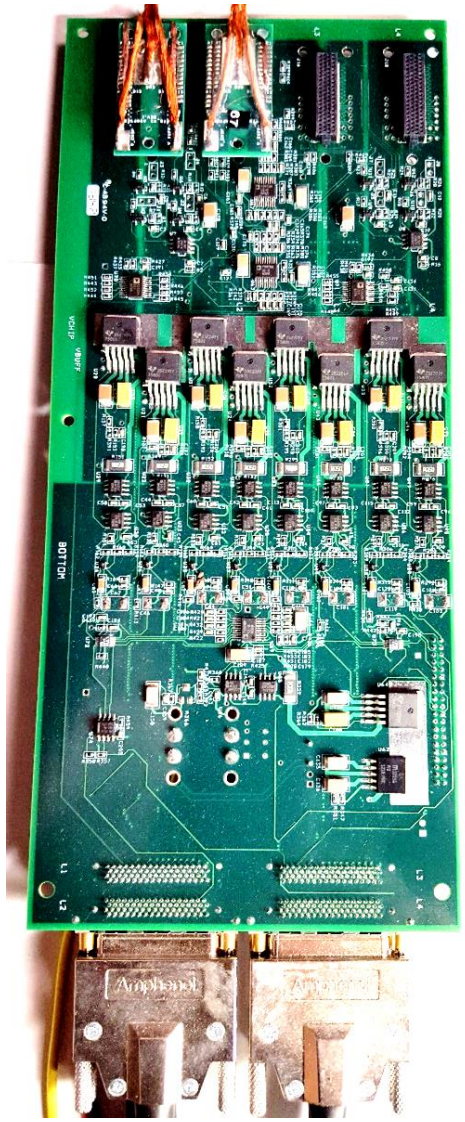
356 M pixel readout in a single 9U size crate

Detailed Sector Readout Architecture

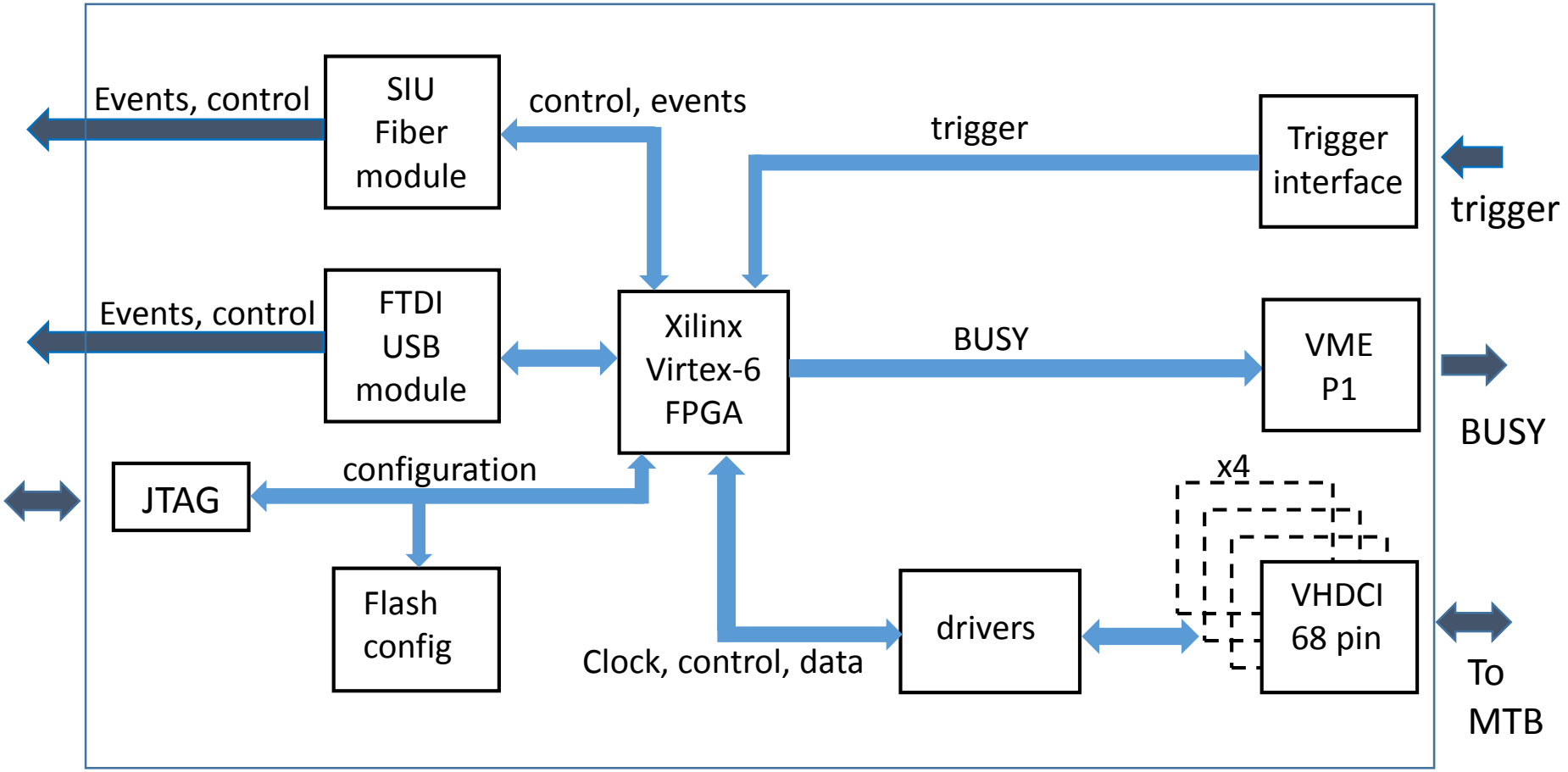


Mass Termination Board (MTB)

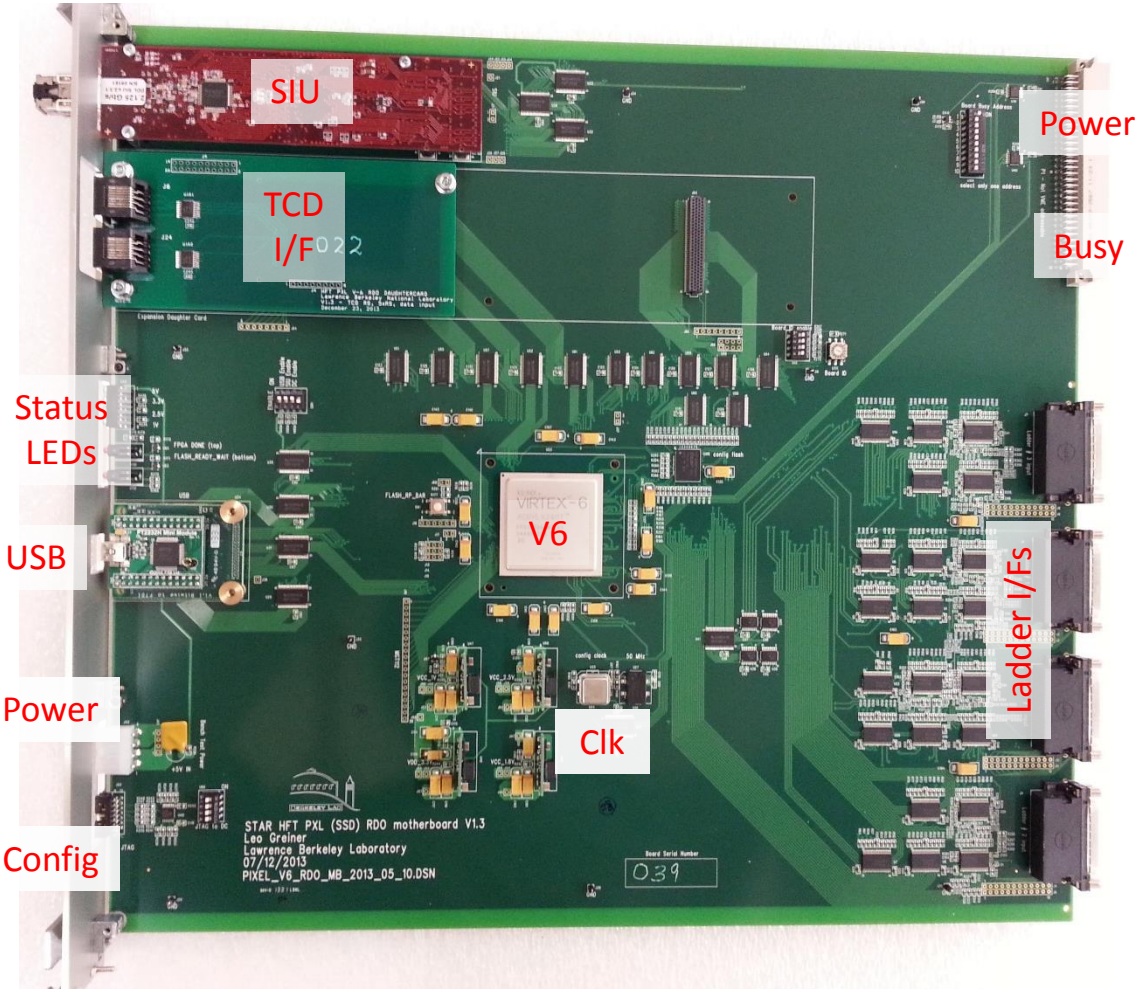




Readout Board Block Diagram



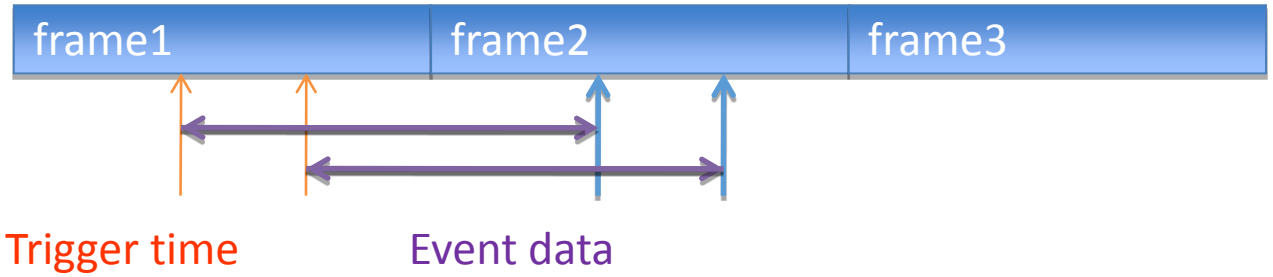
Readout Board (RDO)



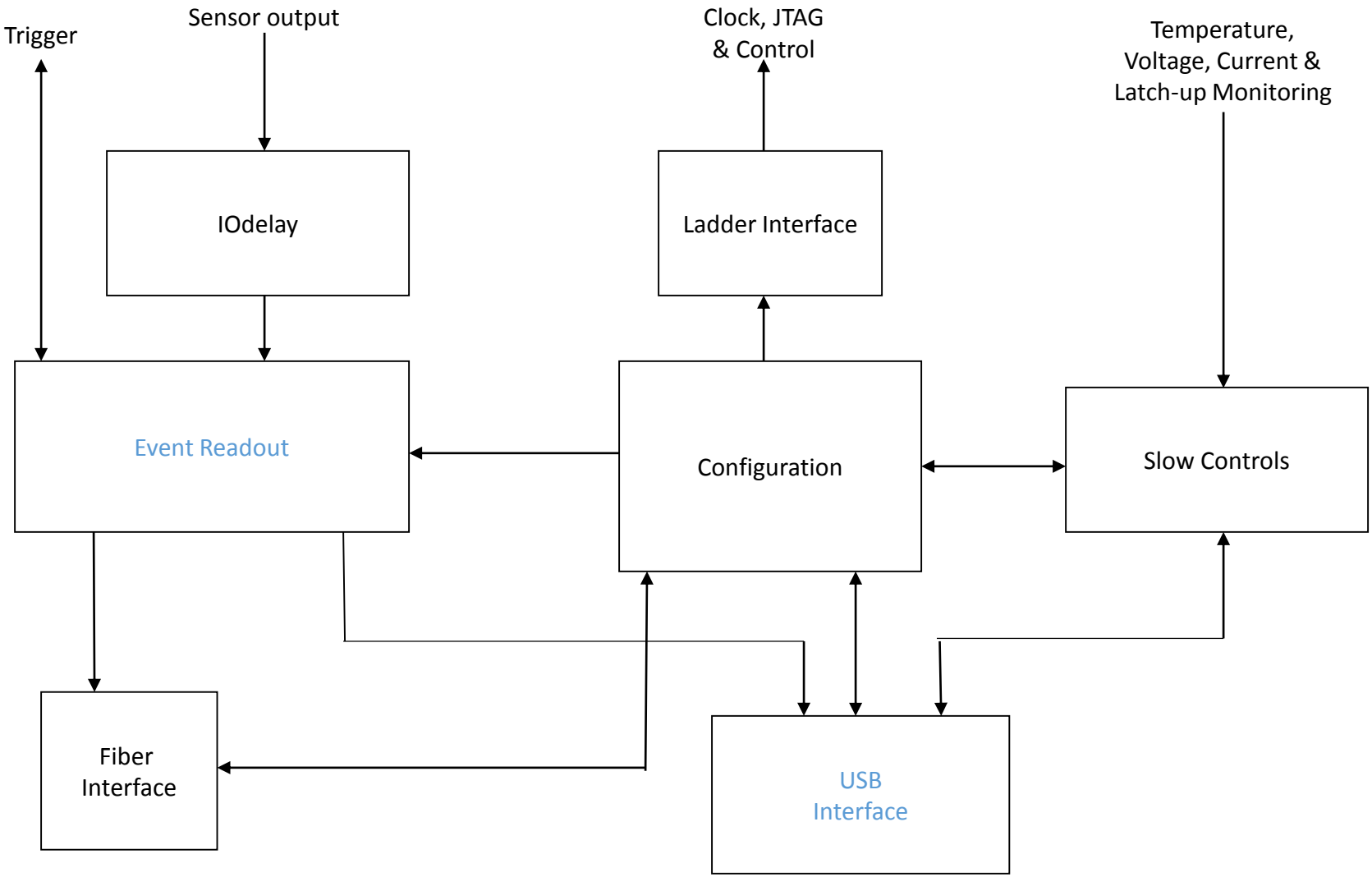
- Virtex-6 LX240T-FF1759:
  - 15 Mb RAM
  - 720 User I/O
  - high-performance SelectIO technology
- FPGA Configuration via either Platform Flash XL (DS617) or front panel JTAG header
- USB Interface: FTDI FT2232H daughter card
- DAQ I/F: ALICE DDL "SIU" daughter card
- Trigger (TCD) interface via daughter card
- Ladder interfaces on the back of the board via VHDCI connectors:
  - Data (LVDS) from sensors
  - Clock to sensors
  - JTAG for sensor config
  - I2C for MTB monitoring & control

Firmware: Readout Requirements

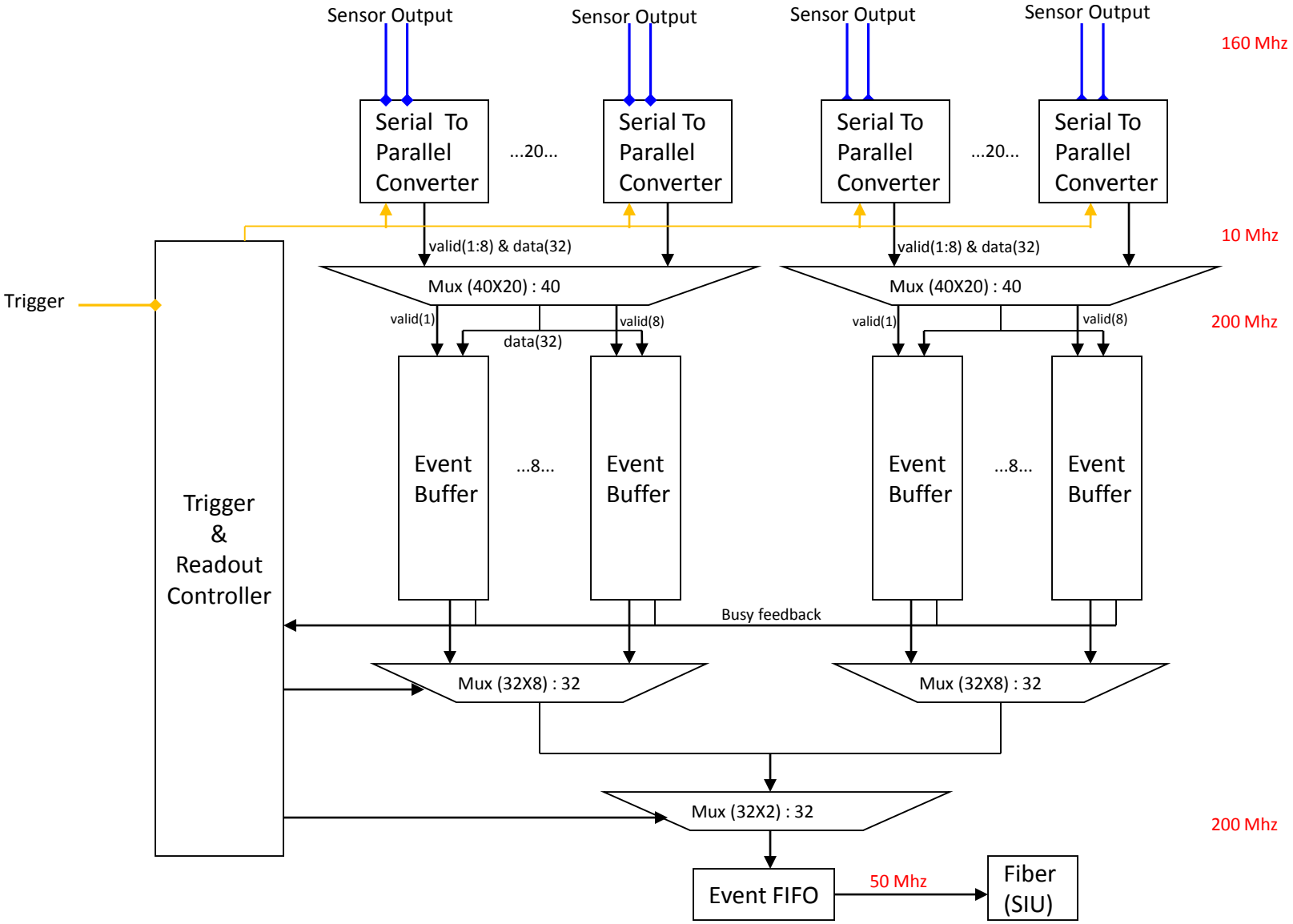
- 40 sensors per RDO = 80 data LVDS pairs at 160 MHz
- Data consists of bit-serially transmitted run-length encoded hit addresses
- Average trigger rate in excess of 1kHz
- Data generation speed (40 sensors x 160MHz x 2 = 12.8 Gb/s) must be reduced to fiber speed (2Gb/s)
- RDO burst (buffer) capability must match TPC RDO capability (1 event every 50 µs in bursts up to 8 events) in order to not increase the DAQ dead time
- Each trigger will result in a separate event containing a full frame to DAQ:



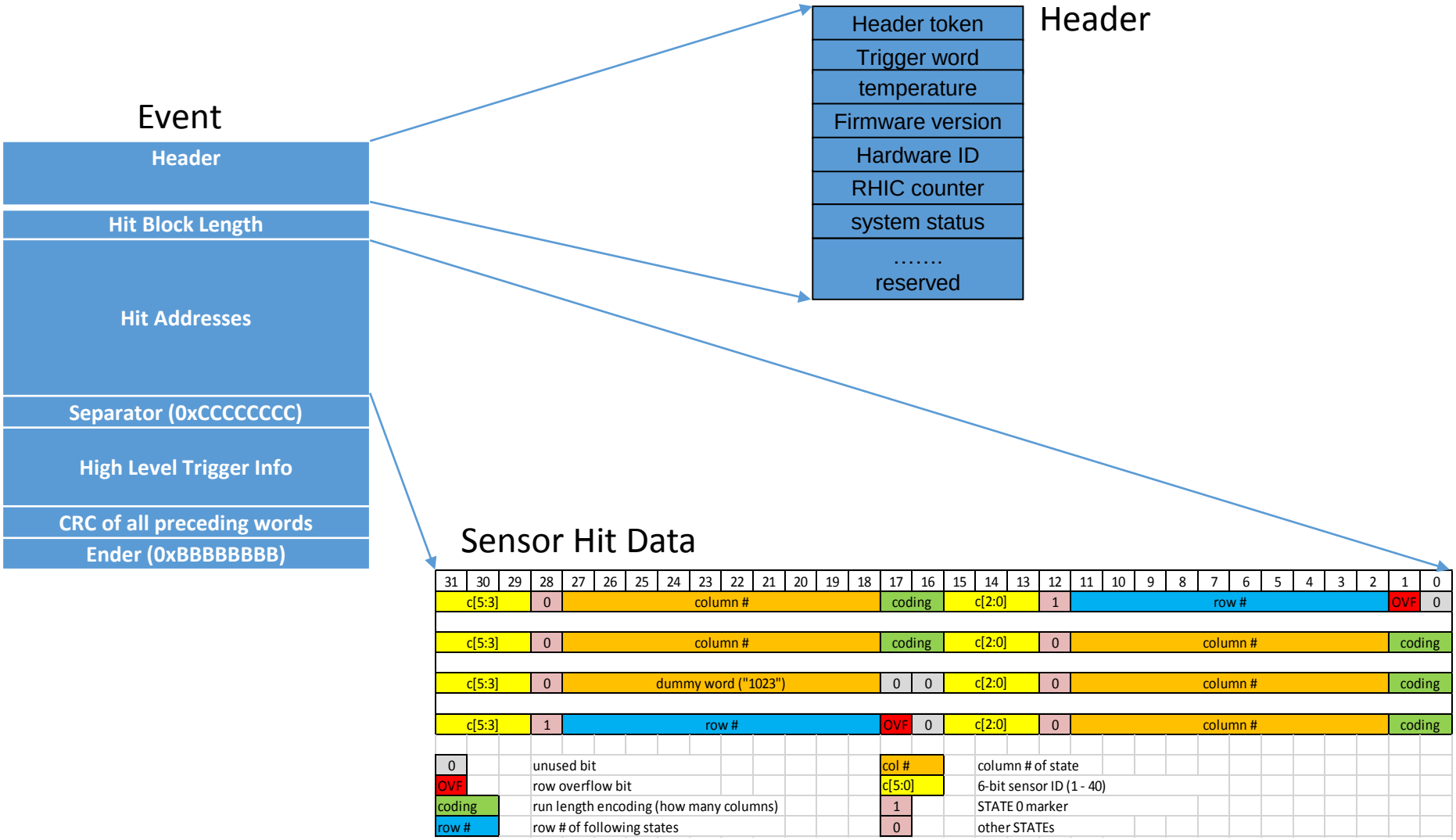
Firmware Architecture



Firmware: Event Readout Module

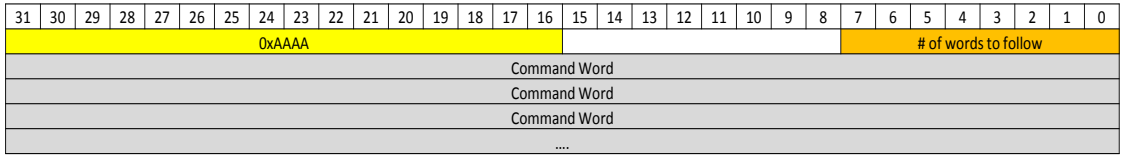


PXL DAQ Data Format

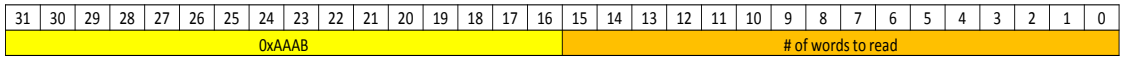


USB Protocol

- FT2232H chip's FIFO interfaces to FPGA Firmware
- Two levels of protocol: USB-FPGA low level, FPGA High Level Protocol
- Low Level Protocol: Separate "WRITE" and "READ" transaction to 2 Firmware FIFOs



WRITE Transaction



Start of READ Transaction

- High Level Protocol:
  - 32bit "Command words" interface to "memory-mapped" 16-bit registers
  - "WRITE" command word: set configurations or start actions
  - "READ" command word: results in Data in "READ" FIFO, which can then be read with a READ low-level transaction

Command Word Format:

4bit control
31 READ/NOT-WRITE
30-28 not defined

12bit address

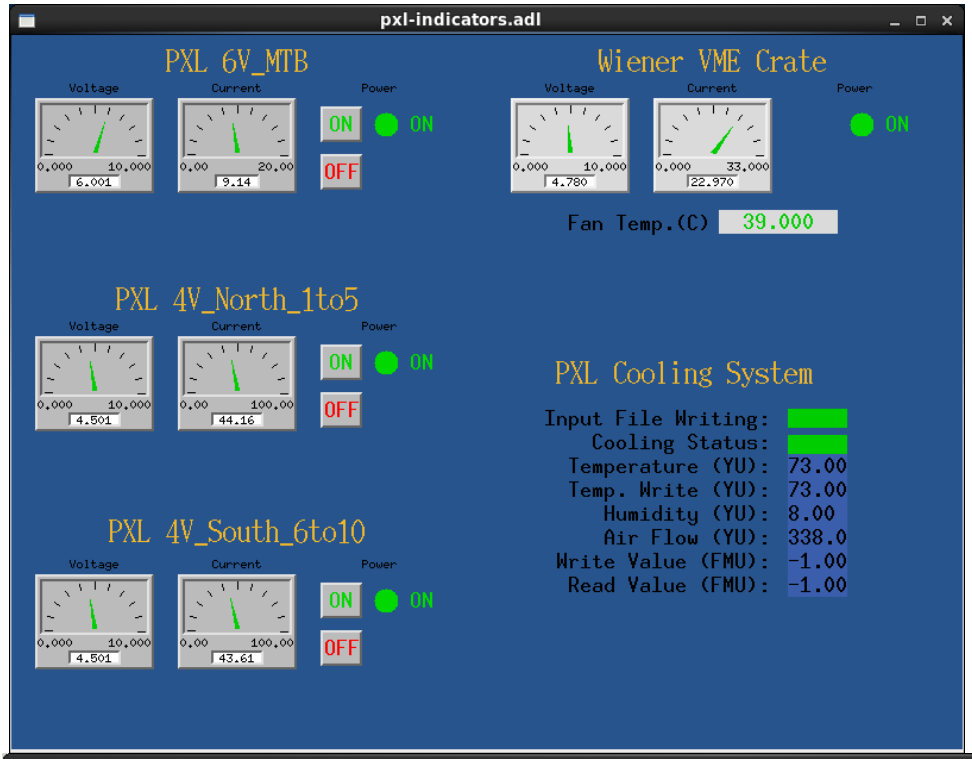
16bit data

USB Software Interface

- Lowest level interface via libD2xx or lib_ftdi on either Linux or Windows
- Four types of memory mapped registers:
  - “Configuration” (R/W)
  - “Status” (read-only)
  - “Action” (write-only) – start FPGA transactions like JTAG or I2C
  - “Indirect” (R/W) – memory or FIFO interfaces (“Count”, “Address”, “Data”)
- PXL library provides convenience functions in C++ and Python
  - open_ftdi, close_ftdi
  - readReg, writeReg
  - readMem, writeMem
- Python used for scripting and control GUIs
- Interface to STAR Slow controls (EPICS) via EPICS “soft-IOCs” that C++ and Python can read/write

PXL Slow Controls (EPICS and Python)

Power Supply and Cooling Monitor



PXL control GUI

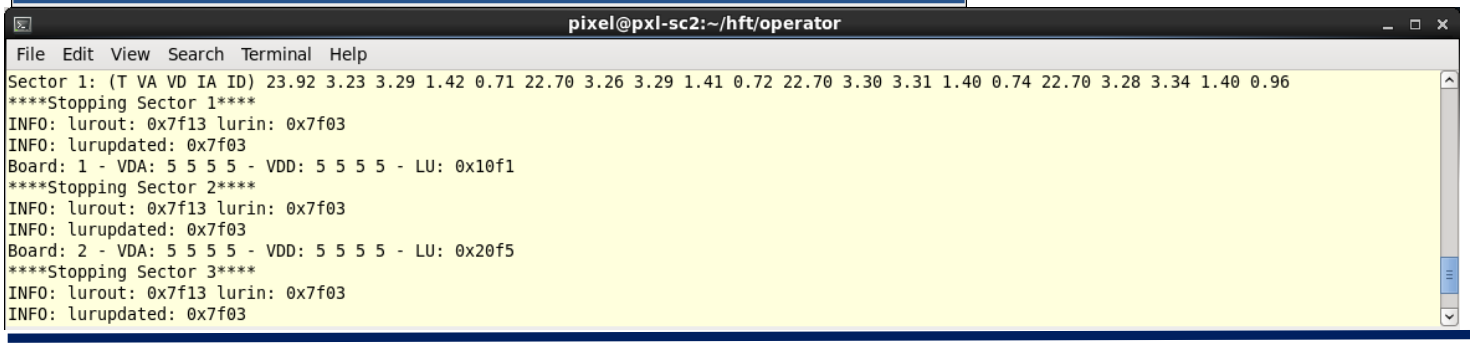
Power up, configure and check for errors

Controlled shut down

Fast reset

Status indicator

Error indicator



Process monitoring terminal

Concluding Remarks

- Readout Performance:
  - Readout through DAQ tested up to ~3 kHz (limit of trigger system)
  - Typical event rate during 200 GeV Au-Au ~ 1kHz with <5% PXL dead time
  - Typical Au-Au PXL data rate about 120 MB/s
- PXL operation highly scripted, very little shift operator intervention needed (mostly just turning PXL on and off)
- Latch-up events cleared automatically by RDO firmware
- Electronics was used successfully during STAR Run 14 and Run 15
- More than 1B events taken each run, which allowed STAR to perform direct topological reconstruction of charmed hadrons

Thank you for your attention