Charge Collection Properties on a Depleted Monolithic Active Pixel Sensor using a HV-SOI process

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ACKNOWLEDGMENTS:

T. Hemperek, H. Krueger, T. Kisishita, N. Wermes for useful discussions,
M. Cerv, B. Ristic and M. Kocian for their technical support at the test beam

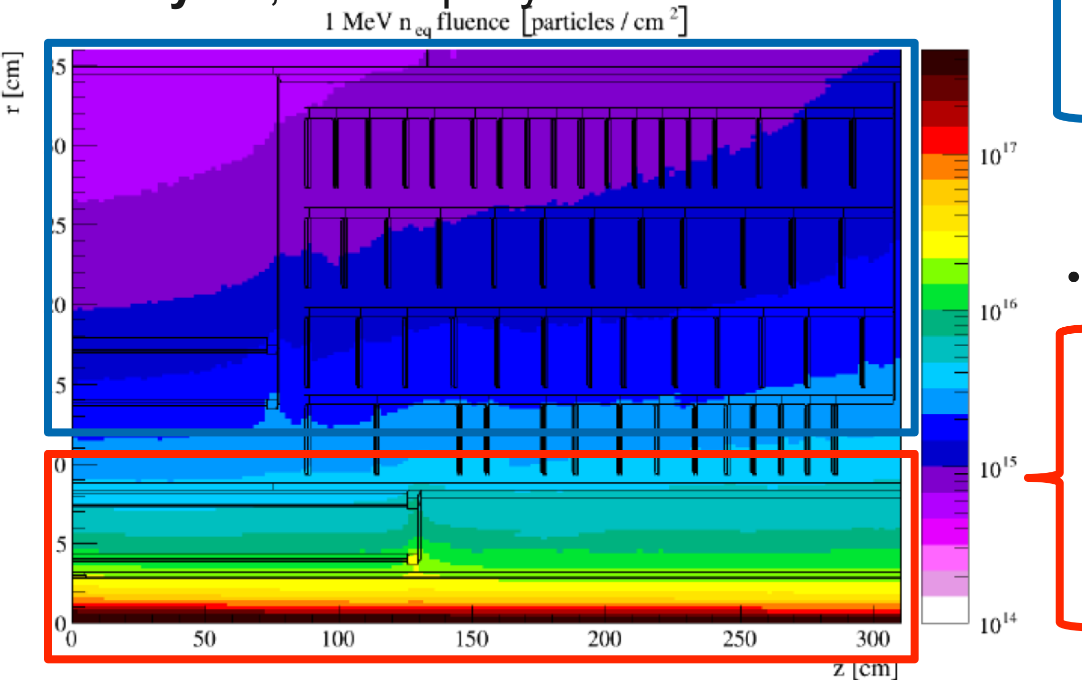
Outline

- Possible application: ATLAS ITK
- Introduction to SOI DMAPS
- Laboratory measurements
    - Radiation hardness to TID up to 700 Mrad
    - Drift, diffusion contributions on silicon bulk
    - Acceptor removal effect
    - eTCT measurements
- Test beam Results

Possible application: ATLAS ITk

Layout:

- New all silicon Inner Tracker in development for ATLAS in HL-LHC
- Layout in discussion, likely **4-6 pixel layers**, 4-6 strip layers



- Outer Layers
  - Occupancy: 1 MHz/mm^2
  - TID: 50 Mrad
  - NIEL: 1x$10^{15}n_{eq}/cm^2$
  - Area: 10.8 to 20.8 m^2 of silicon
  - → **Price + Production Schedule crucial Challenges → Industrial, monolithic**
- Inner Layers
  - Occupancy: 10 MHz/mm^2
  - TID: 1 Grad
  - NIEL: 2x$10^{16}n_{eq}/cm^2$
  - Area: 0.8 m^2 of silicon
  - **→ Challenges radiation driven → hybrid**

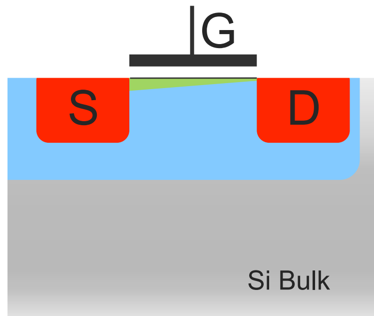
→ Investigate Depleted Monolithic Active Pixel Sensors as option for ITk outer pixel layers

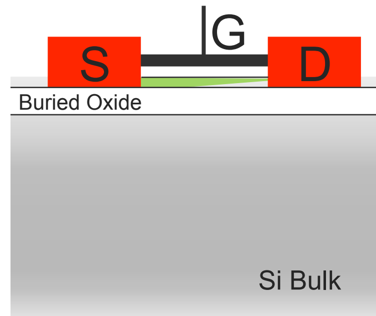
Introduction to Silicon On Insulator (SOI)

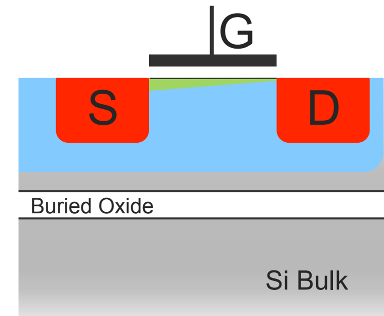
- Bulk-transistor

Fully Depleted SOI-, transistor

Partially Depleted SOI- / Thick film transistor







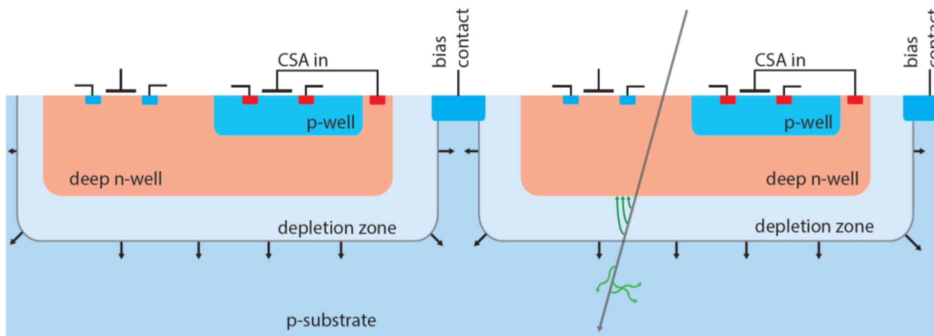
- Channel formation in silicon bulk
- Deep wells used for full CMOS technology

- Ultra-thin transistor body ~O(40 nm)
- Body fully depleted.
- Si Bulk isolated from transistors

- Partially depleted body ~O(several μm)
- Body isolated and floating wrt. bulk.
- Transistors can be shielded from BOX using deep wells
- Full CMOS technology

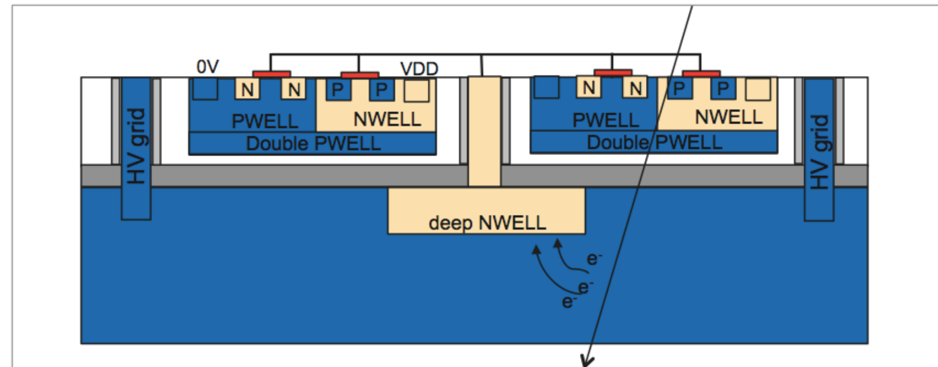
Motivation for XFAB SOI process

HV / HR CMOS proccesses:



- Electronics (partially) shielded from substrate by well structure
- Large fill factor
  → short drift distance
  → high radiation hardness
- Large sensor capacitance + crosstalk (Large well, several well junctions)

Partially depleted XFAB SOI process:

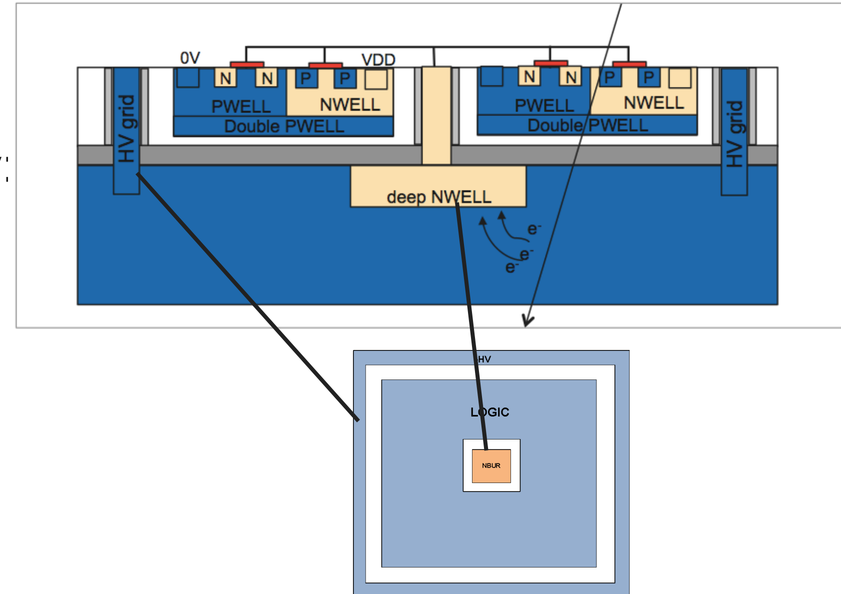


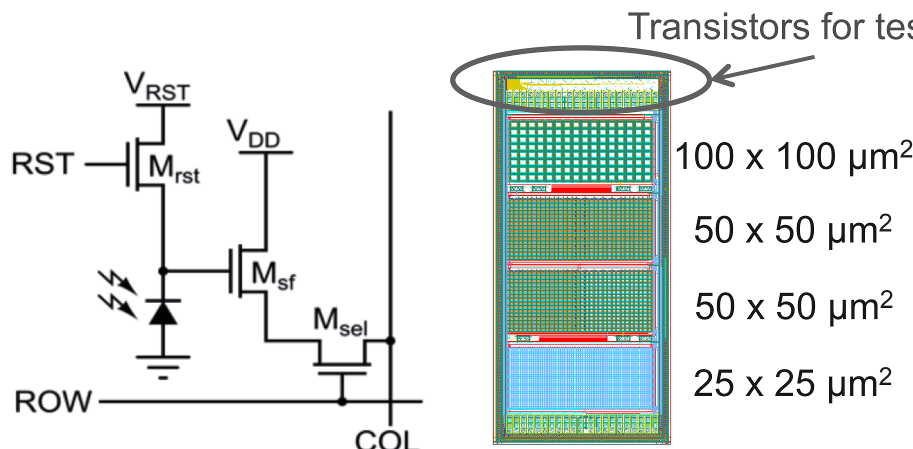
- Electronics isolated from substrate by BOX
- Small charge collecting electrode
  → But no „competing wells“
- Double wells in transistor body + particular geometry
  → No back-gate effect and high rad. hard. expected
  → Full CMOS logic
- Full depletion possible

Designed by T. Hemperek, T. Kisisita and H. Krüger
[T. Hemperek et al.: http://dx.doi.org/10.1016/j.nima.2015.02.052]

XTB01 prototype

- XFAB Trench SOI 0.18 µm CMOS low-power 1.8/5.0V
- P-type bulk, 4 metal layers
- Wafer size: 8“
- Relatively high handling wafer resistivity:
  - 100 Ω cm CZ
  - 1 kΩ cm possible
- Currently no back-processing
  → HV applied from front side
- Size: 5 x 2 mm²
- 3T cell readout





Designed by T. Hemperek, T. Kisisita and H. Krüger
Tested by M. Backhaus, S. Fernandez-Perez, T. Hemperek, T. Kisisita and H. Krüger

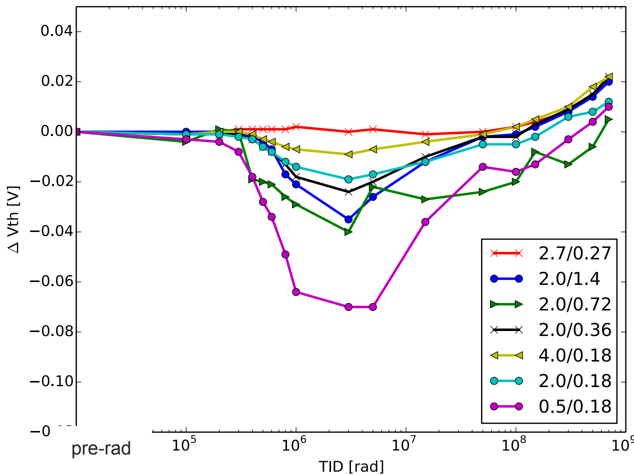
Acknowledgments to F. Faccio , M. Barbero

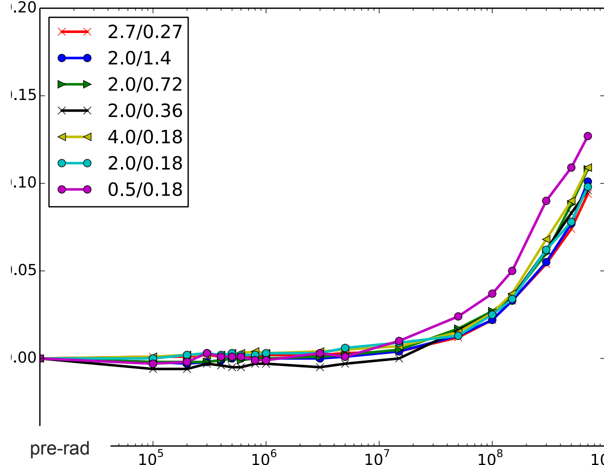
Highlights from TID radiation hardness

(S. Fernandez-Perez, doi:10.1016/j.nima.2015.02.066)

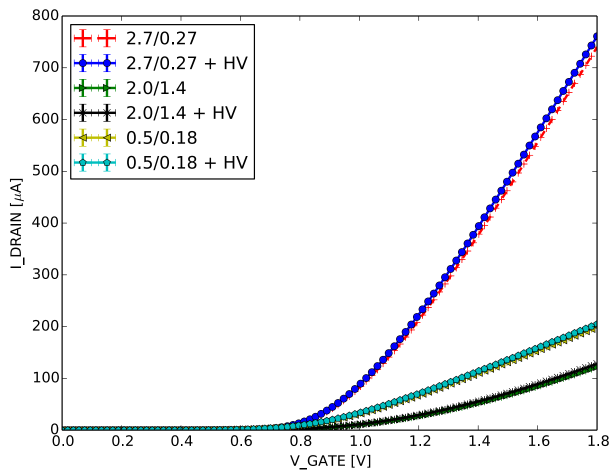
NMOS

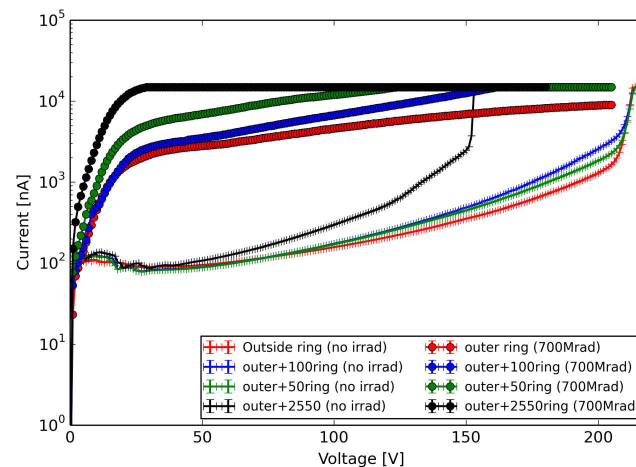
PMOS

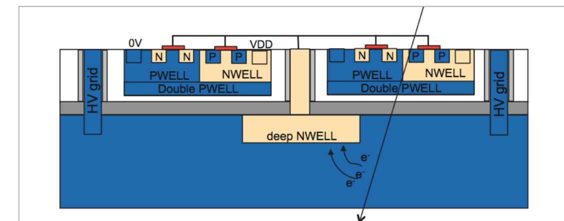




- Transistors radiation hardness proven up to 700 Mrad
- NMOS and PMOS with similar response to TID as non SOI technology, esp. IBM 130 nm (FE-I4, ATLAS IBL R/O chip)
- Back Gate effect not observed





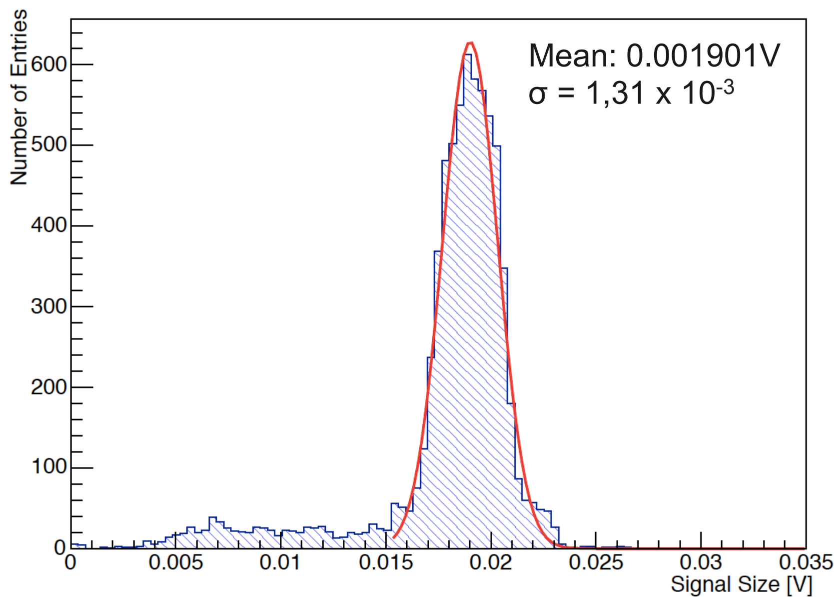


- Accumulation layer below BOX forms due to positive charge generation
- Channel from bias grid to charge collecting n-well
- “Leakage current” high after TID

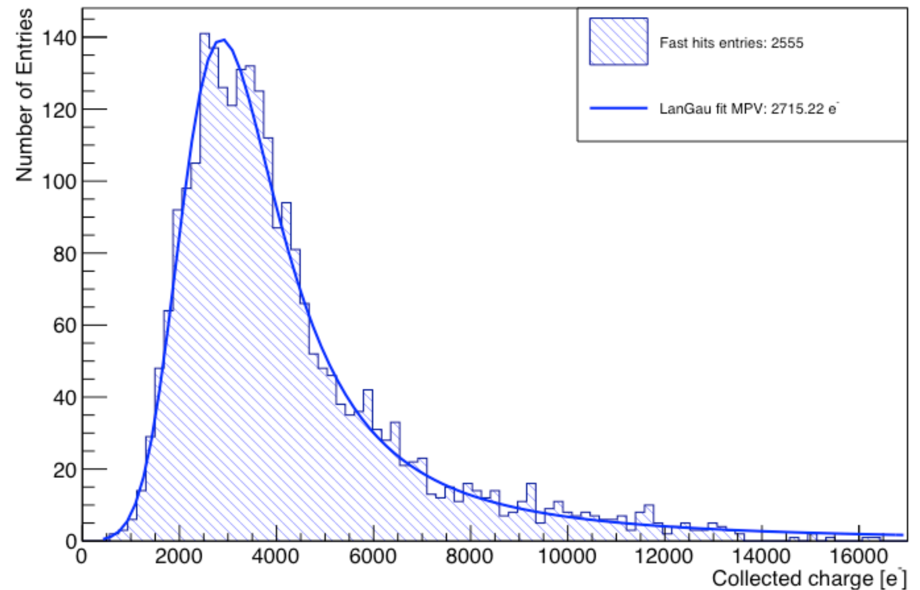
Highlights from Charge collection properties (1 / 3)

(S. Fernandez-Perez, et al. to be submitted by this month)

^{55}Fe – 50 x 50 µm^2 pixel -100V at 0°C



^{90}Sr – 50 x 50 µm^2 pixel -120V at 0°C



→ Calibration factor: K=(11,59 ± 0,79$_{(sys)}$ ± 0,01$_{(stat)}$) x 10^{-6} V/e

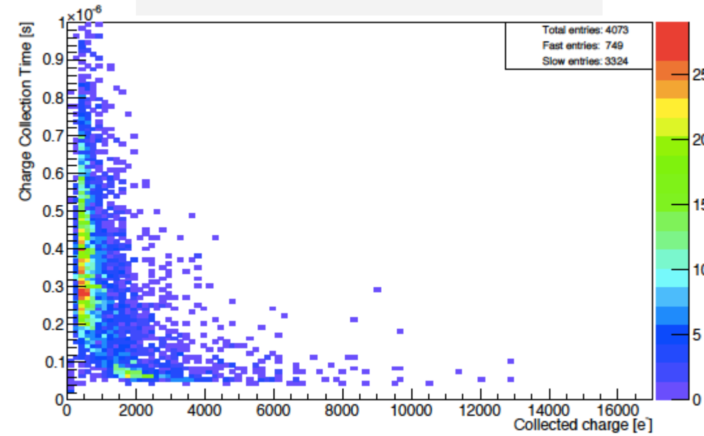
→ Depletion depth at 120 V: (33,9 ± 2,7) µm

→ SNR: 22

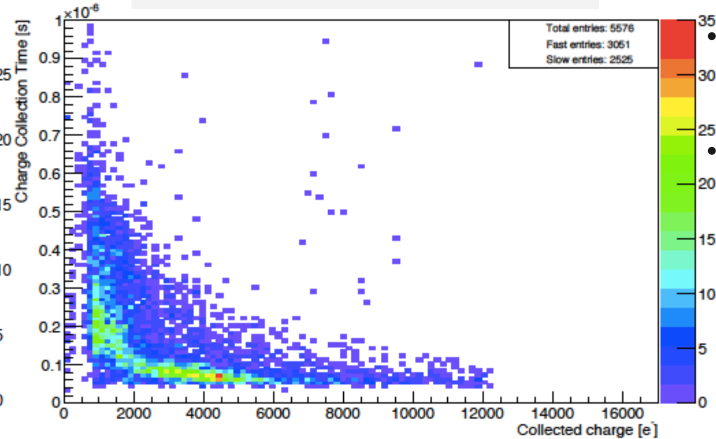
Highlights from Charge Collection Properties (2 /3)

(S. Fernandez-Perez, et al. to be submitted by this month)

^{90}Sr -30V at 0°C



^{90}Sr -140V at 0°C

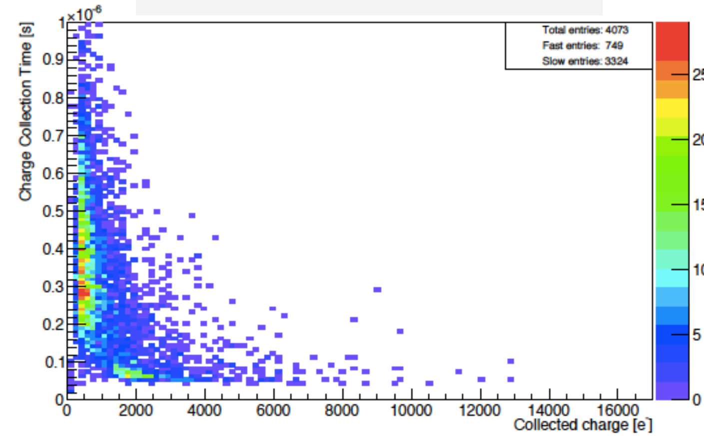


- By increasing the bias voltage the amount of slow collected hits reduces.
- By increasing the bias voltage the amount of fast collected hits increases.

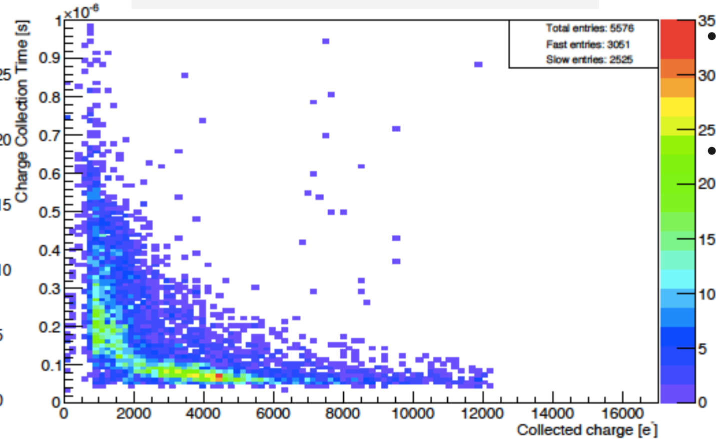
Highlights from Charge Collection Properties (2 /3)

(S. Fernandez-Perez, et al. to be submitted by this month)

^{90}Sr -30V at 0°C

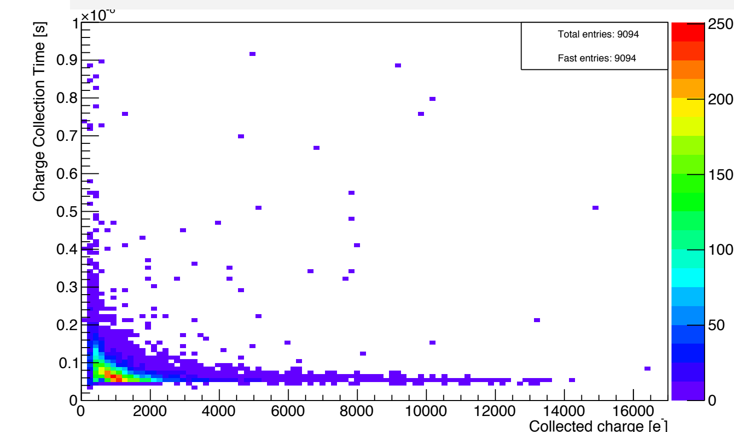


^{90}Sr -140V at 0°C



- By increasing the bias voltage the amount of slow collected hits reduces.
- By increasing the bias voltage the amount of fast collected hits increases.

Neutron irraditated 1 x 10^{13} n_{eq}/cm
^{90}Sr -30V at -30°C

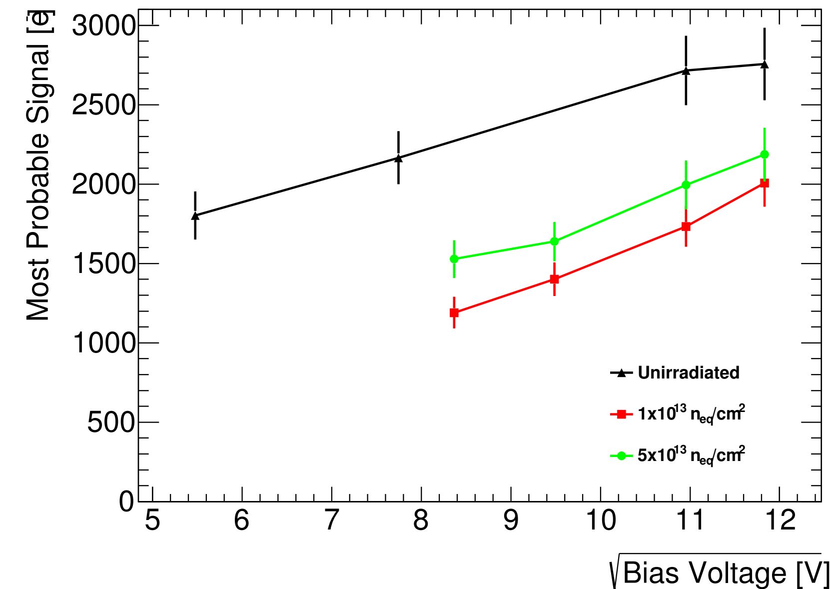


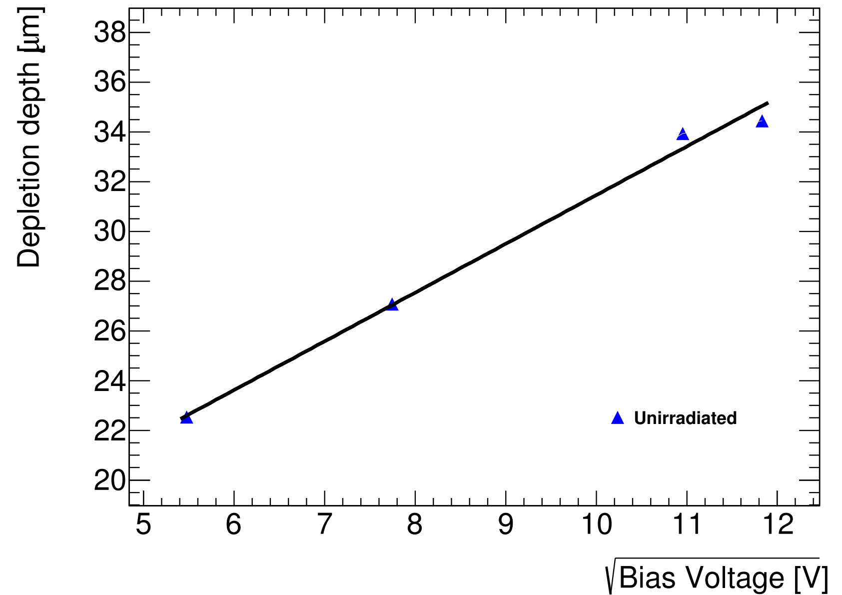
- The slow collected hits disappear for the irradiated samples

→ Drift and diffusion are observed in the collected charge and can be separated !!

Highlights from Charge Collection Properties (3 /3)

(S. Fernandez-Perez, et al. to be submitted by this month)



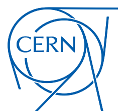


- Sample at 5 x 10^{13} n_{eq}/cm^2 collects more charge than sample at 1 x 10^{13} n_{eq}/cm^2 at same conditions.
- Might be due to acceptor removal effect.

- The depletion depth increases linearly to the square root of voltage, as expected

- Acceptor removal effect observed in 10-20 ohm cm → Igor Mandic et al,. in ITK September 2015:

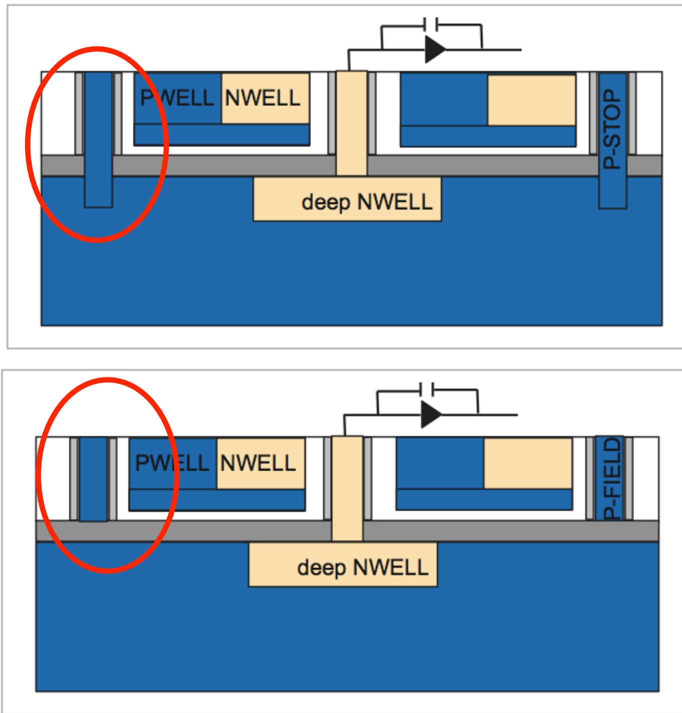
https://indico.cern.ch/event/369608/session/6/contribution/35/attachments/1155045/1659892/ITK_sept2015_mandic.pdf

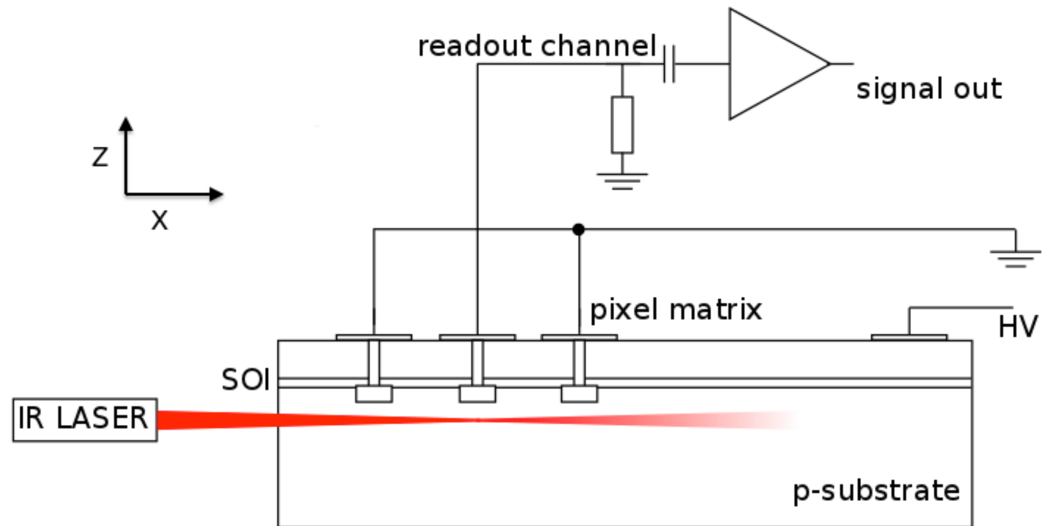


Highlights from eTCT measurements (1 / 2)

(S. Fernandez-Perez, et al. to be submitted this month)

XTB02 prototype



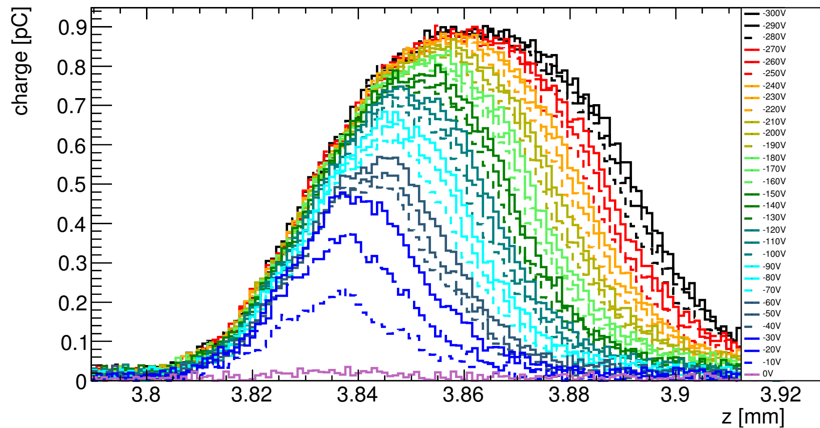


- Leakage decreases by a factor of ten with respect to XTB01
- Breakdown increases to above 300V (see more in backup)

Highlights from eTCT measurements (2 / 2)

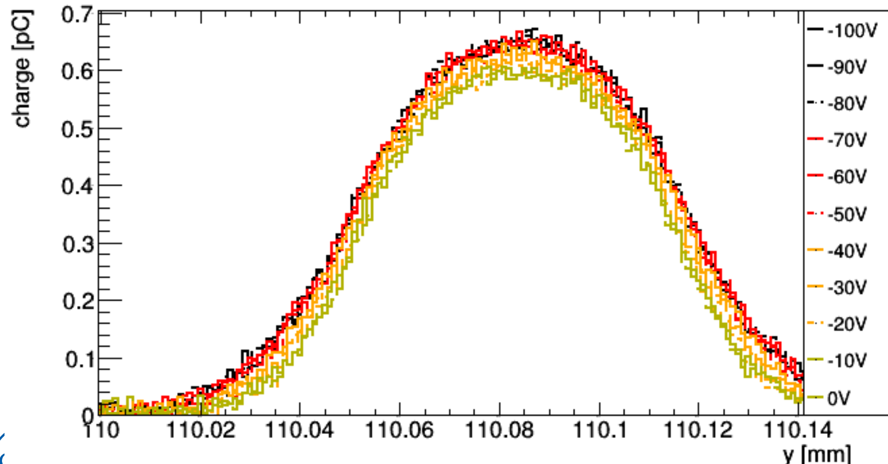
(S. Fernandez-Perez, et al. to be submitted this month)

Z direction (p-field floating)



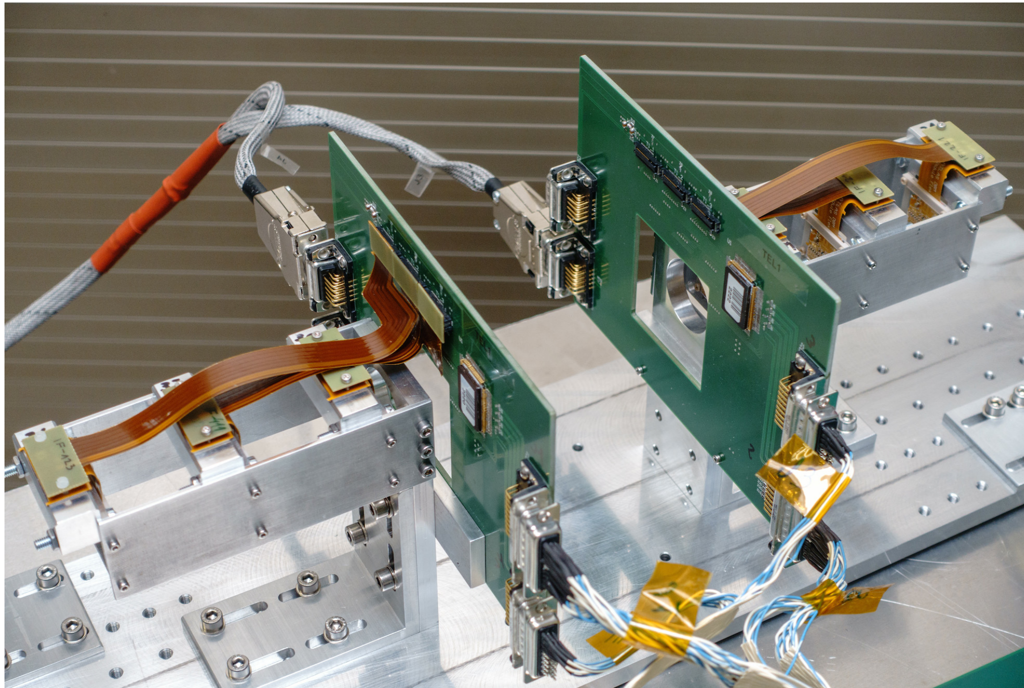
- Depletion depth grows in bulk as expected (agrees with source measurements), no in Y direction
- Depletion in lateral direction (Y axis) under investigation

p-field biased

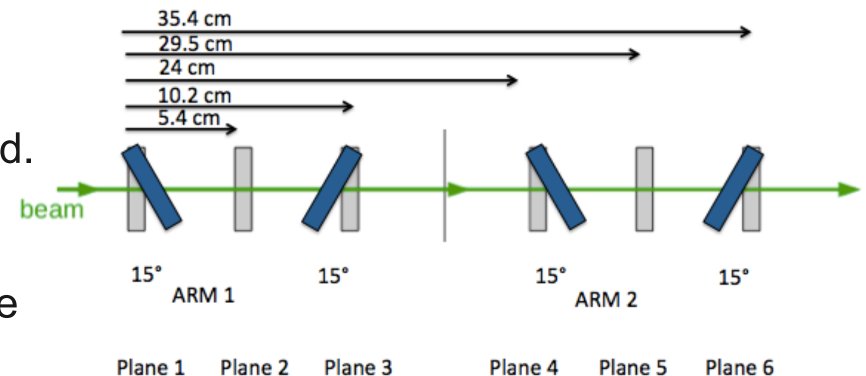


- P-field and p-stop structures influence the charge collecting properties when biasing
  - → *y* direction 5 µm increase for 100V
  - → no change in z direction
- Being investigated with TCAD

SPS Test Beam

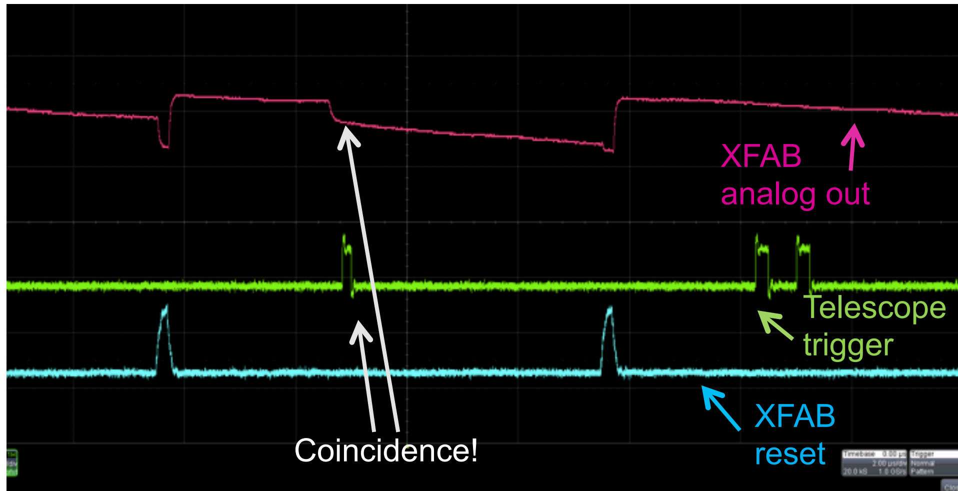


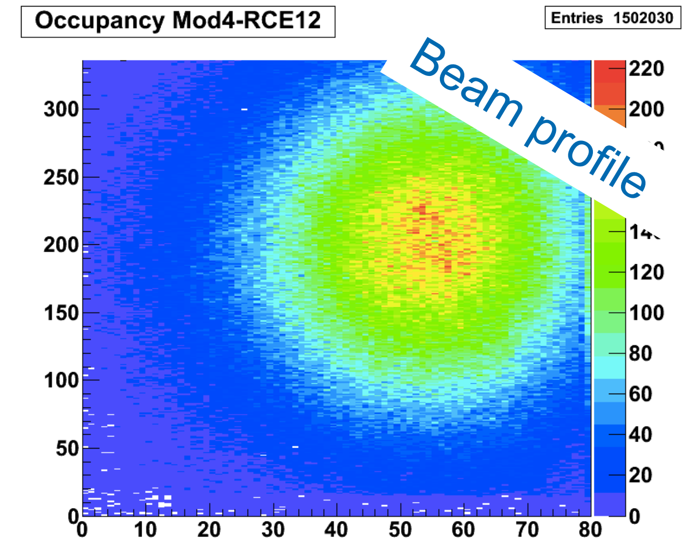
- AIDA SBM FE-I4 telescope
- 6 FE-I4 planes with 50 x 250 μm^2 pixel
- Every second plane is rotated by 90°→ resolution improvement

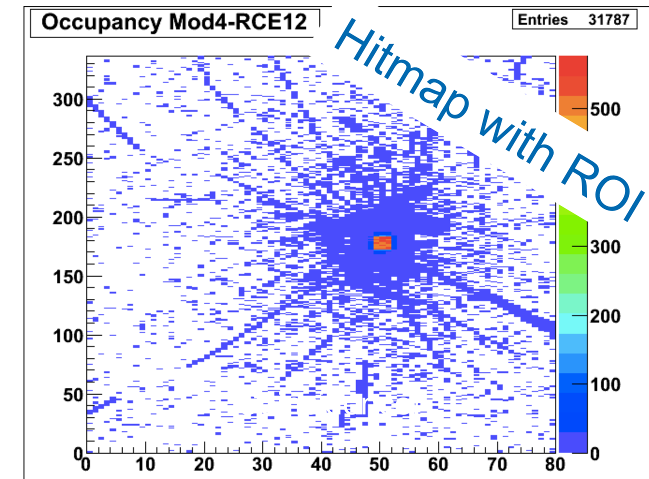


- Bias voltage was varied for 60-V, 90-V, and 120-V.
- Reconstruction + analysis (Judith) performed.
- Single pixel readout (50 x 50 μm^2) with oscilloscope
- Computed residuals and the efficiency for the pixel

SPS Test Beam: First beam particles detected







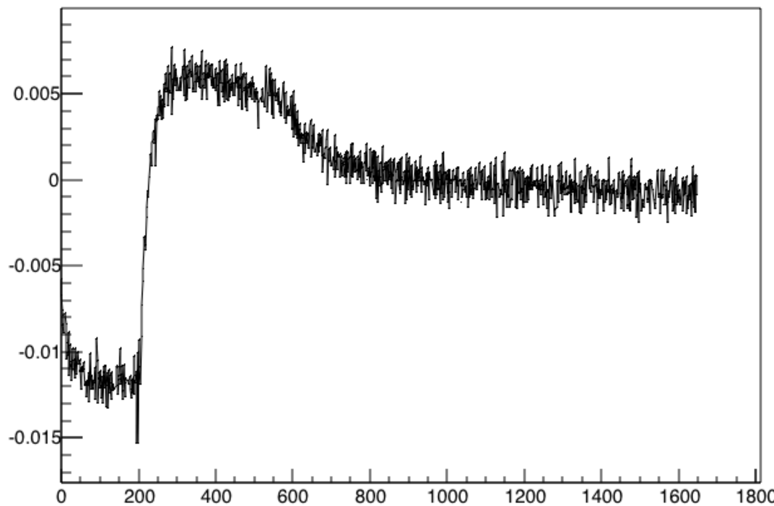
- High beam rate needed due to small sensitive area
  → very careful alignment done, focused beam
- Used oscilloscope trigger on hits in XFAB to define ROI in telescope
- Rate in order of 5 - 10 hits per spill in XFAB, mostly two spills per 36 seconds
- Took about 10M events to ensure 20.000 events in XFAB

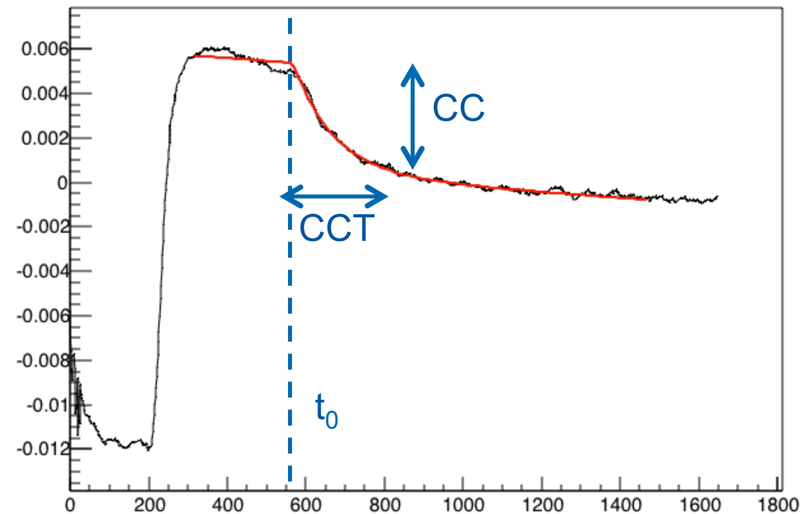
SPS Test Beam: output pulse shape reconstruction R/O

- Implemented 3TcellAnalyser (used in sources measurements too)
  → Extract additionally the charge collection time, hit detection time

$$f(t)\begin{cases} t \le to & f = a + m\,(t - to) \\ t > to & f = a + m\,(t - to) + b\,(e^{\frac{t-to}{c}} - 1) \end{cases}$$

b: charge collection (CC)
c: charge collection time (CCT)
t_o: hit detection time

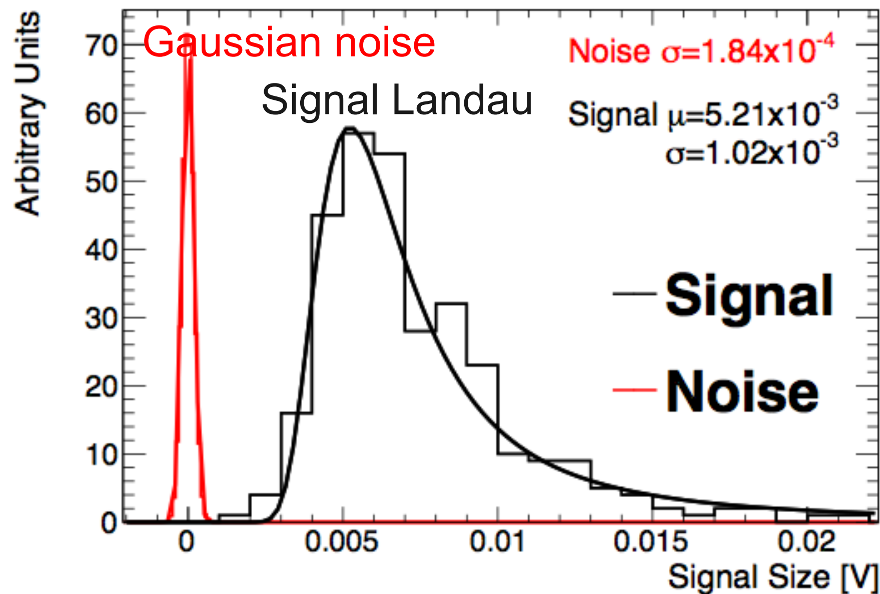




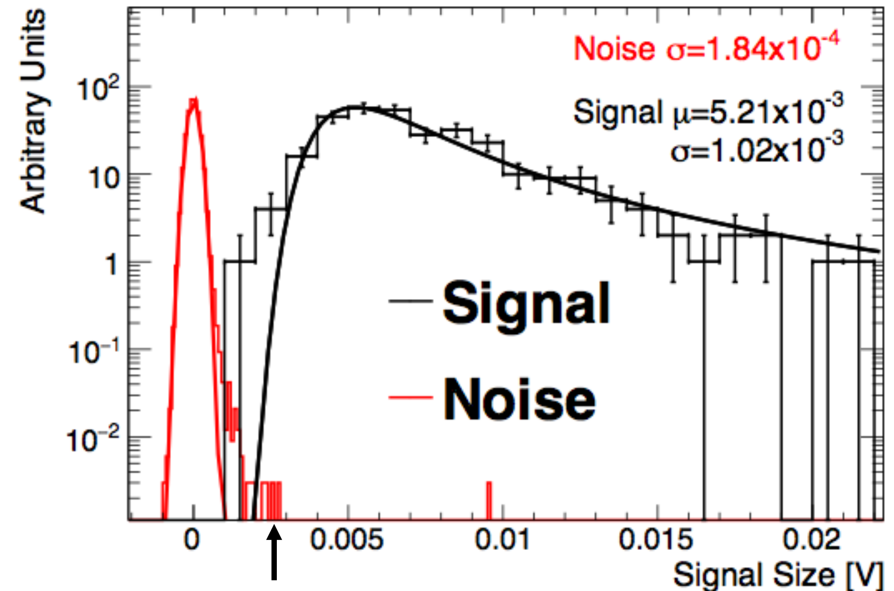
Signal Versus Background

Signal 120V @ room T
(Single run, 150.000events)

- **Noise** is defined as all readout not identified as a hit (fit with a Gaussian)
- **Signal:** all identified hits using the algorithm on the previous slide (fit with a Landau)
- Signal-to-noise (SNR): 22
- Select DUT hits with V>~0.035 (choice depends on the bias voltage)



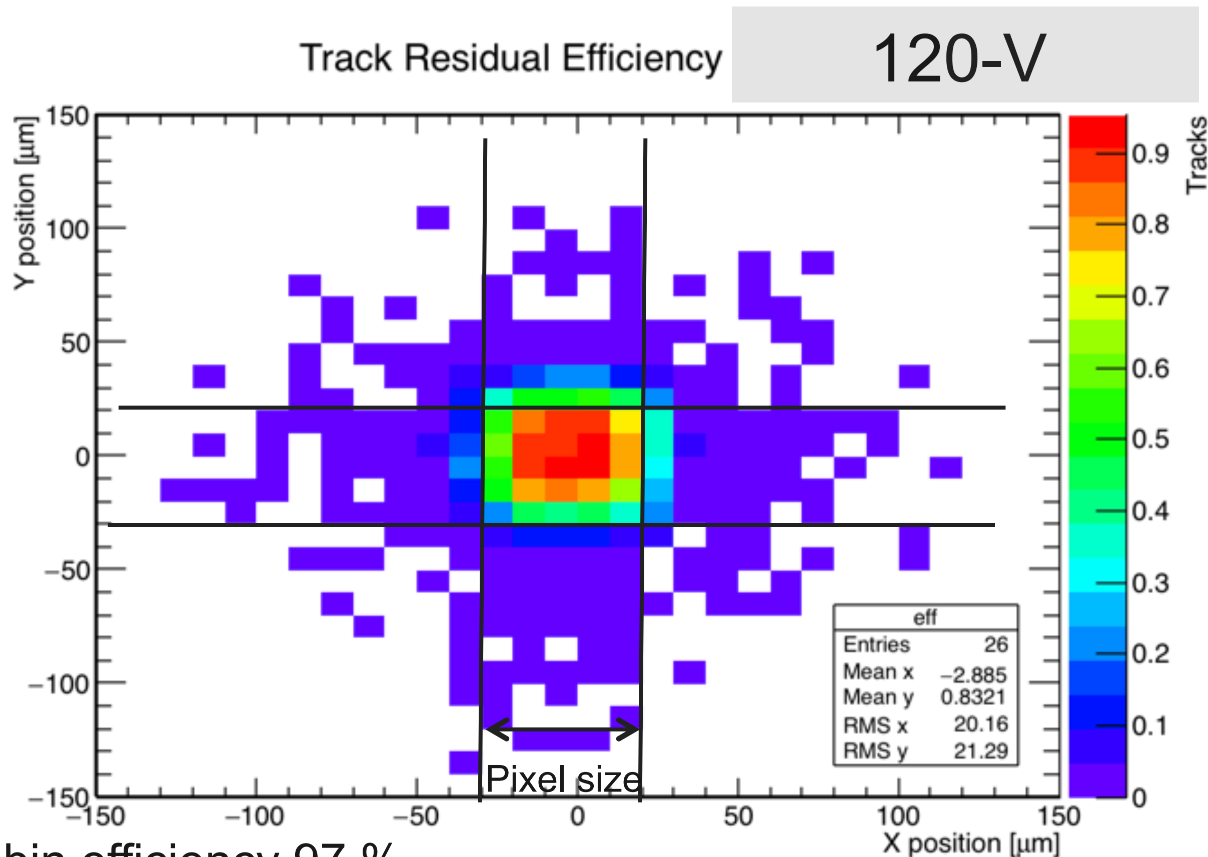
Normalized to roughly the same height



Some non-Gaussian tails (likely small signals)

DUT efficiency

- Efficiency of the DUT with **no cuts** on the clusters

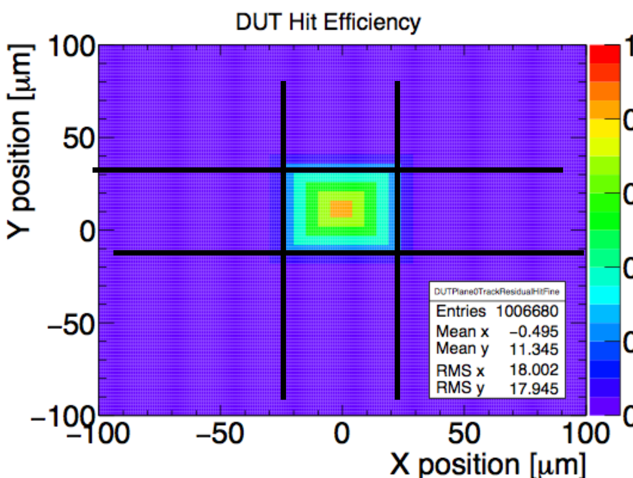


- Maximum bin efficiency 97 %
- Central part of the pixel is 20% more efficient than outside part → charge sharing
- The pixel collects tracks from neighbor pixels
  → diffusion contribution: they disappears by cutting on CCT or T_0

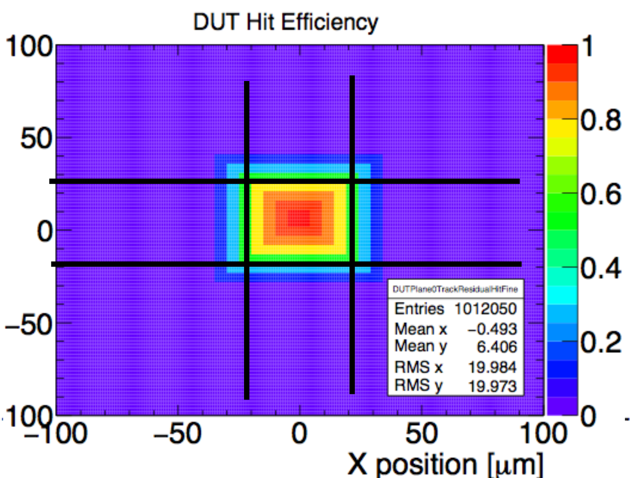
DUT efficiency

- Efficiency of the DUT with **no cuts** on the clusters
- For the 60, 90-V and 120-V, the edges are averaged in rings to increase the statistics

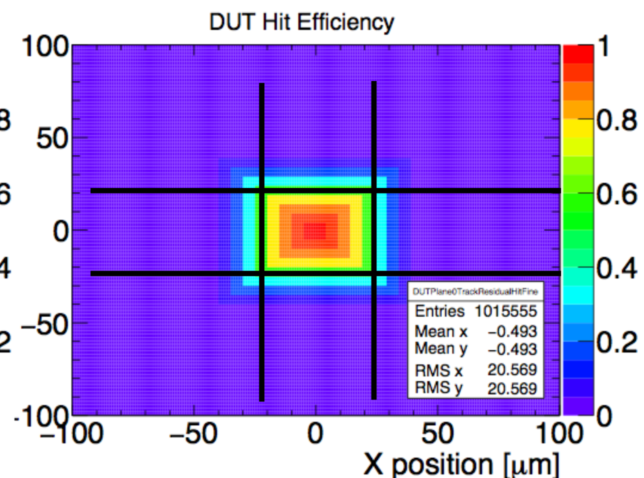
60-V



90-V



120-V

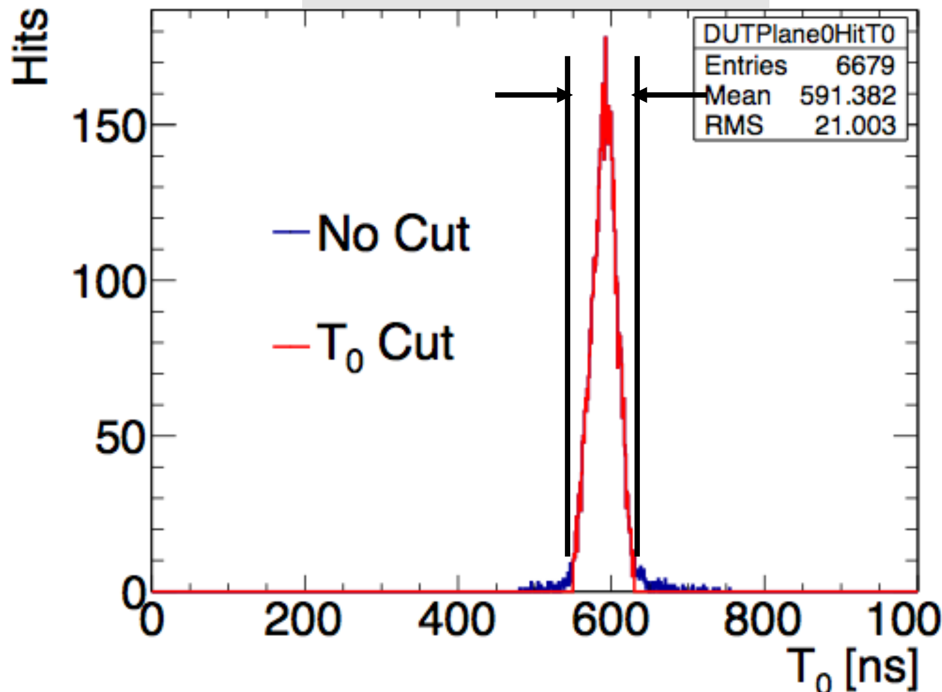


- ✓ The outer pixel efficiency size grows
- ✓ The inner pixel efficiency increases
- ✓ Outline the approximate pixel size

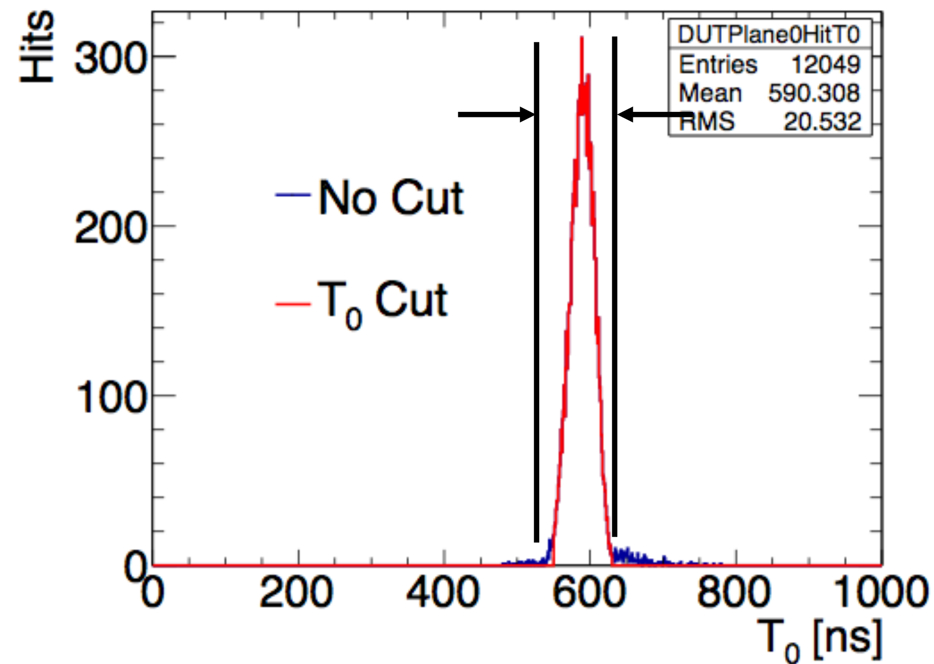
Example of the Cut on T_0

- Different cuts can be implemented to invalid events.
  → charge collection time (diffusion) , T_0
- T_0 should be always at the same time, fixed by the external trigger (600ns)
- Example cut on the T_0 form 550-630 ns

60-V

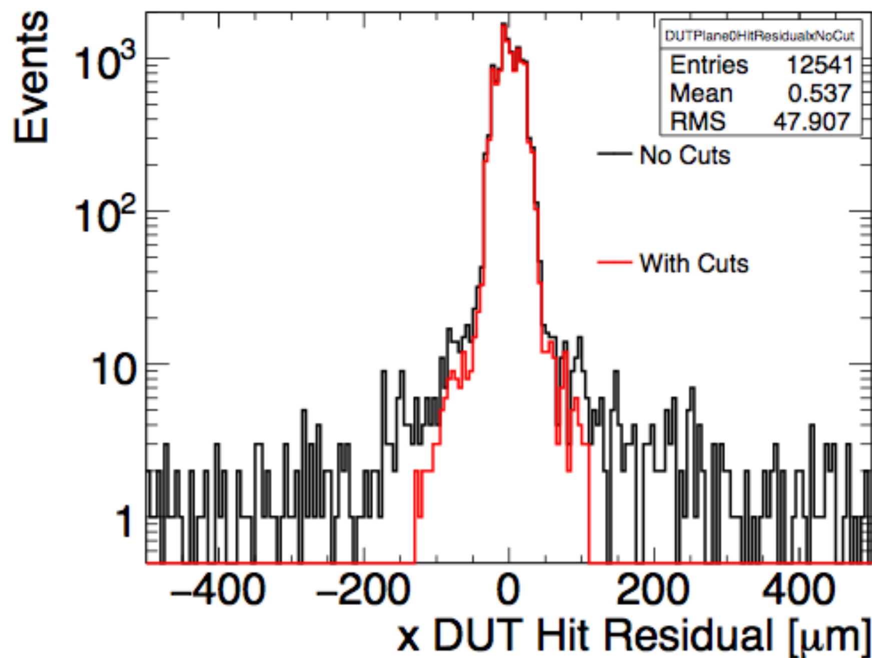


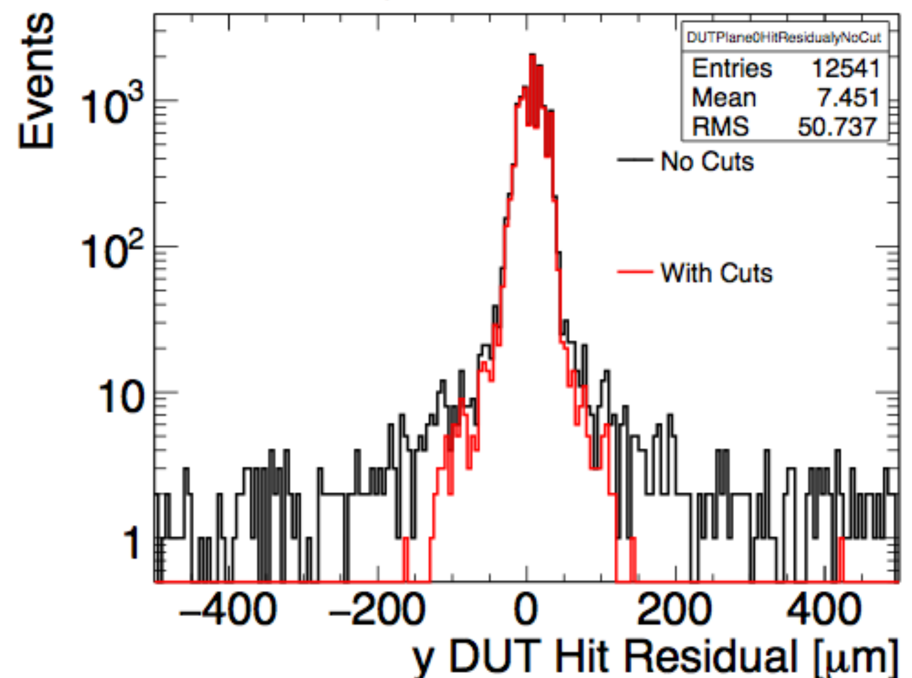
90-V



Difference in Residual After T_0 Cut

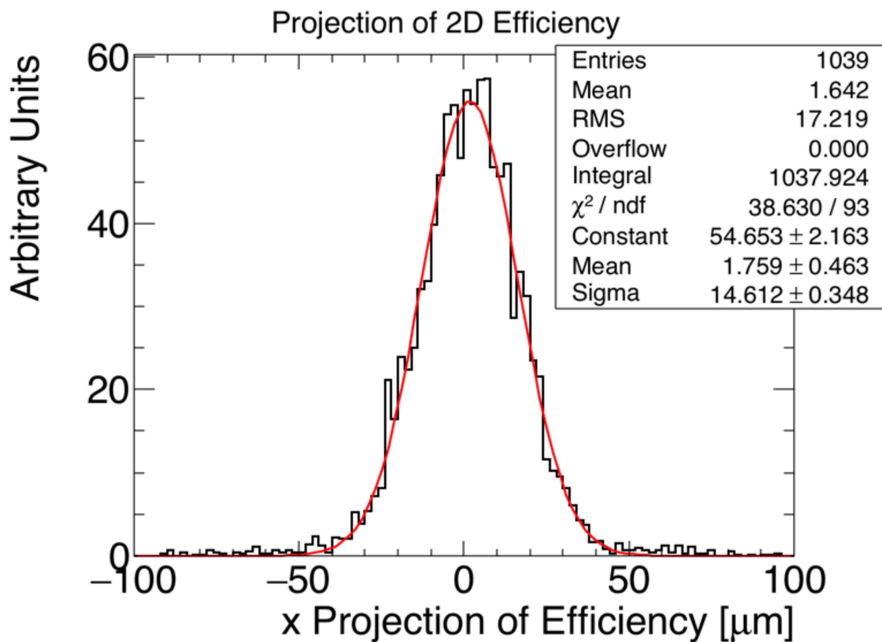
- Hit to track residual before and after cutting on T_0 of the clusters for the 90-V bias
- T0 cut removes almost all hits with a residual of larger than 100 μm

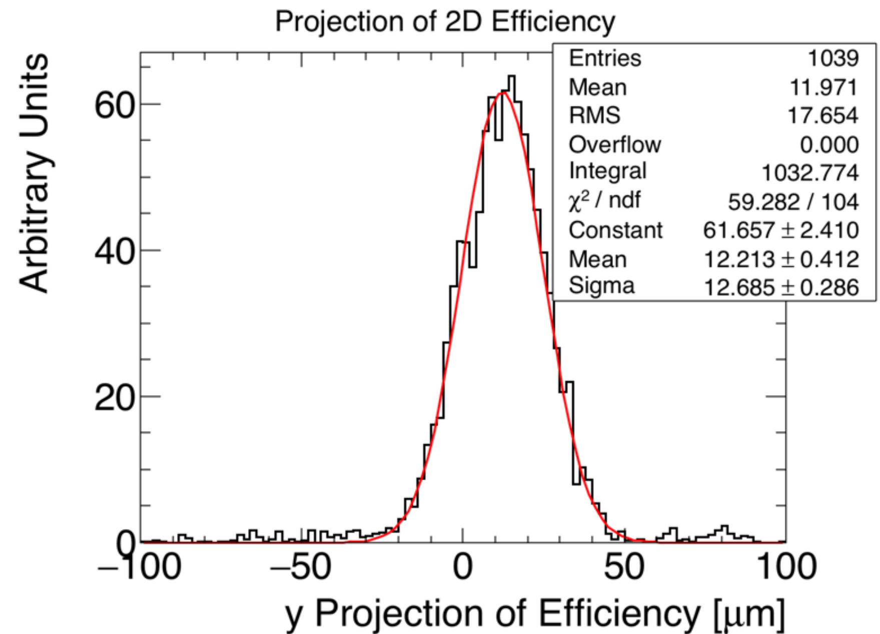




Projected Efficiency

- Efficiency is projected for the x and y directions
- Gaussian width is wider for the x direction (14.6 μm) than y direction (12.7μm)
  → n-well is not square (expected 2-μm bigger in one direction 14μm x 10.5μm)

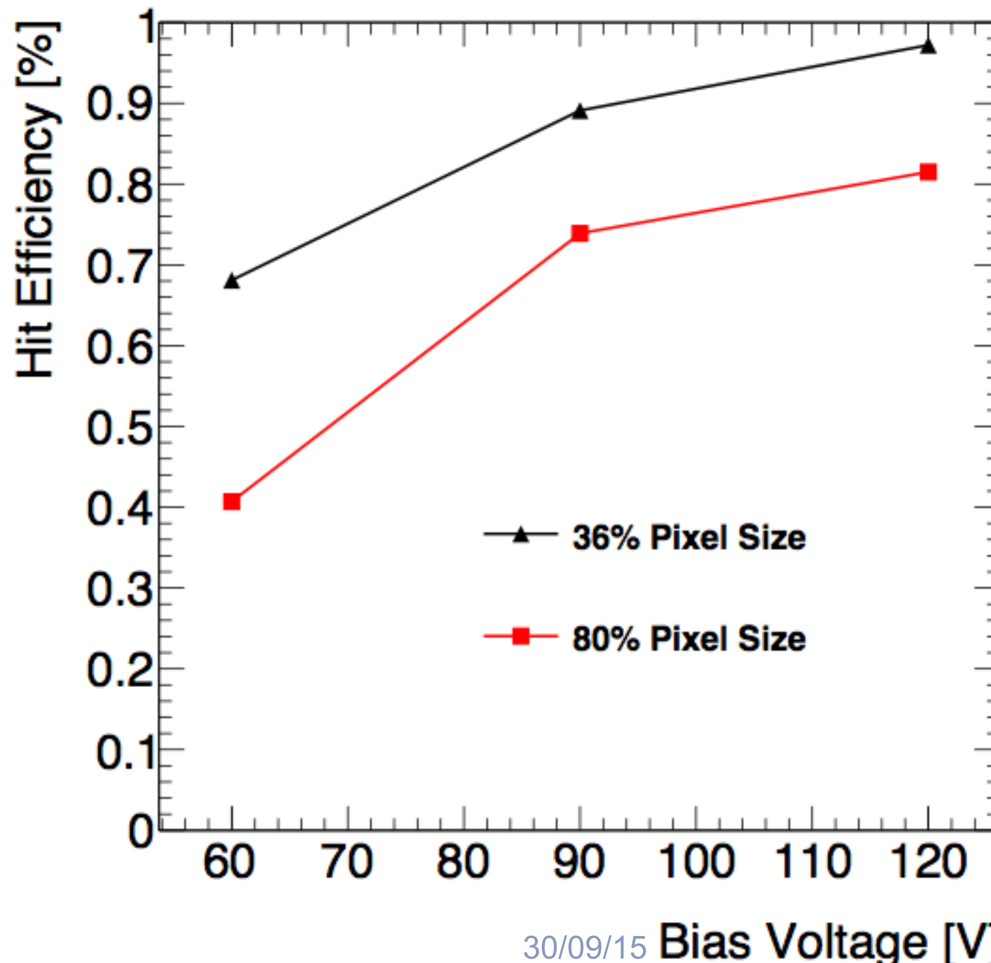




pre-alignment

Efficiency Vs Bias Voltage

- Aligned run by run
- Efficiency is computed for the center 36% and central 80% of the pixel with the T_0 cut.
- Minimum efficiency. We were conservative in the corrections for excluded data



- 97.2% ± 1.3% efficiency at 120V
- The chip stands 200V

Conclusion & Outlook

- XFAB thick film SOI technology extensively investigated on fully monolithic prototype
  - Good electronics radiation hardness
  - No back-gate effect
  - Unexpected high leakage current, intense increase with pos. charge accumulation in the BOX → process change + p-stop / p-field implemented in second prototype
  - Clear ^{55}Fe and ^{90}Sr spectrum up to $5x10^{14}$ n_{eq}/ cm^2
  - Depletion depth grows as expected in depth (sources, eTCT measurements)
  - Possible hints to Acceptor Removal Effect seen → eTCT vs fluence measurements in in coming months in collaboration with I. Mandic et al.

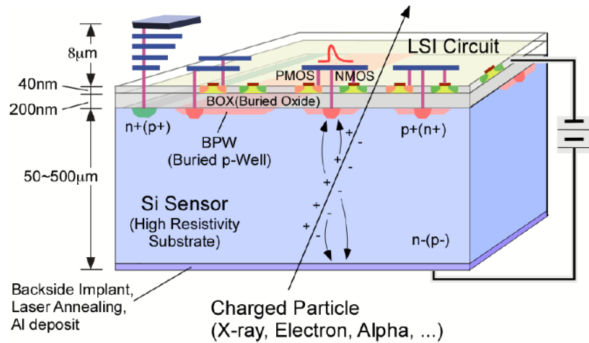
- Test beam studies in unirradiated samples
  - Central 36% of the chip has an efficiency of around 97% @ 120-V
  - Test beam results confirm excellent charge collection properties observed with radioactive sources and eTCT
  - Test beam campaigns in irradiated devices in coming months

- XFAB SOI technology shows promising results for depleted monolithic pixel layers in HL-LHC experiments.

Backup

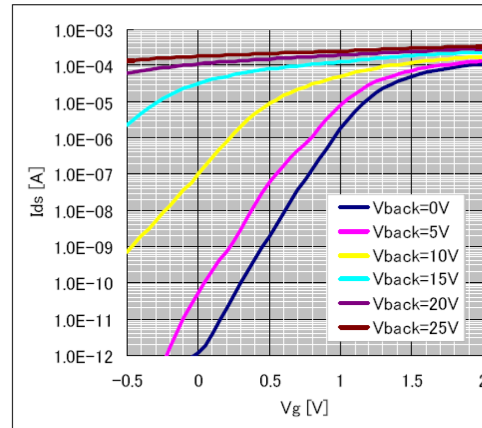
Recent results on SOI

- Big achievements of SOI community wrt. radiation hardness shown [Yasuo Arai, Vertex 2013]:

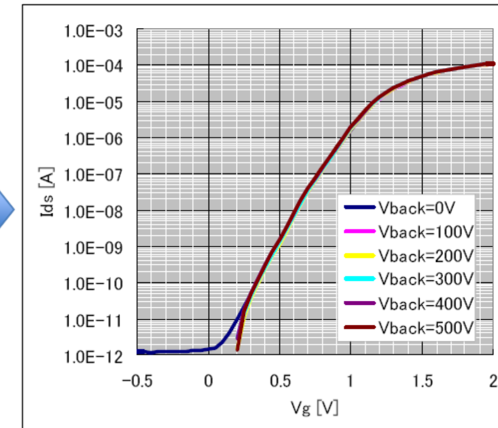


Silicon-On-Insulator Pixel Detector (SOIPIX)

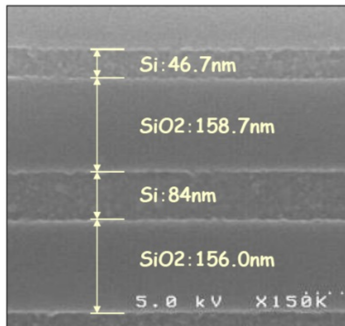
a) Middls-Si Floating

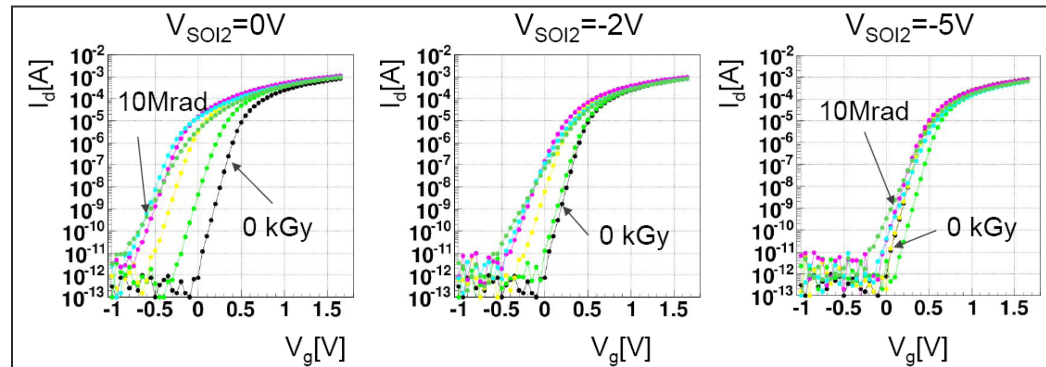


b) Middle-Si = GND



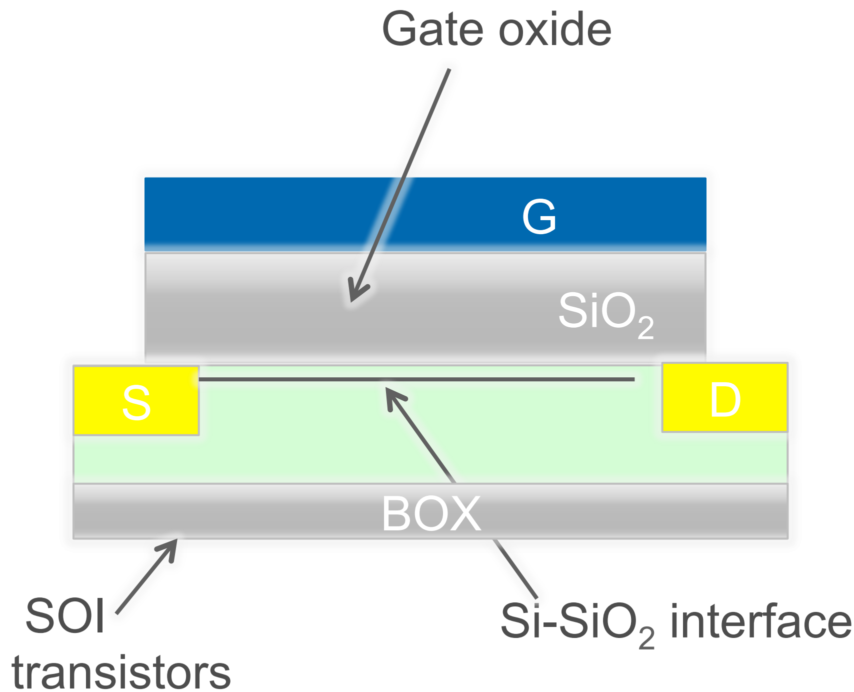
Double BOX SOITEC wafer

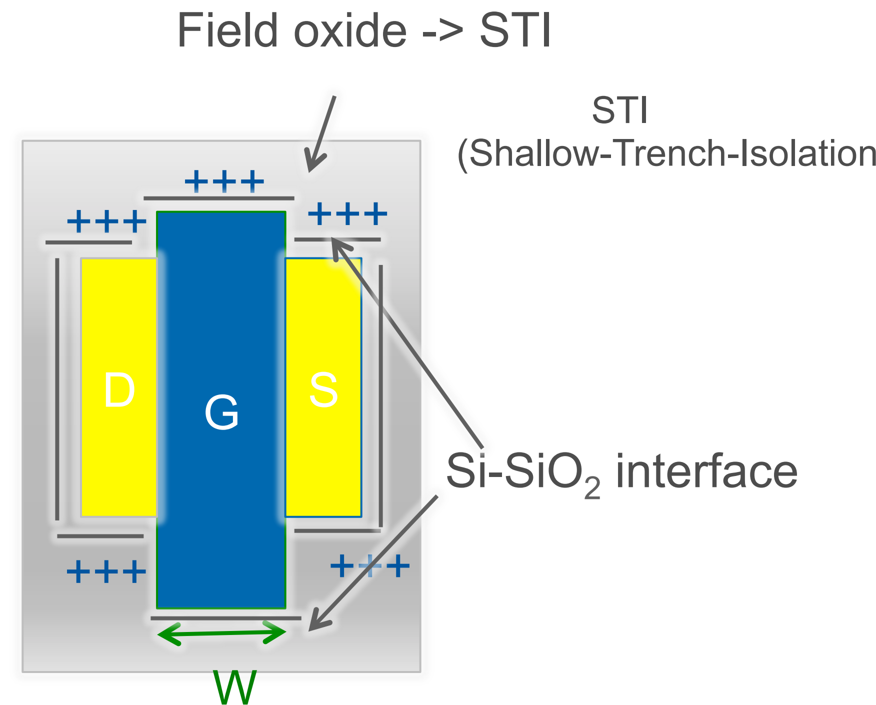




Radiation damage in MOSFET

1. Positive charges trapped in the oxide -> parasitic currents
2. Traps in the Si-SiO_2 interface



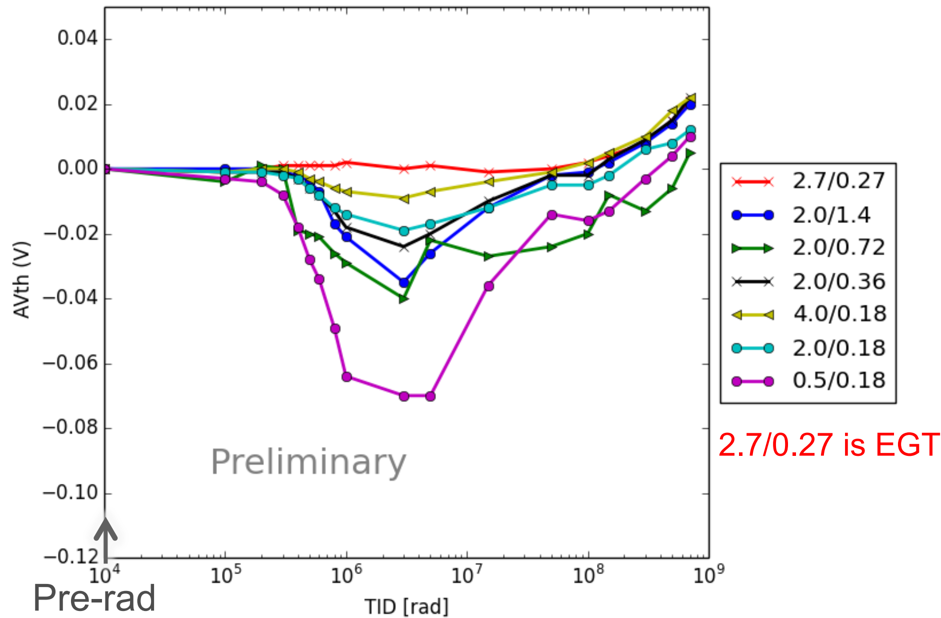


- Bias conditions during irradiation are crucial !!

Threshold voltage shift -NMOS

CHIP #3 – Bias option A

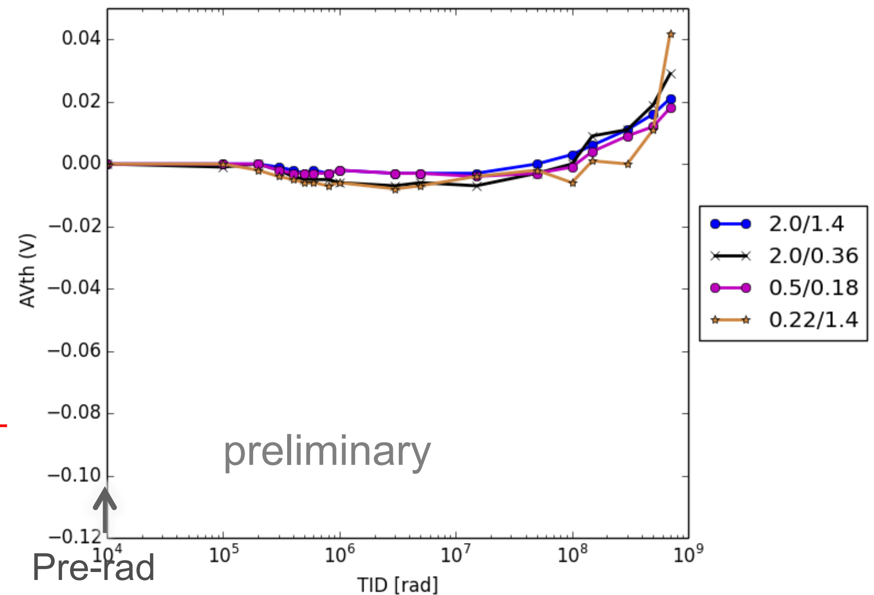
Vg=1.8V ; Vd, Vs =0V (NMOS ON)



- Shift in a rebound way due to: 1)gate/STI oxide 2)gate/STI interface traps
- Enclosed NMOS no shift
- The shift scales with W ->STI dominate
- 0.5/0.18 @700Mrad AVthr=70mV

CHIP #6 – Bias option B

Vg=0V ; Vd, Vs =0V (NMOS OFF)



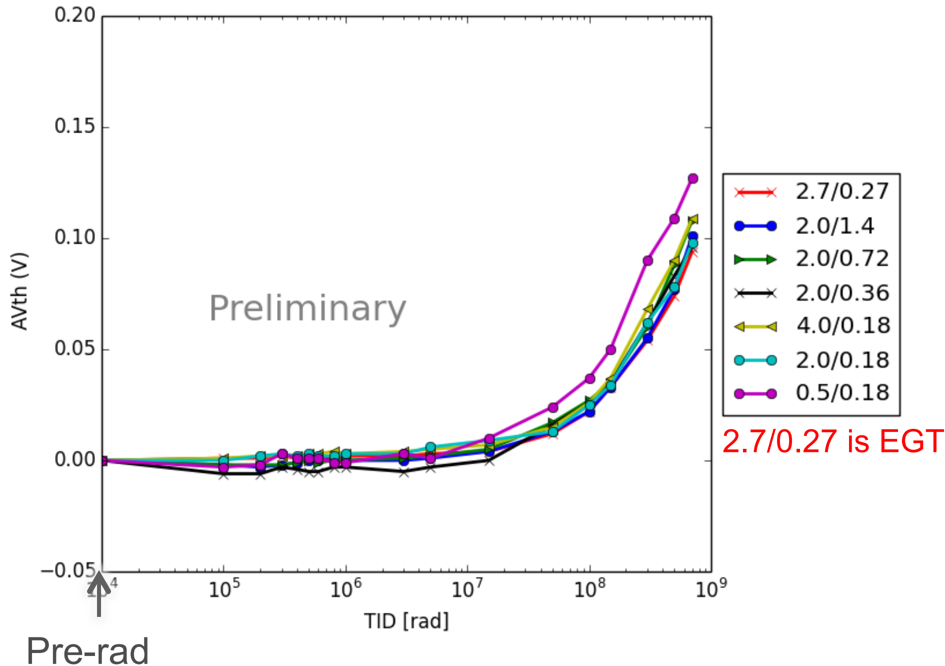
- Almost no gate/STI oxide effect since Vg=0 -> e/h pairs recombine.
- Due to lack of electrical field, interface traps appear at about 500Mrad instead of after 5Mrad
- 0.5/0.18 @700Mrad Avthr=20mV

Threshold voltage shift - PMOS

For PMOS is not clear which bias condition is worse!! -> ISSUE nowadays

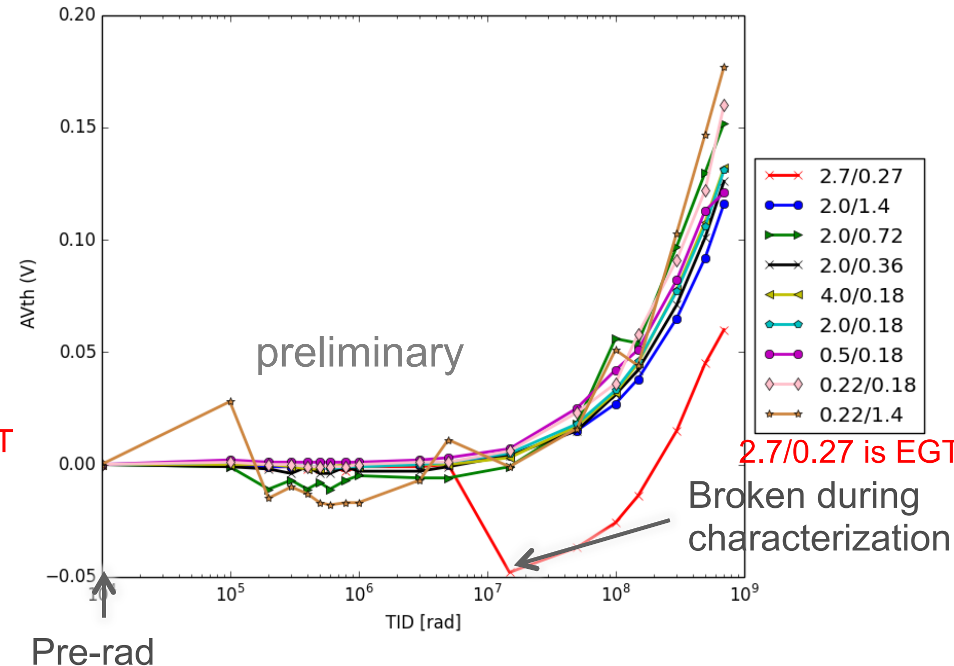
CHIP #3 – Bias option A

Vg=1.8V ; Vd, Vs =1.8V (PMOS OFF)

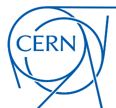


CHIP #6 – Bias option B

Vg=0V ; Vd, Vs =1.8V (PMOS ON)



- As expected, the threshold voltage of PMOS increases for both bias conditions.
- Shift of same order (for 0.5/0.18 -> 120mV).
  - ➔ Not conclusion about worst bias condition

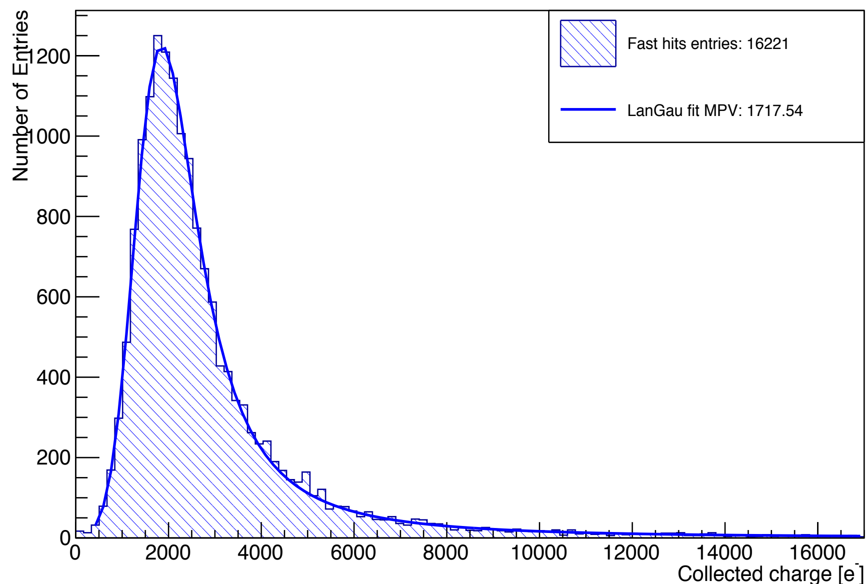


Highlights from Charge Collection Properties

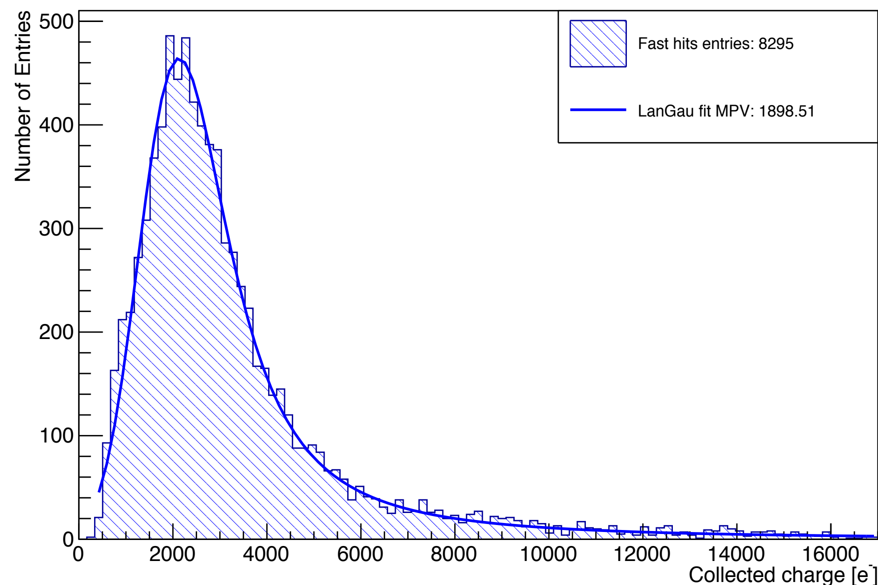
(S. Fernandez-Perez, et al. to be submitted by this month)

^{90}Sr – 50 x 50 μm^2 pixel – 120V at – -30°C

Neutron irradiated
1 x 10^{13} n_{eq} / cm^2



Neutron irradiated
5 x 10^{13} n_{eq} / cm^2



Evolution of N_{eff} with fluence

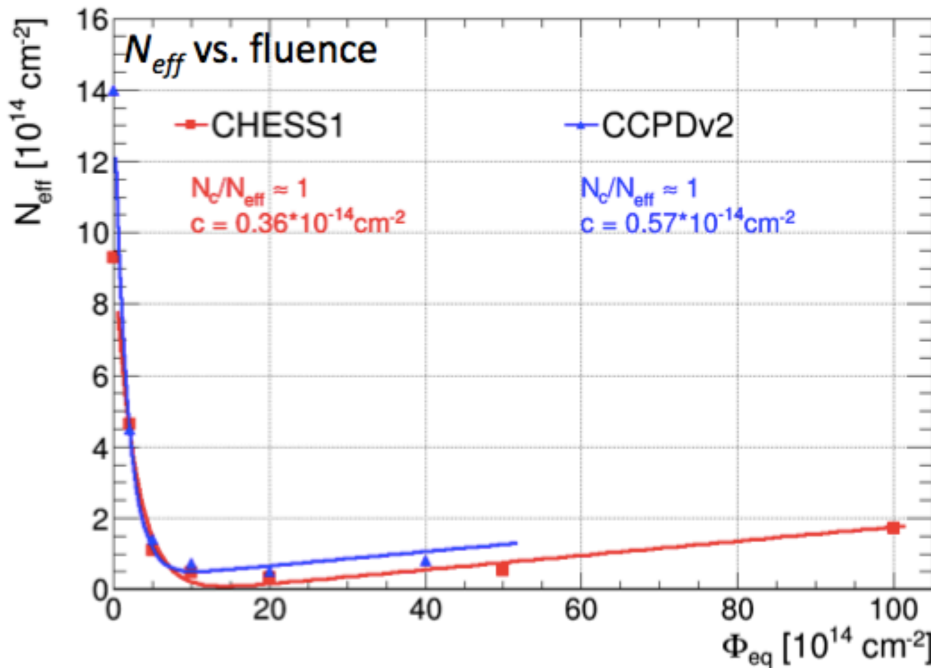
$$N_{eff} = N_{eff\,0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{eq})) + g \cdot \Phi_{eq}$$

$$Width(V_{bias}) = Width(0) + \sqrt{\frac{2\varepsilon\varepsilon_0}{e_0 N_{eff}} V_{bias}}$$

Initial concentration

acceptor removal

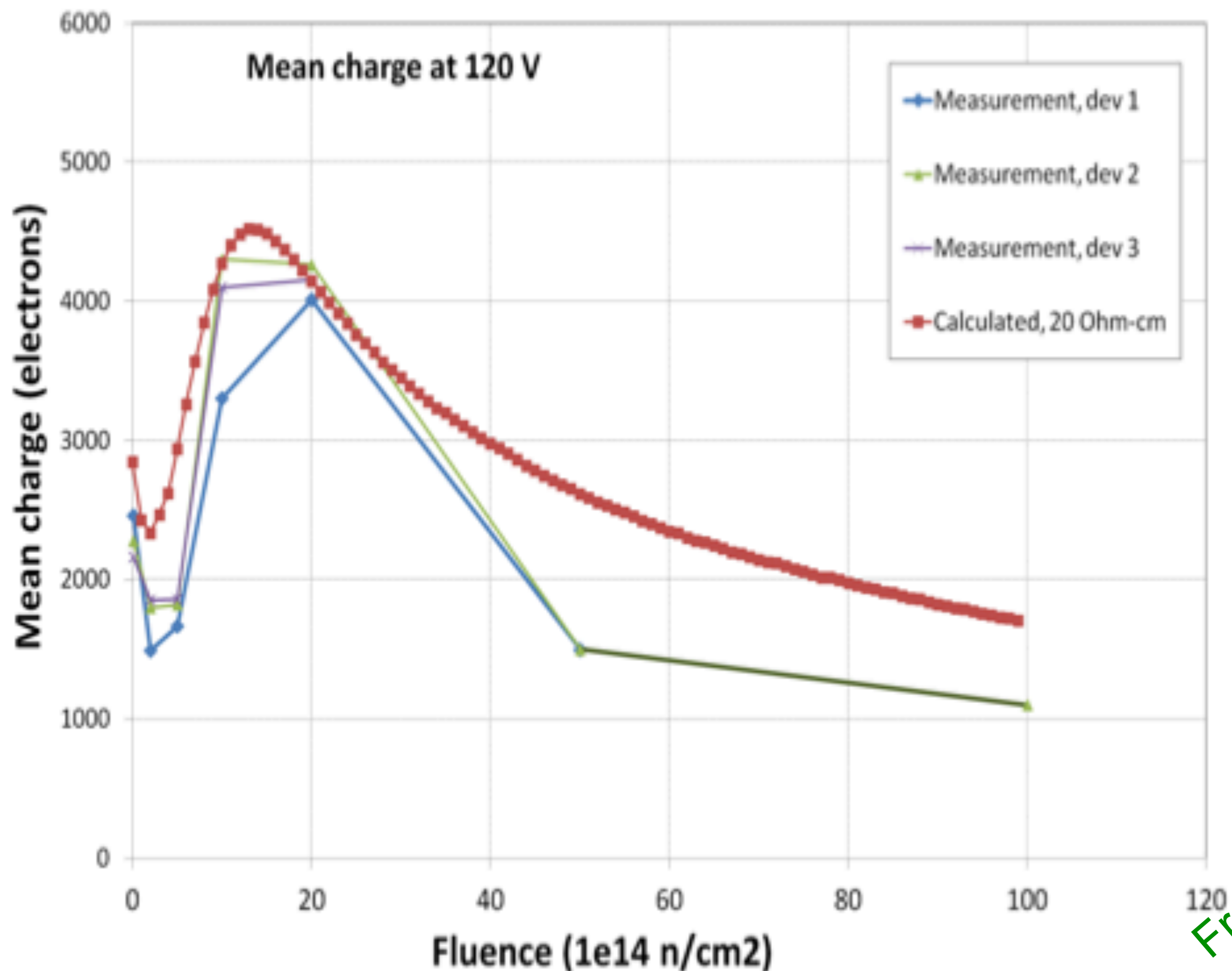
Radiation introduced deep acceptors (stable damage): ***g* = 0.02 cm⁻¹ (fixed)**



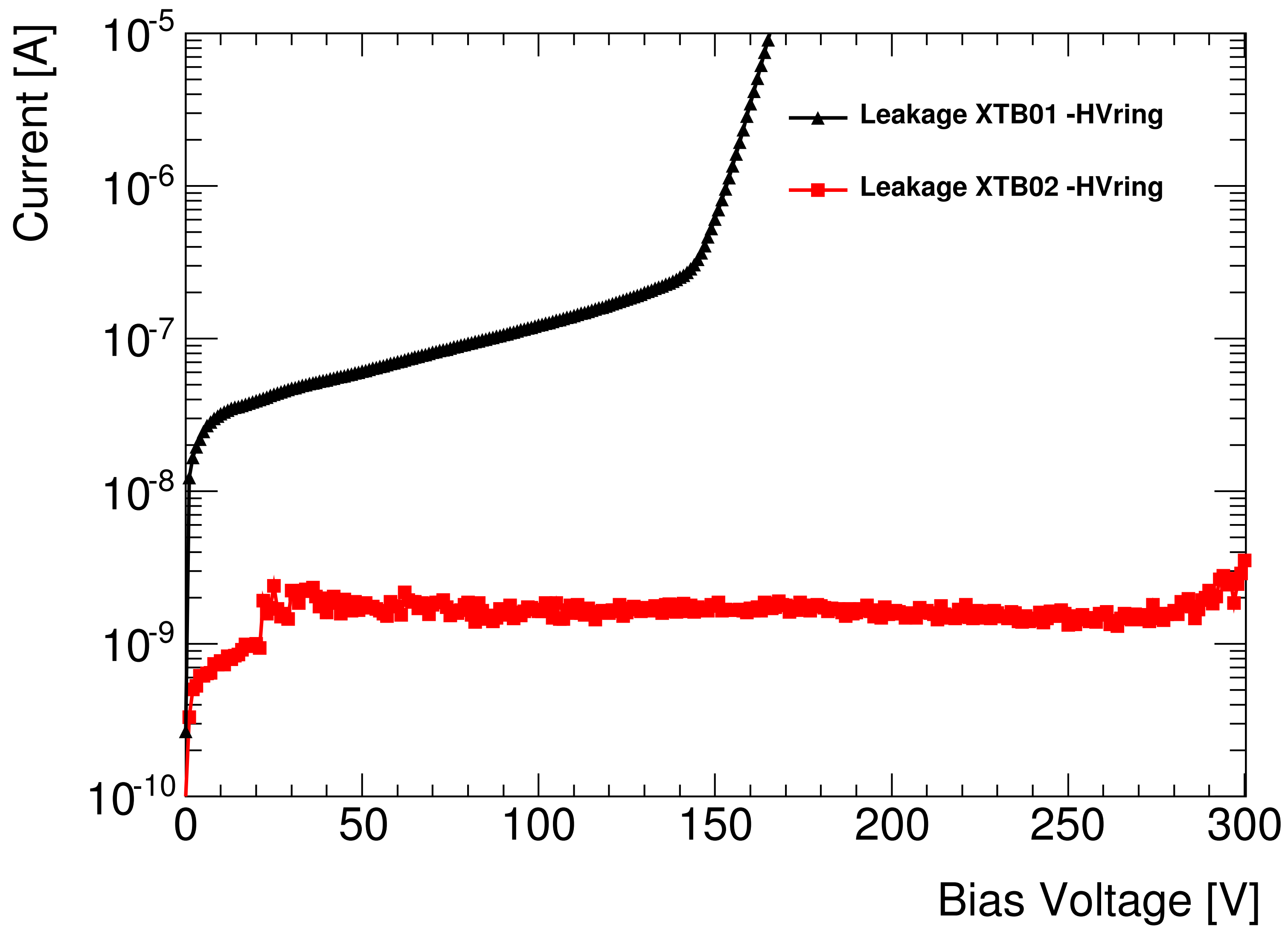
From I. Mandic (ITK week September 2015)

- god fit up to 1e16
- agreement with CCPDv2 (AMS 180 nm, 10 Ohm-cm, measured with active pixels)

Compare measured/calculated

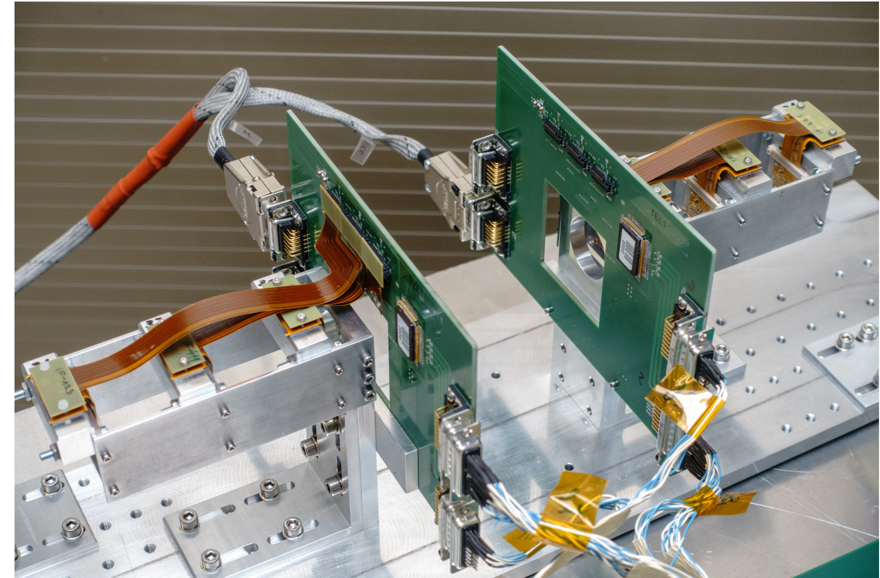


From I. Mandic
(ITK week September 2015)



Current [A]
10-5
10-6
10-7
10-8
10-9
10-10
0
50
100
150
200
250
300
Bias Voltage [V]
Leakage XTB01 -HVring
Leakage XTB02 -HVring

AIDA SBM FE-I4 telescope

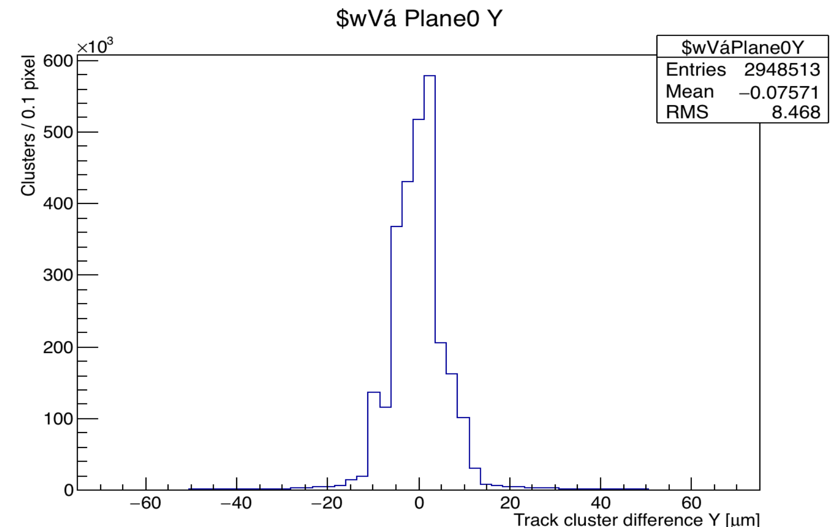


Mechanics

- **Compact** DBM-like mechanics
  - **Size 60x20x20 cm^3**
  - Weight 4 kg
- Two DBM-like telescope arms moveable along Z and Y axis.
- One **rotatable arm**
- Max. **400 mm spacing** between the arms
- 6 single-chip **FE-I4B** Silicon planar sensors (**250x50 um^2 pitch, ~2x2 cm^2 active area**)

Triggering

- External – PMTs
- Internal – HitOR functionality in FE-I4s. Hitbus chip for HitOR trigger handling (e.g. trigger issued when a hit is recorded in all planes)
- Triggering on a region of interest in FE-I4



1) The outer pixel efficiency size grows

	60-V	90-V	120-V
Entries	1006680	1012050	1015555
Mean x	−0.495	−0.493	−0.493
Mean y	11.345	6.406	−0.493
RMS x	18.002	19.984	20.569
RMS y	17.945	19.973	20.569

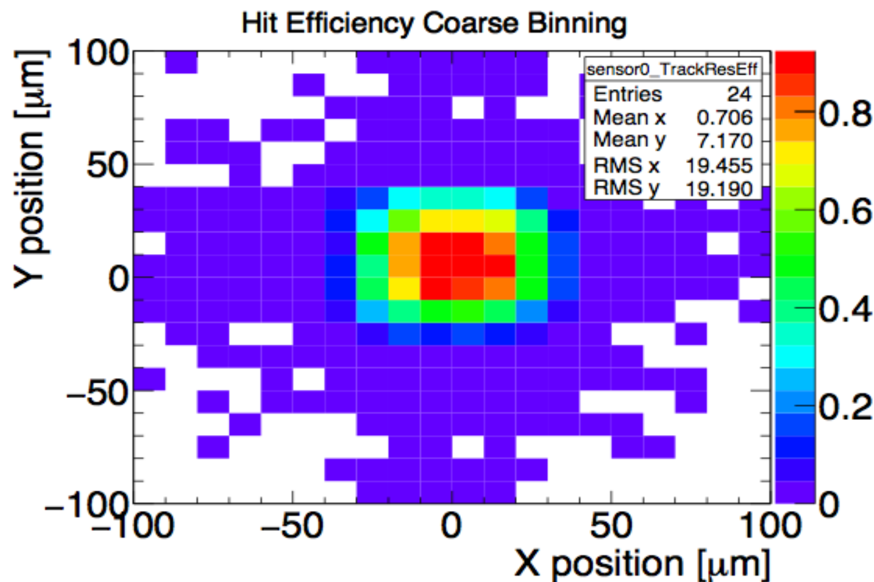
2) The inner pixel efficiency increases

	60-V	90-V	120-V
Entries	1006680	1012050	1015555
Mean x	−0.495	−0.493	−0.493
Mean y	11.345	6.406	−0.493
RMS x	18.002	19.984	20.569
RMS y	17.945	19.973	20.569

DUT Efficiency at 90-V

- Comparison with and without T_0 cuts on the clusters for the 90-V bias
- Reduction in hits far from the chip center

No cut on the clusters



Cut on T_0