TID effects in 65nm transistors: summary of a long irradiation study at the CERN X-rays facility

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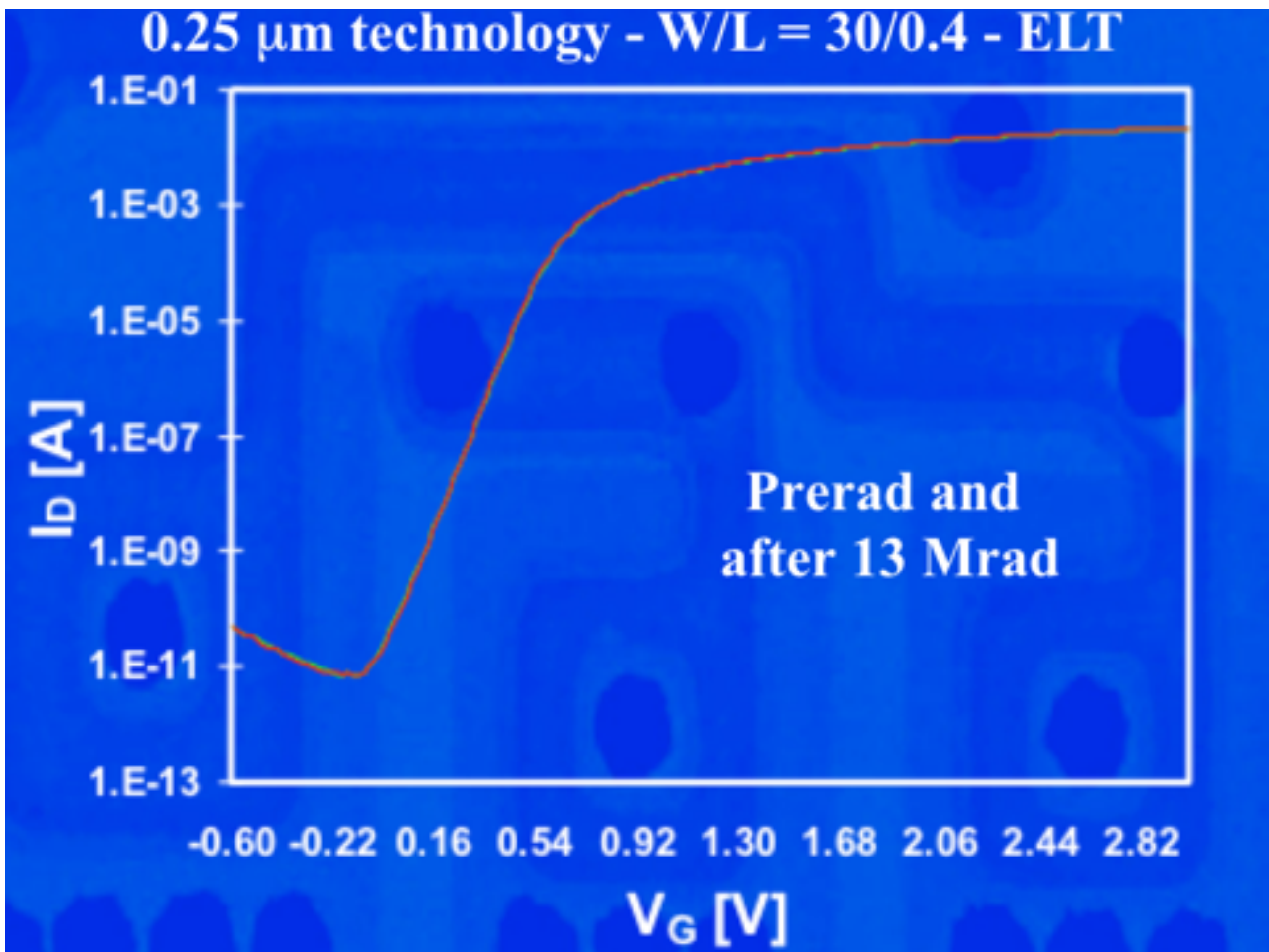
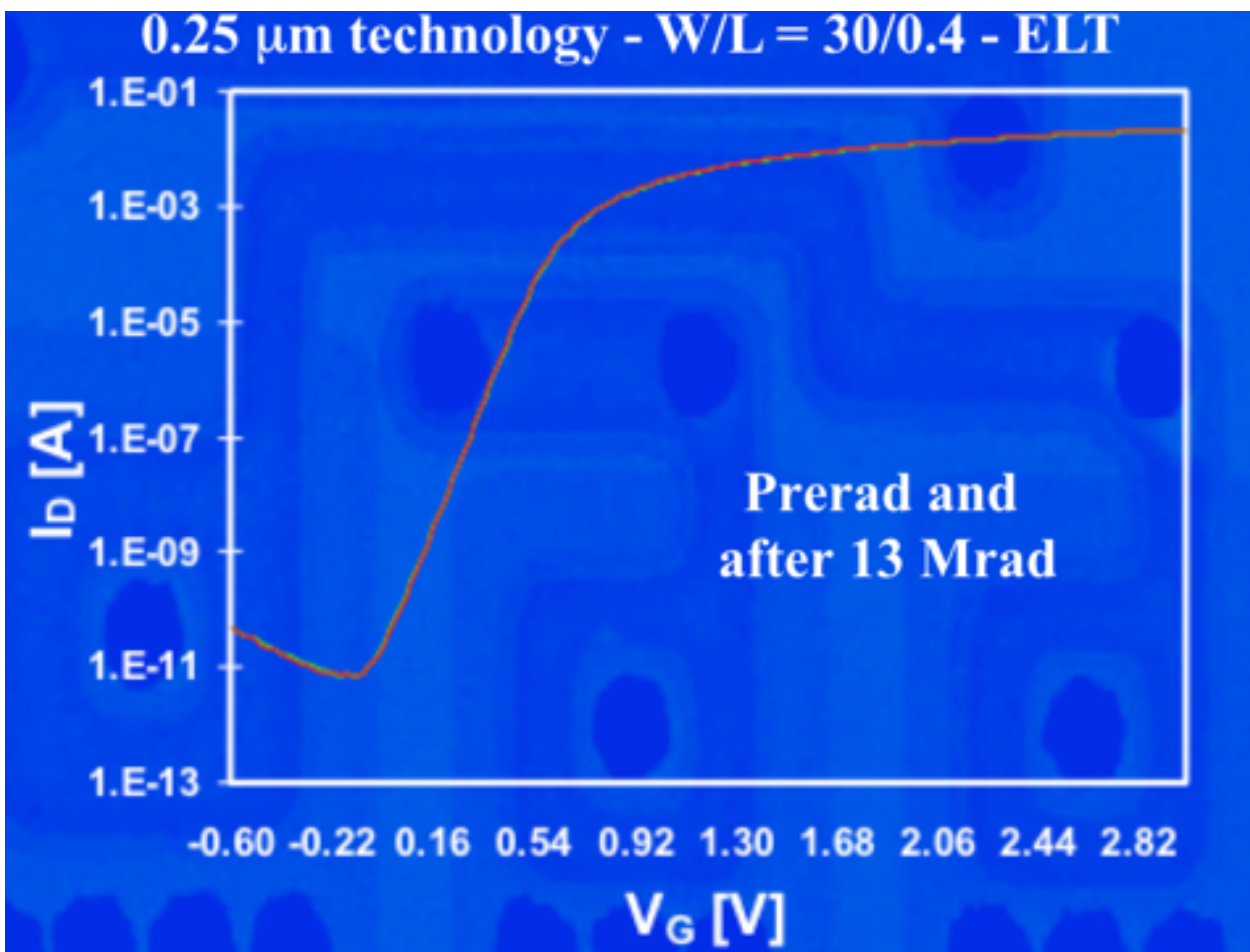
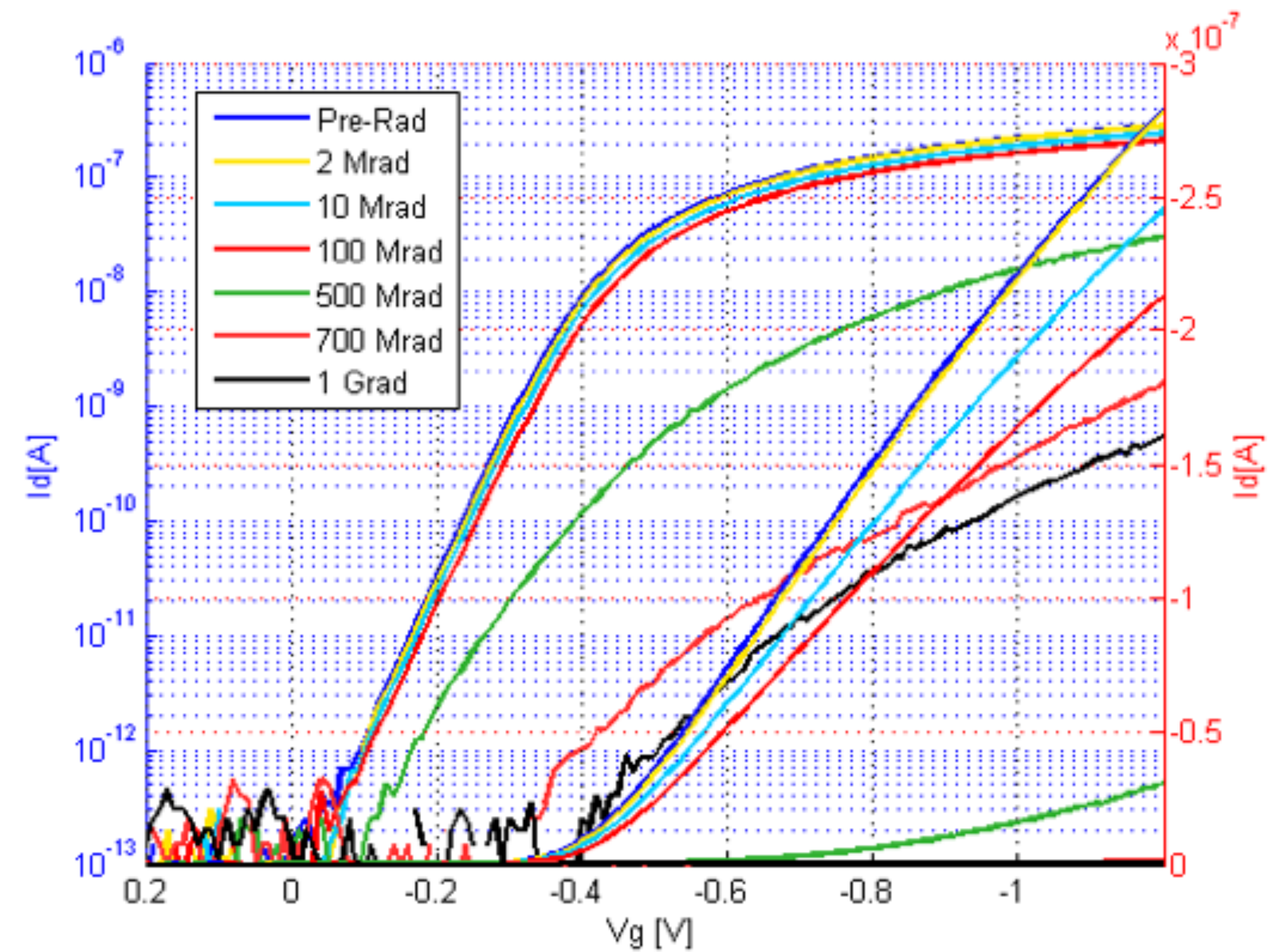
LEB Workshop 1998



LEB Workshop 1998

TWEPP Workshop 2014-15





Very complex phenomenology
Long time to run each experiment
Non-ideal test structures
Need to make a synthesis

Approximate
Incomplete
Hopefully correct

This is a summary of the results in graphical form (qualitative)

Size

L	60nm	500nm	1um	10um
W	120nm	500nm	1um	10um

Bias

Vgs	1.2V	0.6V	0V
Vds	1.2V	0.6V	0V

T

100C	60C	25C	-30C

Transistor size matters!!!

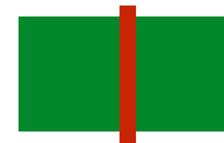
Bias and Temperature strongly influence the results, in a way that is difficult to explain on the basis of our previous experience

What was measured?

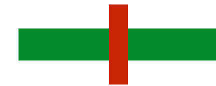
TID-induced degradation of the electrical performance (I_{on})

Narrow channel transistors

Short channel transistors



Short and Narrow channel transistors



Results from Negative Bias Thermal Instability stresses (combined with TID)

Results from Hot Carrier Injection stresses (combined with TID)

Variability of the TID-induced degradation

WHAT

Transistors - Only CORE (no I/O)

HOW

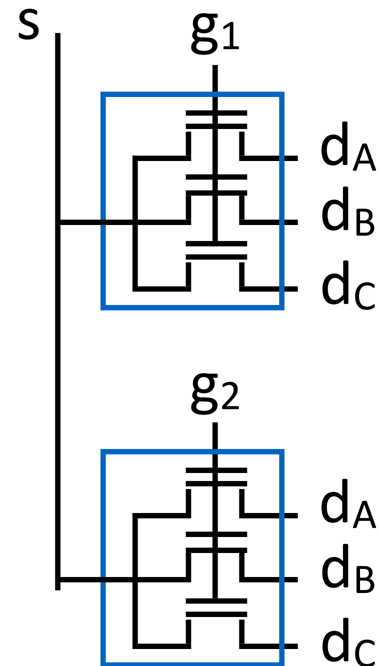
DC bias during irradiation and annealing
Regulated T during irradiation and annealing

We learnt that the test structures, even with those most recently added, are not sufficient for our purposes

Standard

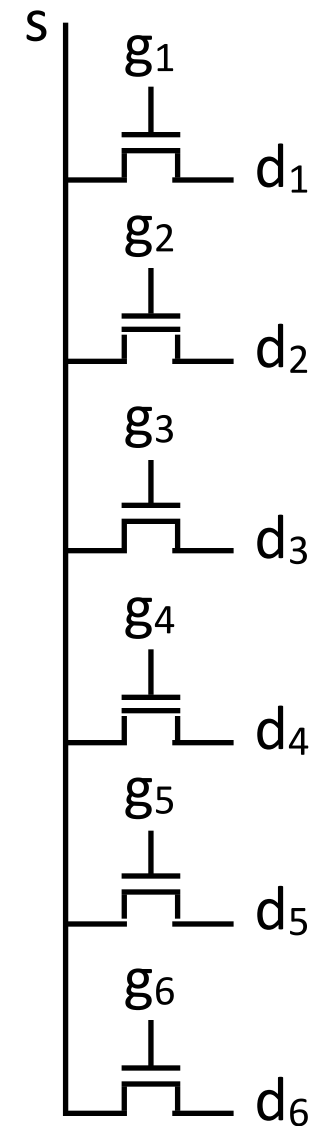
Array of W (L=60nm)
Array of L (W=1um)

Different bias



A = 600/60nm
B= 0.12/1um
C= 0.6/1um

Variability



all = 160/60nm

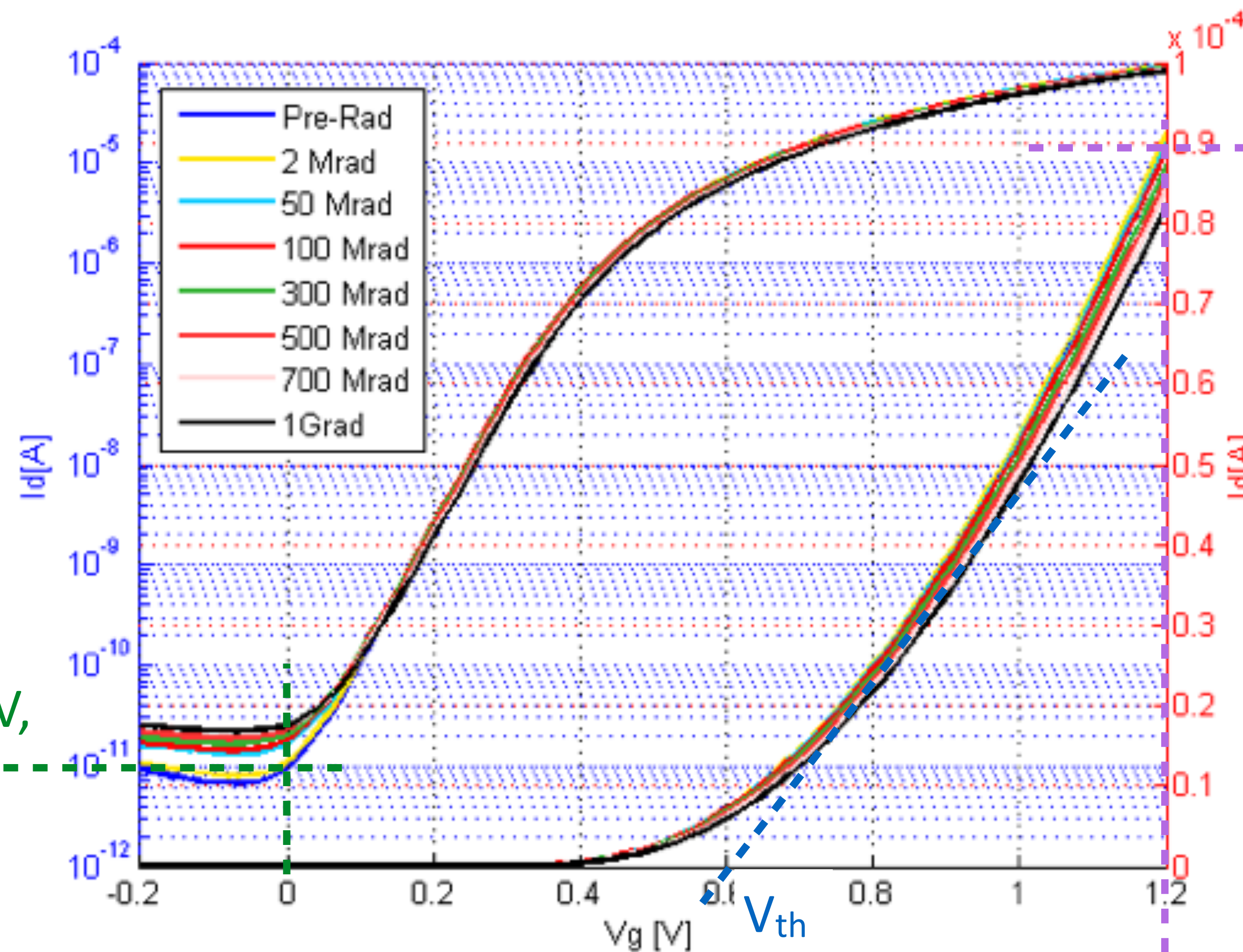
Missing

Array of W (L=10um)
Array of L (Enclosed transistors, ELT)
'Different bias' structures with longer and larger sizes, and ELTs
'Variability' structures with longer and larger sizes

The main parameters extracted from the measurements are:

- **Drive current (I_{on})**
- **Threshold voltage (V_{th})**
- **Transconductance (G_m)**
- **Subthreshold swing (SubS)**
- **Leakage current**

Leakage at |Vgs|= 0V, |Vds|=1.2V



I_{on} at |Vgs|=|Vds|=1.2V

What was measured?

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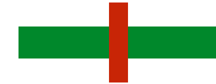
Short channel transistors

Short and Narrow channel transistors



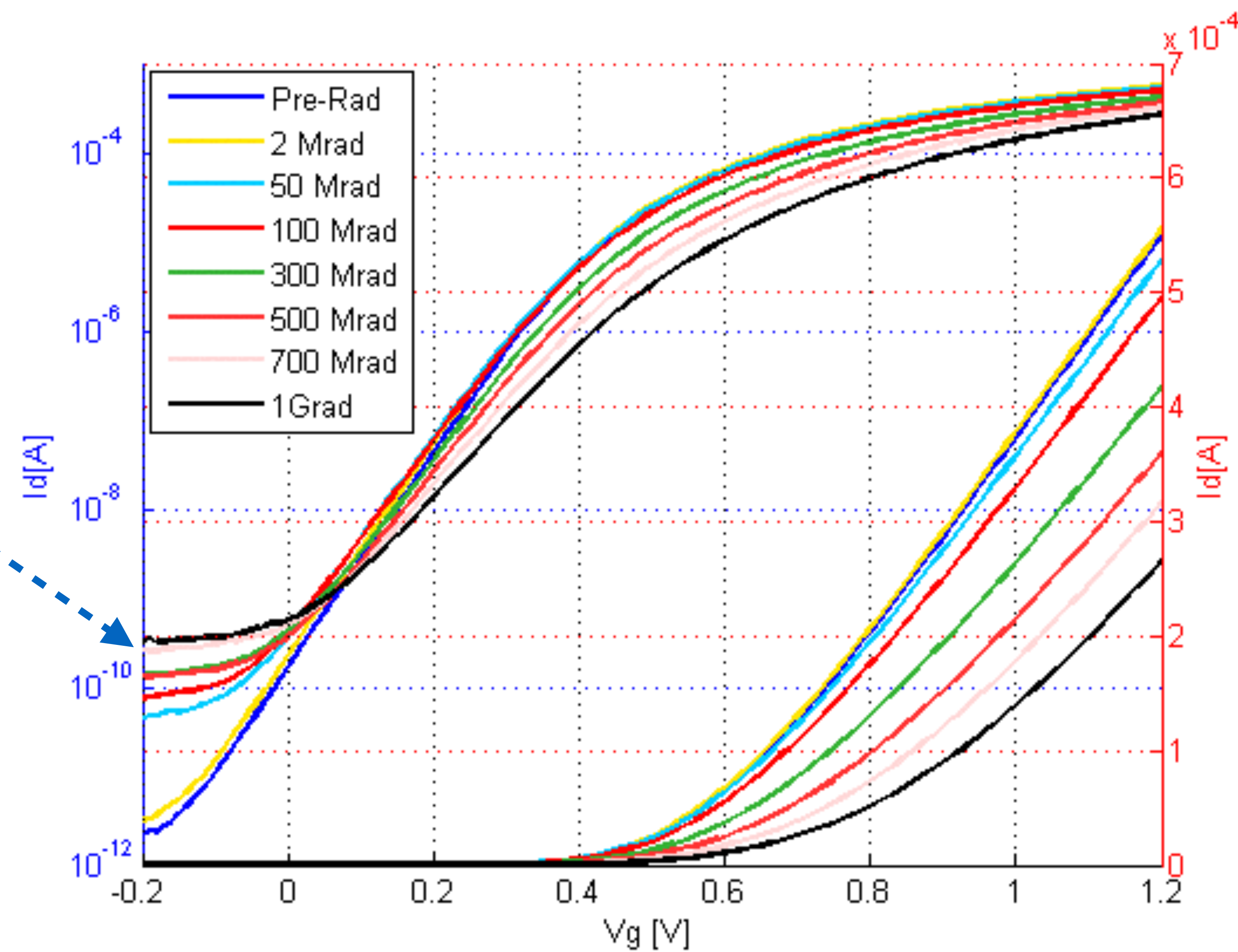
Results from Negative Bias Thermal Instability stresses (combined with TID)

Results from Hot Carrier Injection stresses (combined with TID)

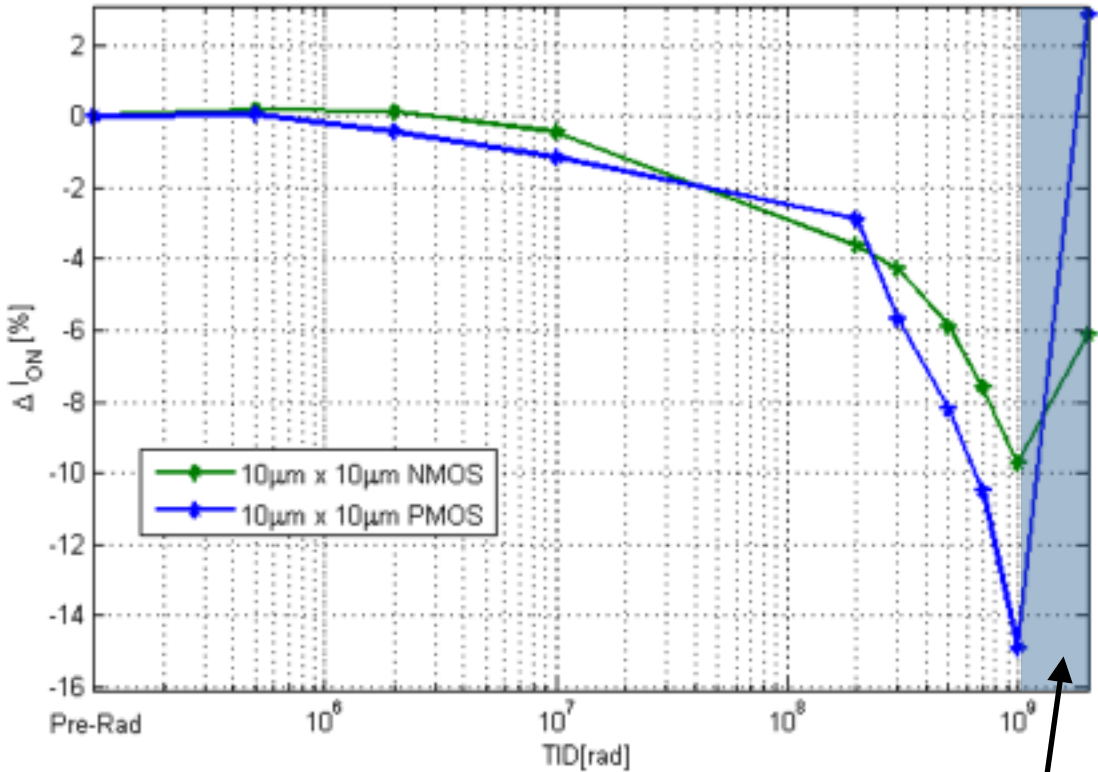
Variability of the TID-induced degradation

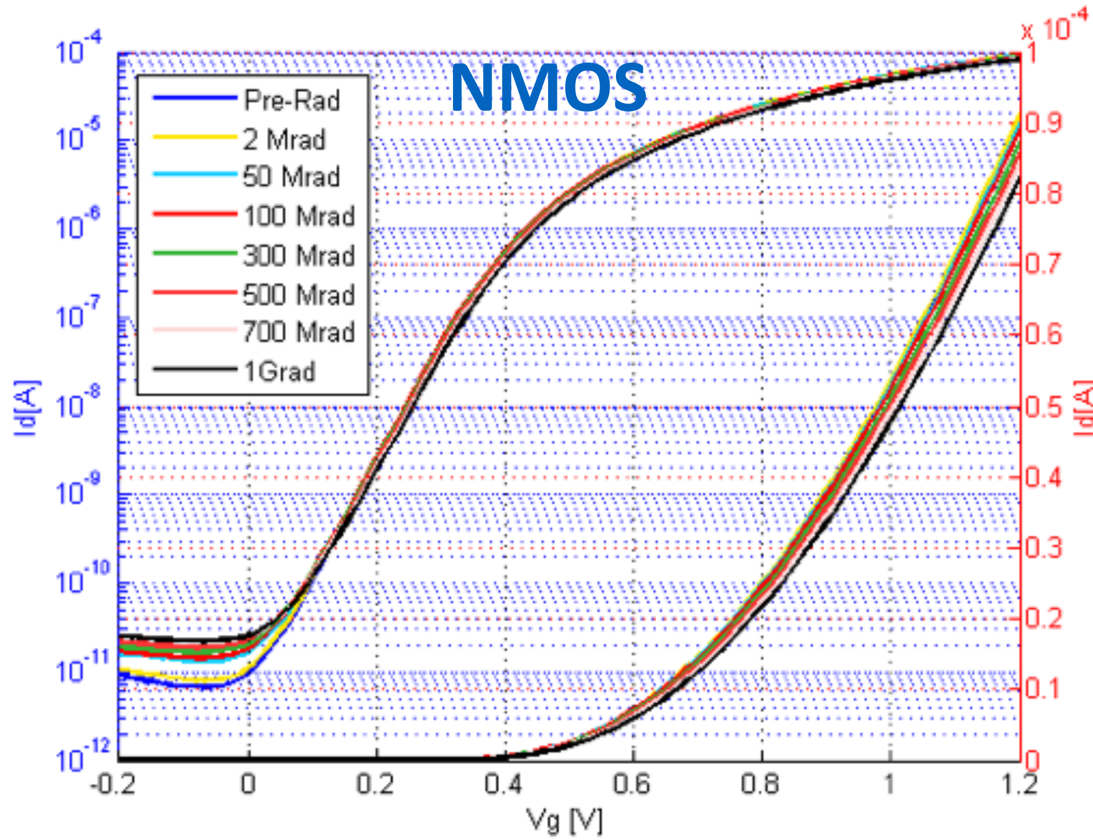
There will be no further comment about leakage currents, because we did not measure significant currents (for typical applications) in either NMOS transistors or FOXFETs

Leakage below 40nA·nm (normalised to L)

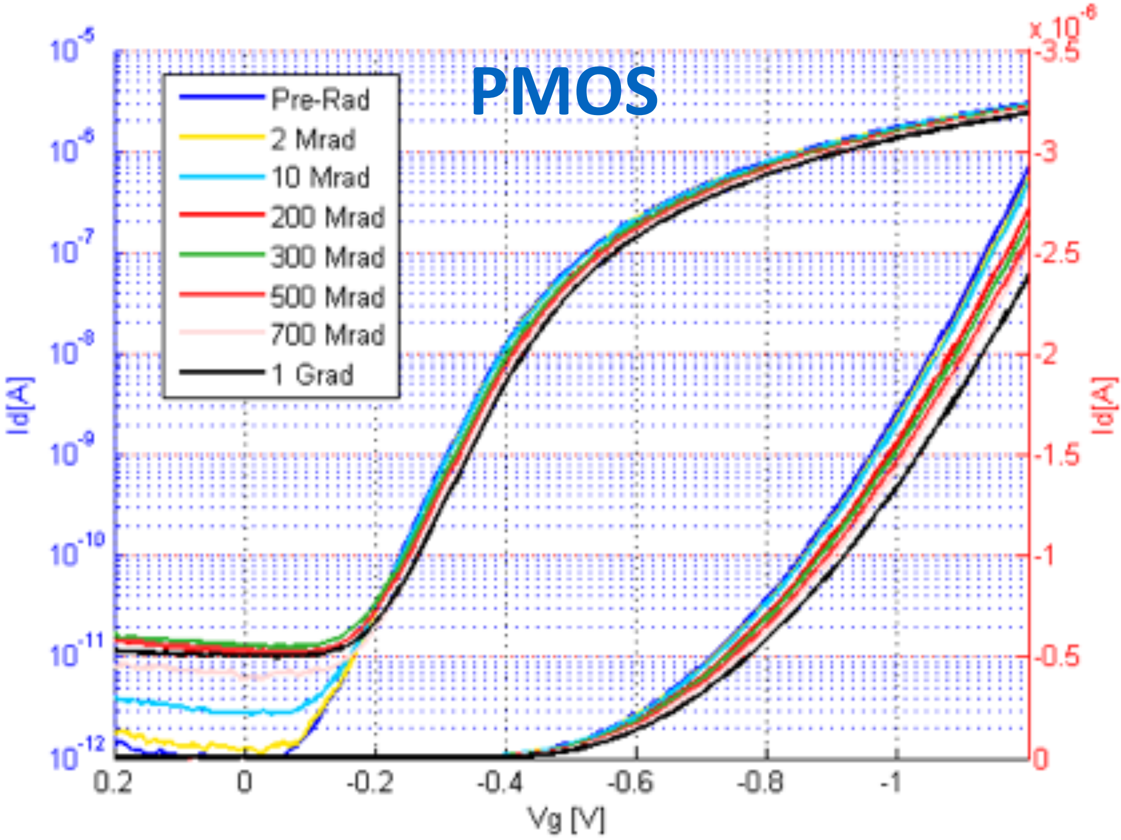


The degradation of long and large transistors is limited: the thin gate oxide is radiation hard!





Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V
Curves Id-Vg in saturation

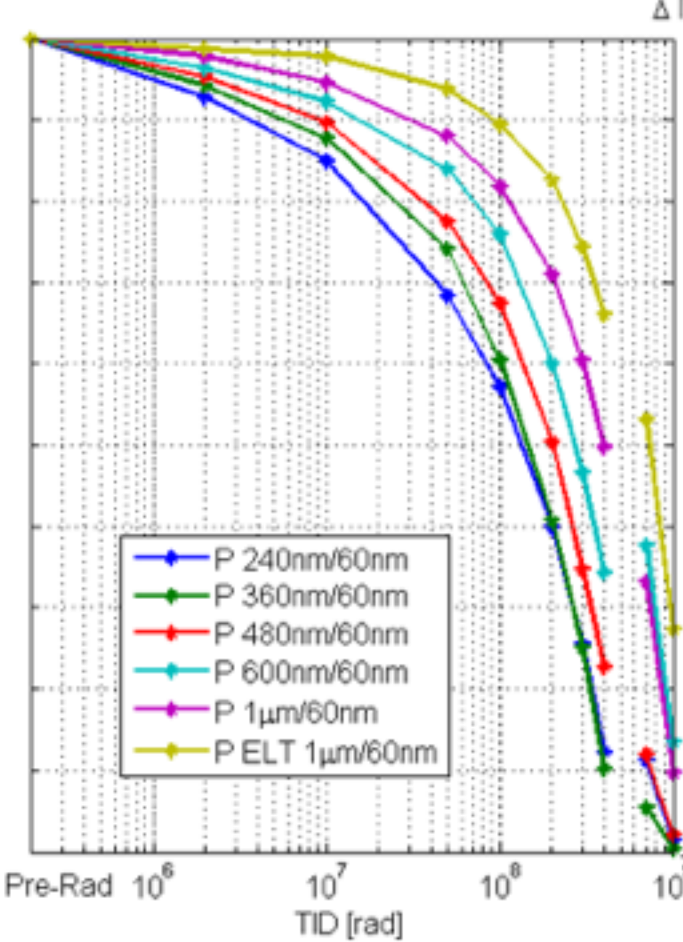


Annealing several days @ 25C, no bias
Very little evolution after that, even with T and bias

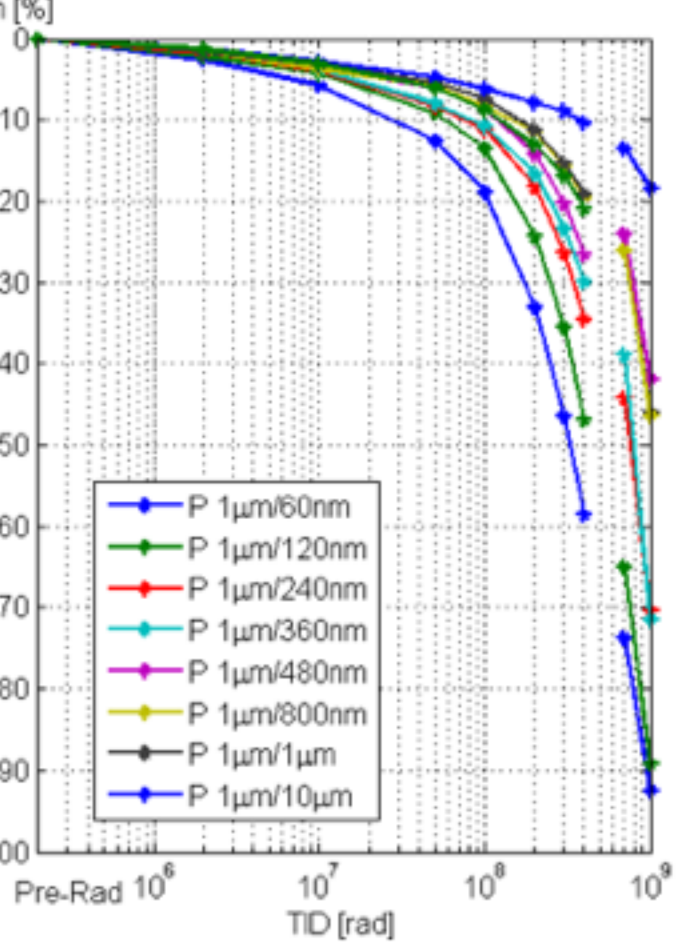
Radiation damage is severe in short and narrow channel transistors, where it depends on the <u>bias</u> and <u>temperature</u> applied both during and after irradiation

Radiation-Induced Narrow Channel Effect (RINCE)
Radiation-Induced Short Channel Effect (RISCE)

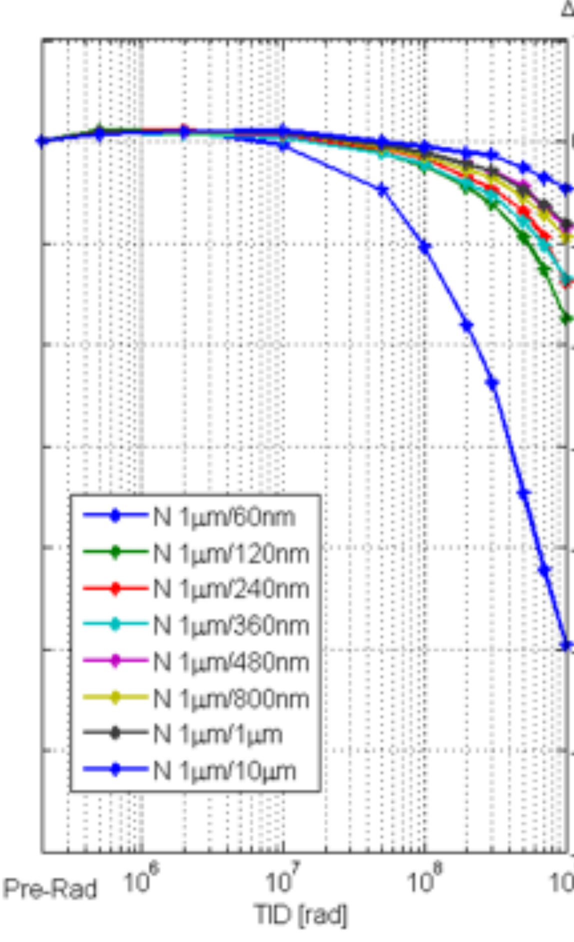
PMOS W array



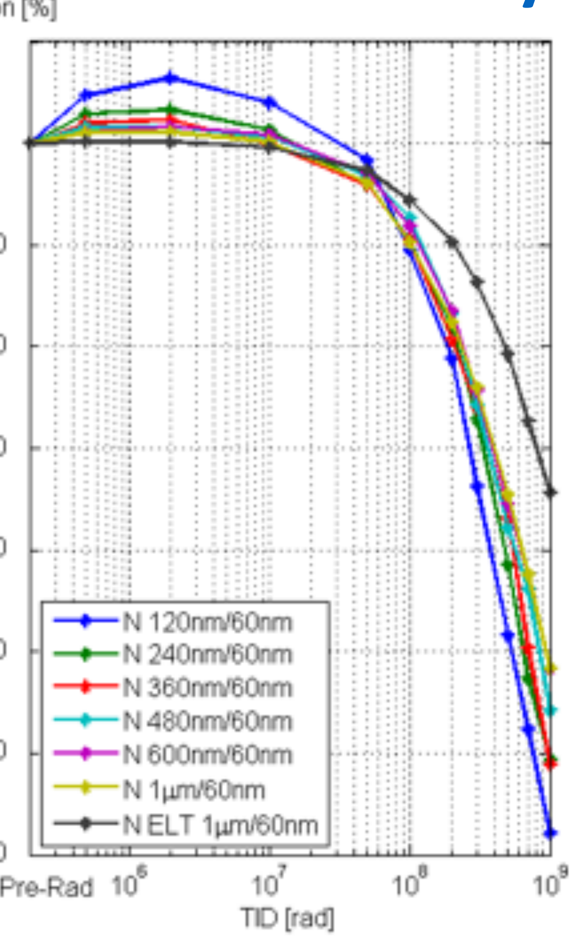
PMOS L array



NMOS L array



NMOS W array

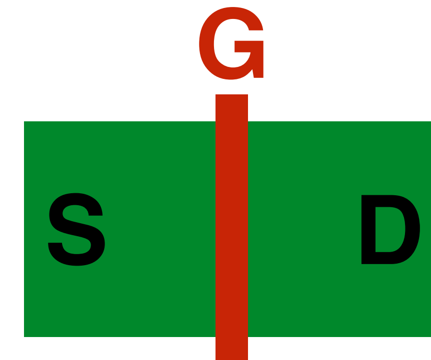


T = 25C
Bias: |Vgs|=|Vds|=1.2V

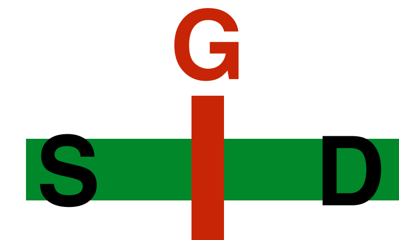
Let's try to tidy up a little……

Narrow channel transistors

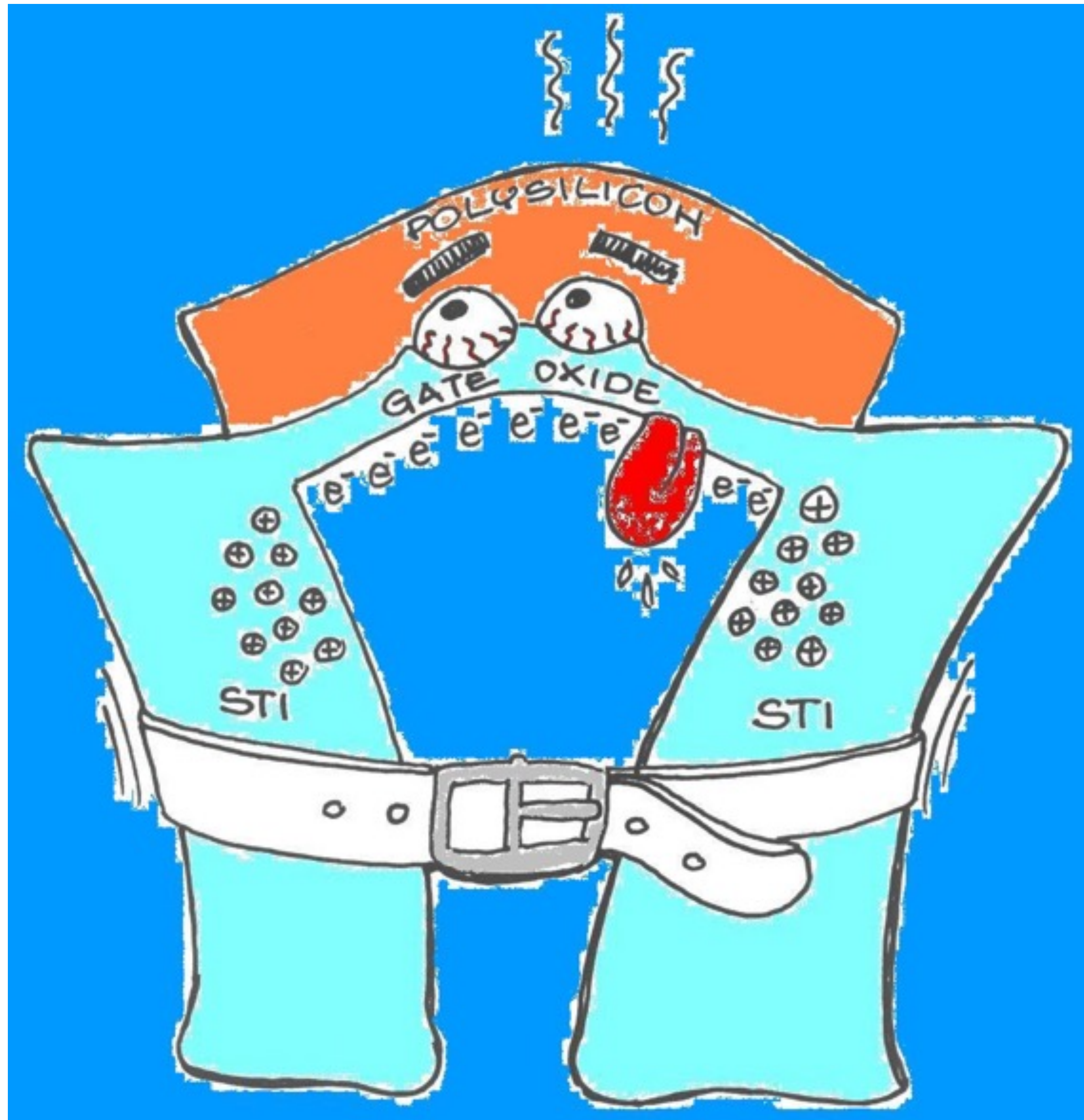
Short channel transistors



Short and Narrow channel transistors



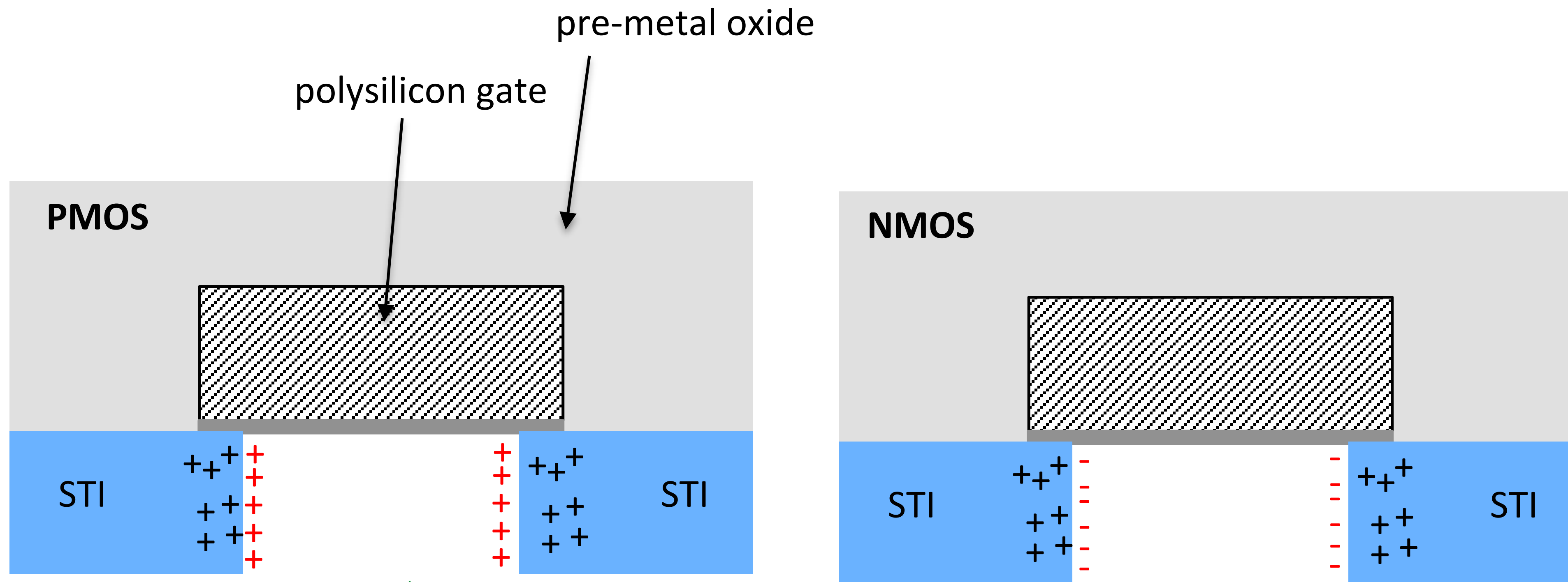
Radiation Induced Narrow Channel Effect (RINCE)

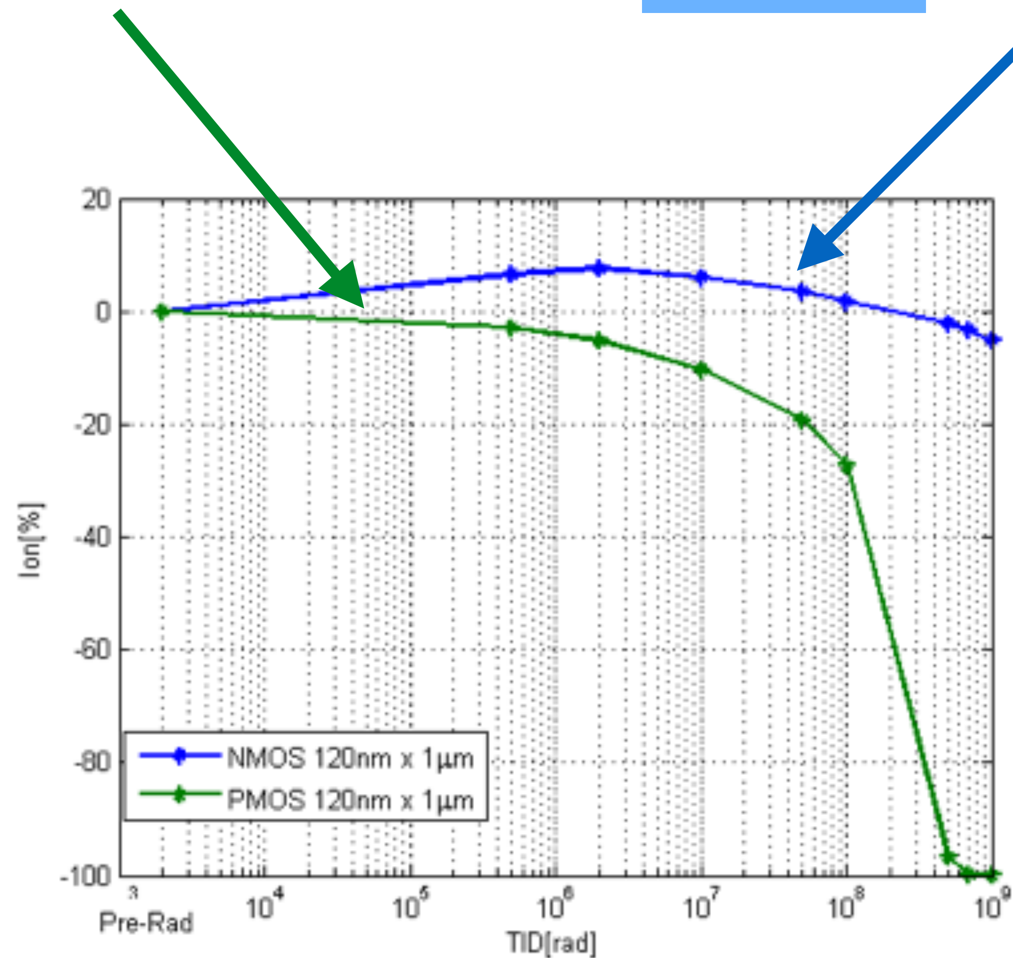


From poster presented at 2005 NSREC, Seattle

RINCE is traceable to radiation effects in the STI oxide

The dynamics of the trapping of charges in the oxide or in interface traps determines the response of NMOS and PMOS - these are mechanisms that are relatively well known

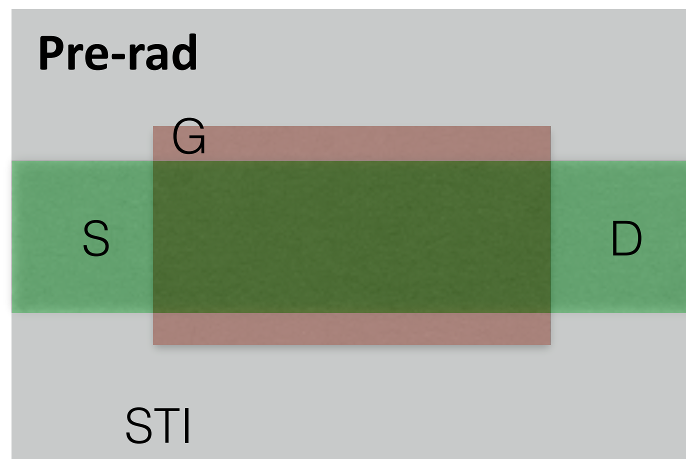


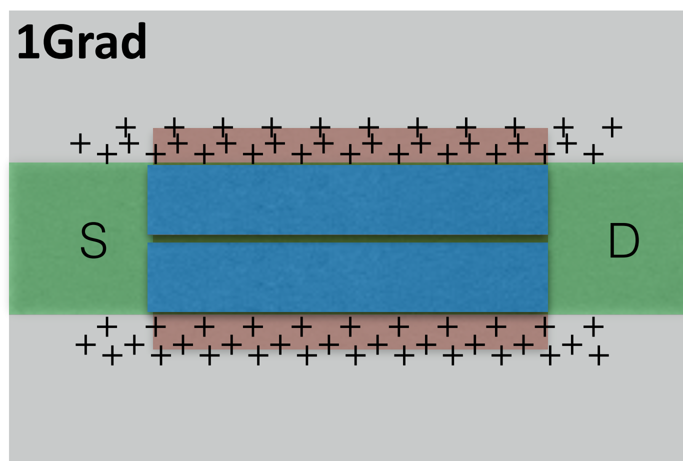


Transistors' size: W=120nm, L=1um
Irradiation conditions:
T=25C
Bias: |Vgs|=|Vds|=1.2V

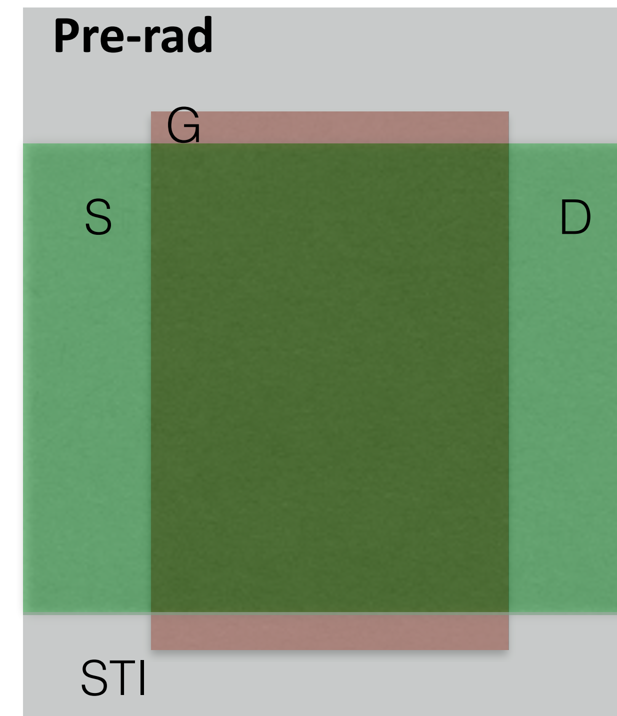
RINCE can be conceptually represented by this cartoon

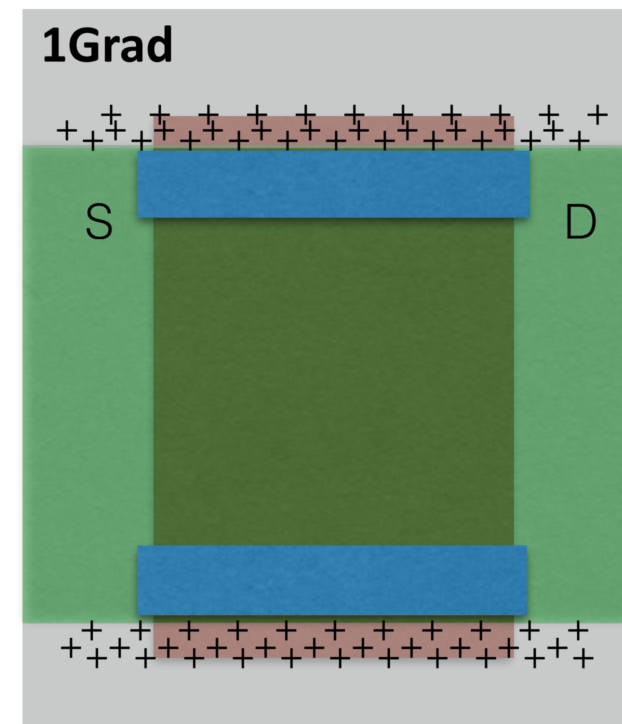
W=min size





W=moderate size



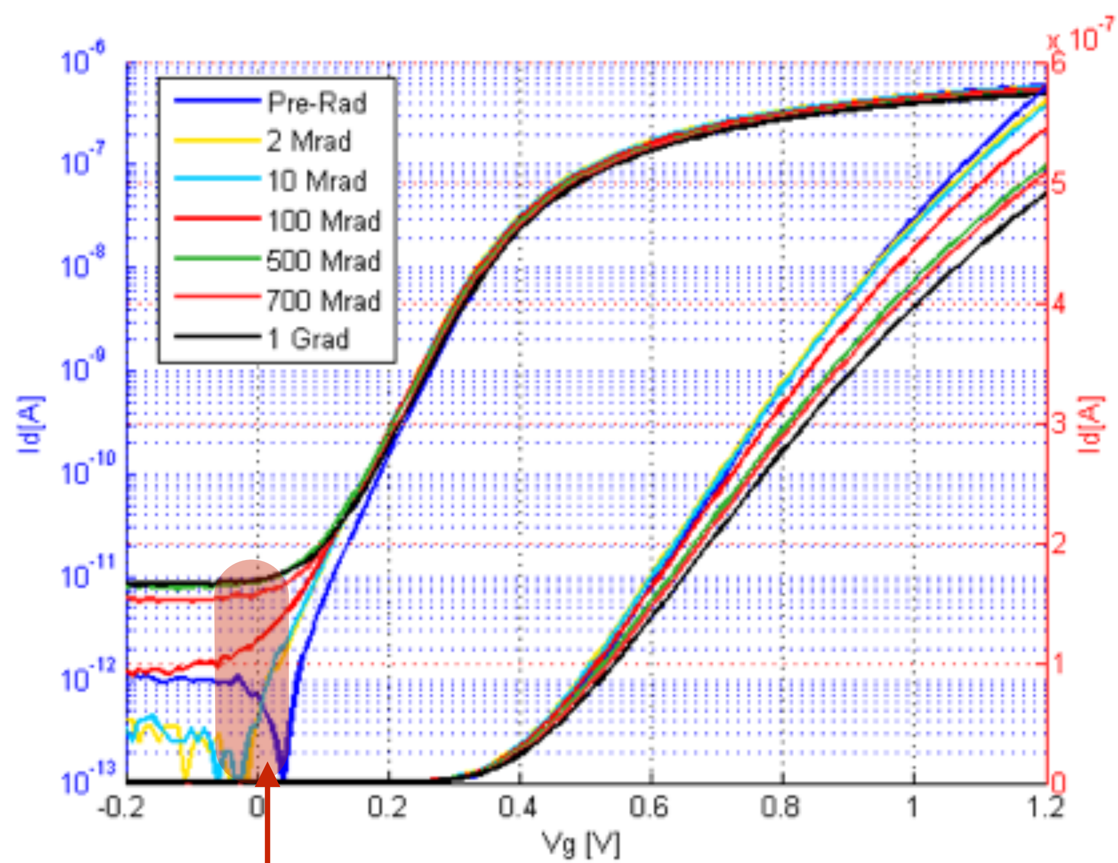


NOTE: In this cartoon, there is no distinction between the positive charge trapped in the oxide or in interface traps

Narrow channel PMOS transistors do not work above 500Mrad, while NMOS are working without large damage up to 1Grad

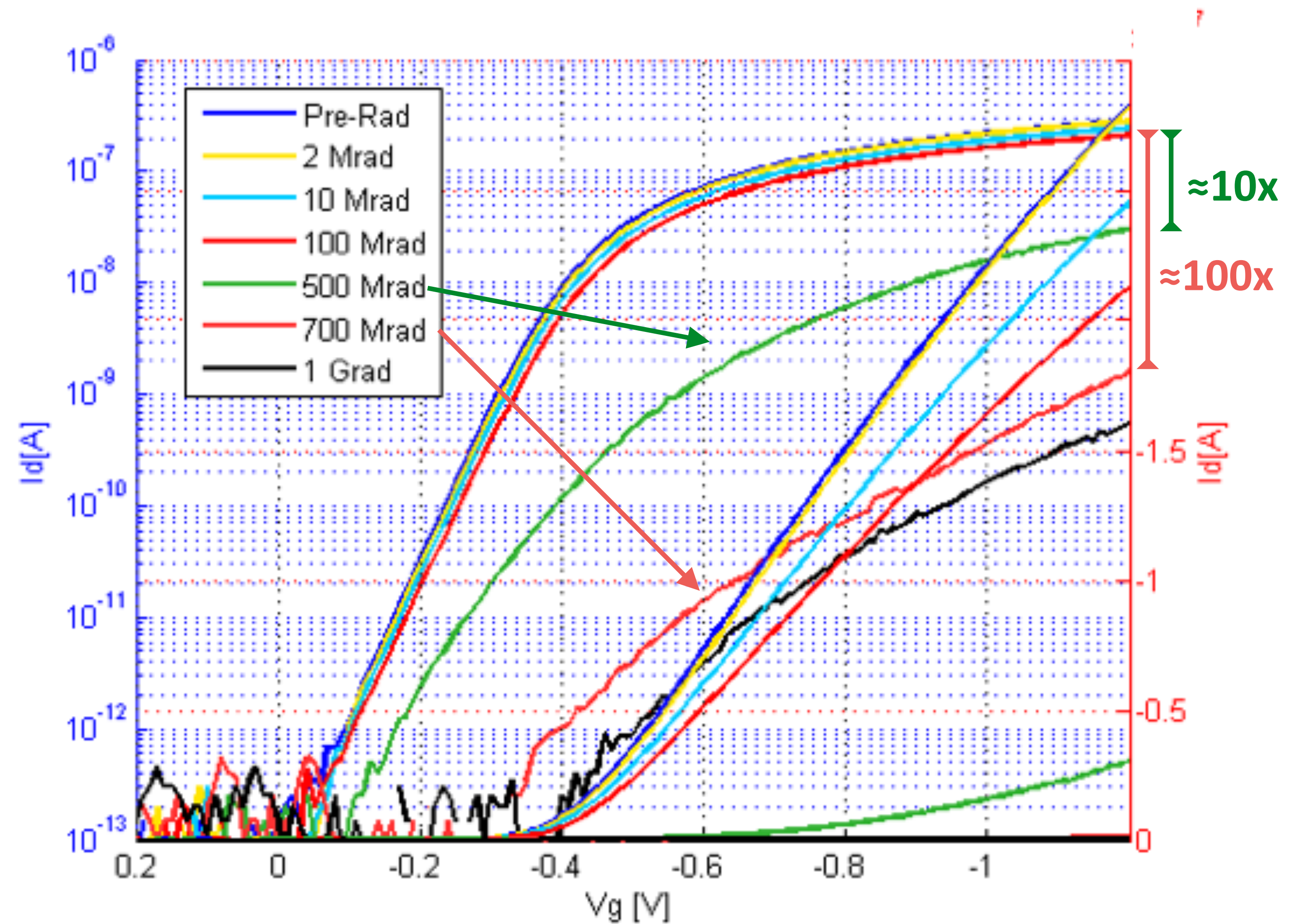
Since NMOS damage is always below 20%, it is not discussed in detail - only PMOS are discussed

NMOS



Very small leakage!

PMOS

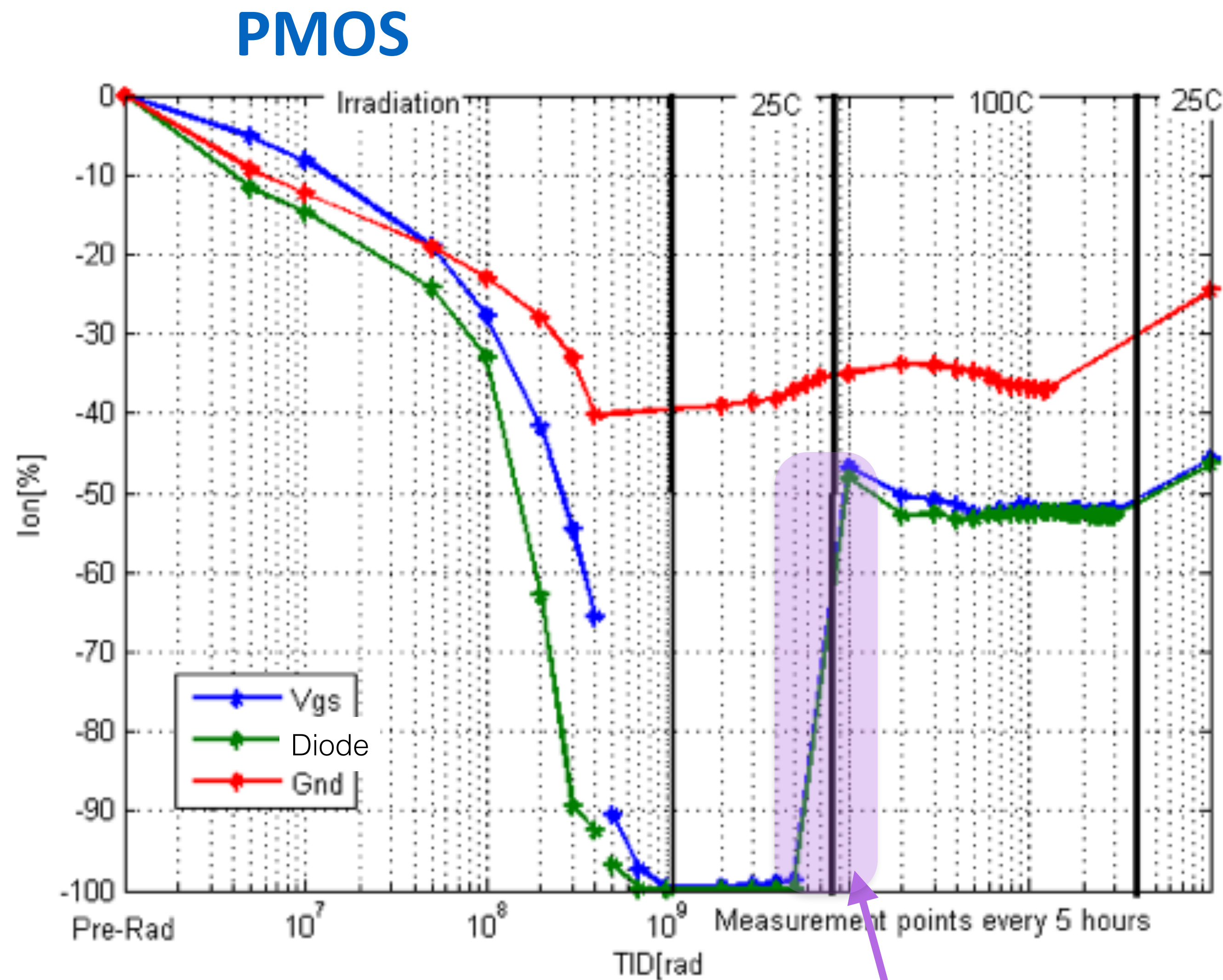


Transistors' size: W=120nm, L=1um
Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V

Influence of BIAS

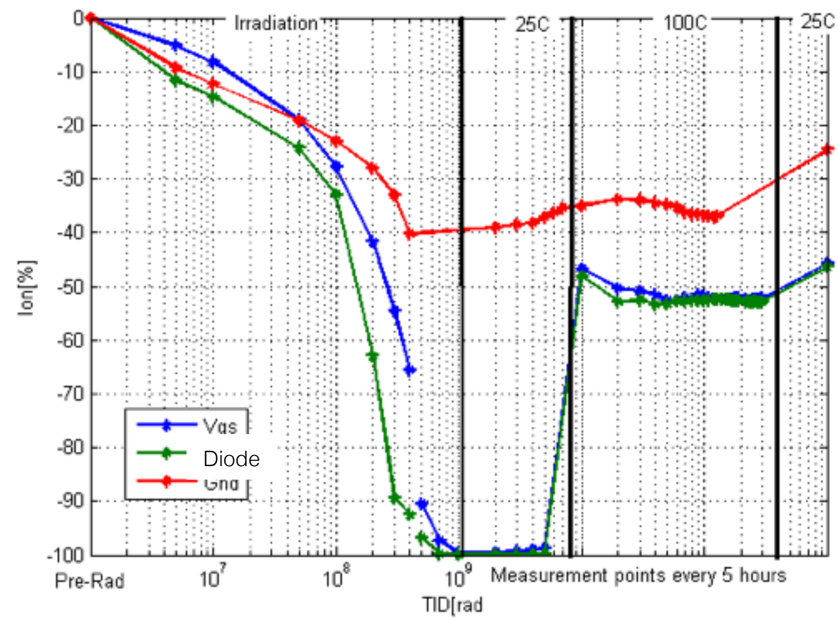
For PMOS, there is a strong bias dependence

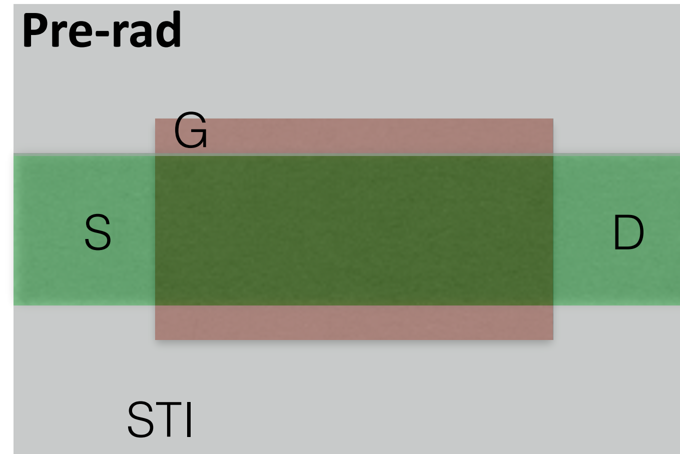
The damage is larger when a V_{gs} is applied, in agreement with common sense.
However, it is more difficult to explain why the application of a large $_{Vds}$ enhances the damage.

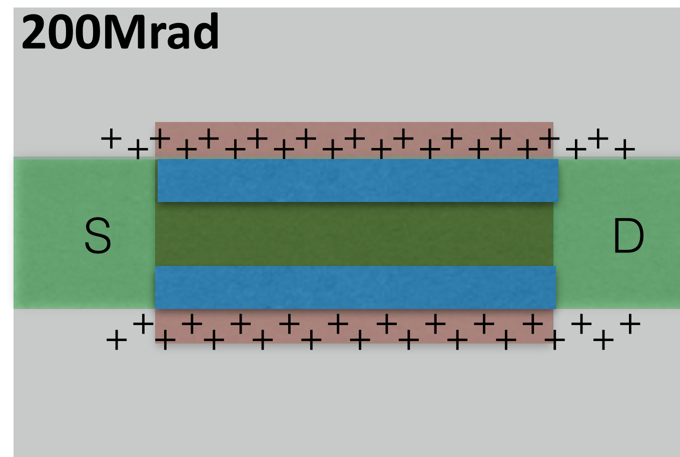


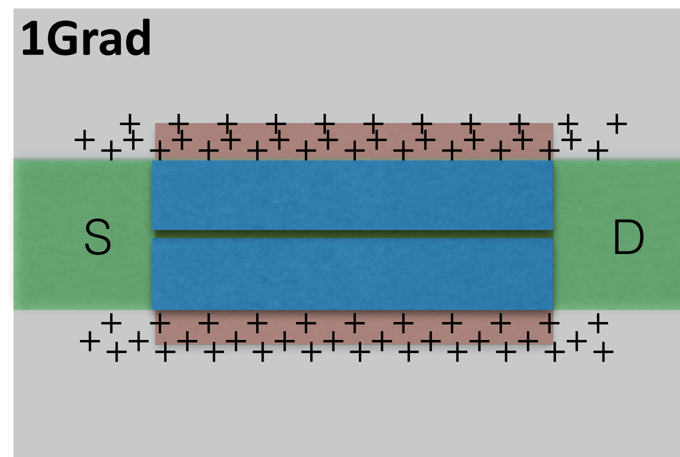
Large recovery!!!

Transistors' size: W=120nm, L=1um
Irradiation conditions:
* T = 25C
* Bias:
  "Vgs" => |Vgs|= 1.2V, Vds=0V
  "Diode" => |Vgs|=|Vds|=1.2V
  "Gnd" =>|Vgs|=Vds=0V

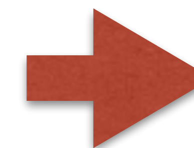




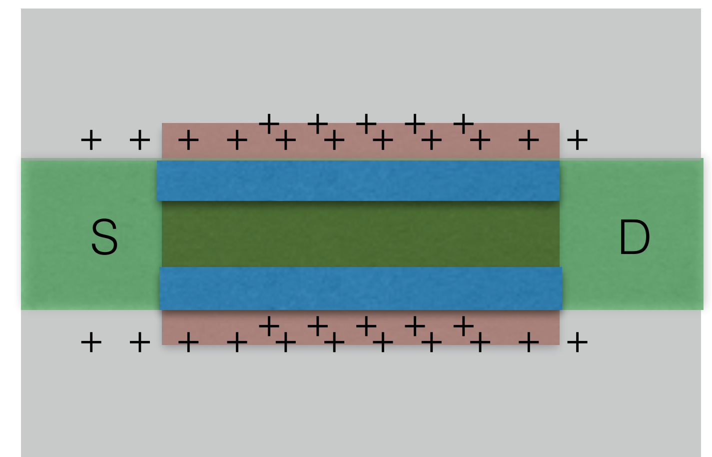




Thermal Energy



Charge trapped in shallow traps is freed

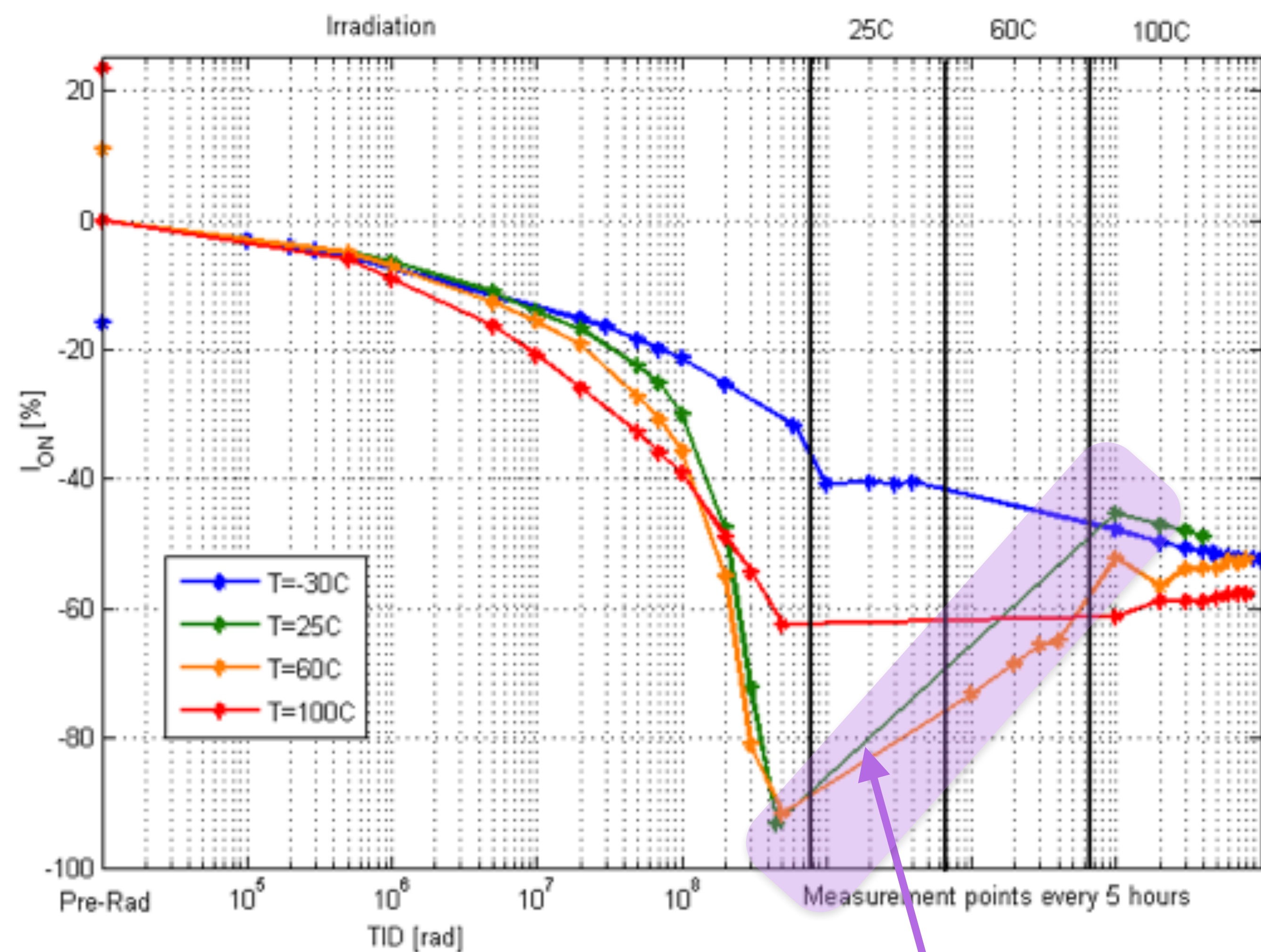


NOTE: In this cartoon, there is no distinction between the positive charge trapped in the oxide or in interface traps; it all appears as positive charge

Influence of TEMPERATURE

RINCE: Radiation damage in PMOS considerably changes with temperature.
At -30C the bias dependence also disappears.

PMOS



Large recovery!!!

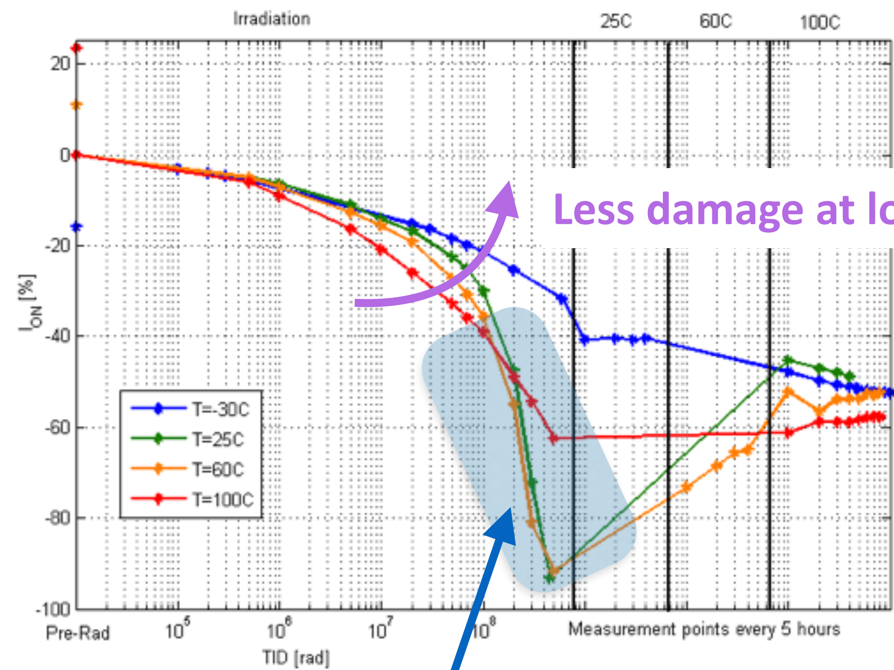
Transistors' size: W=120nm, L=1um
Irradiation conditions:
  * Bias:
    "Diode" => |Vgs|=|Vds|=1.2V

Influence of TEMPERATURE

There are two mechanisms at play:

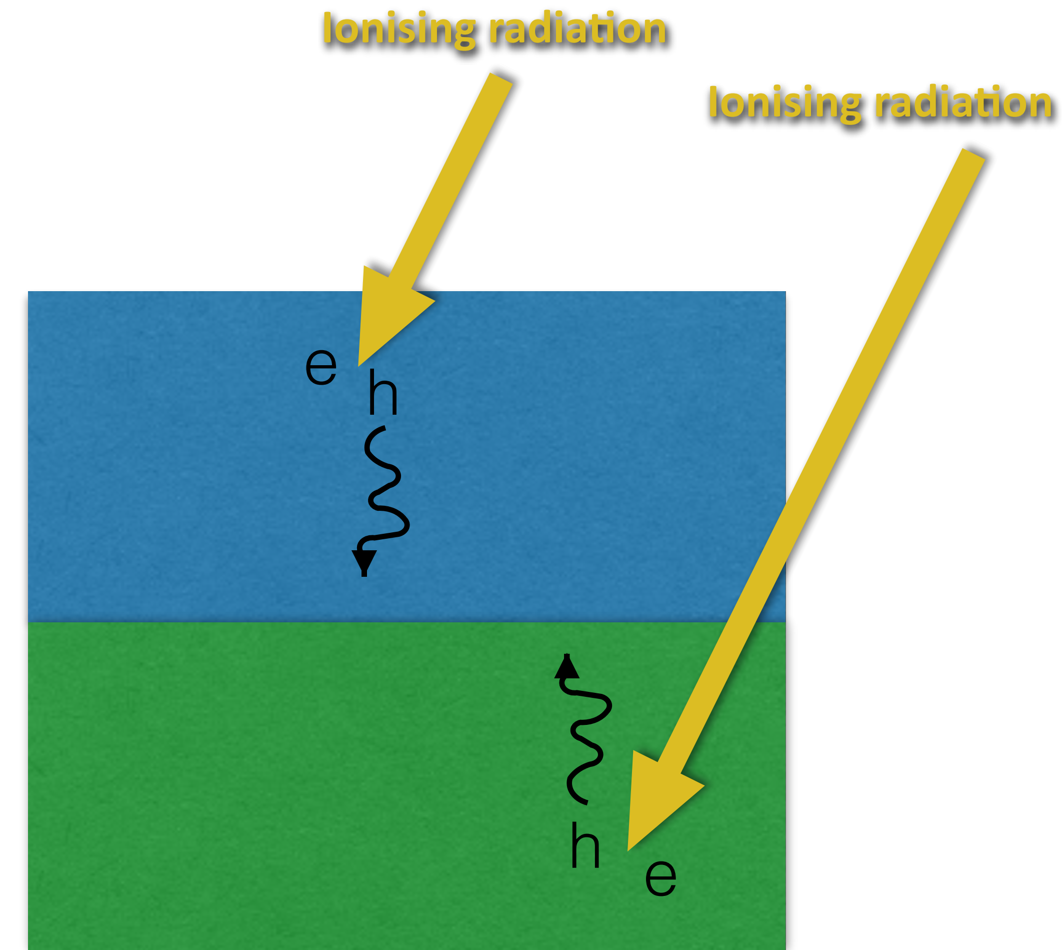
- **smaller damage at low T**
- **larger annealing at high T**

Models for bipolar transistors
(also less damage at low T)



Less damage at low T

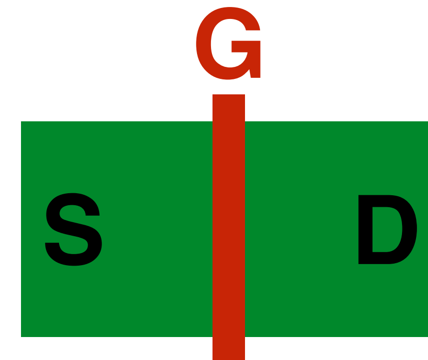
Significant annealing of the damage happens already during irradiation at high T



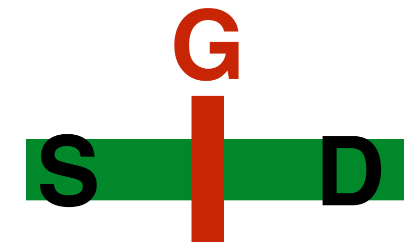
The transport of positive species towards interface is less efficient at high T (and high dose rate)

Narrow channel transistors

Short channel transistors



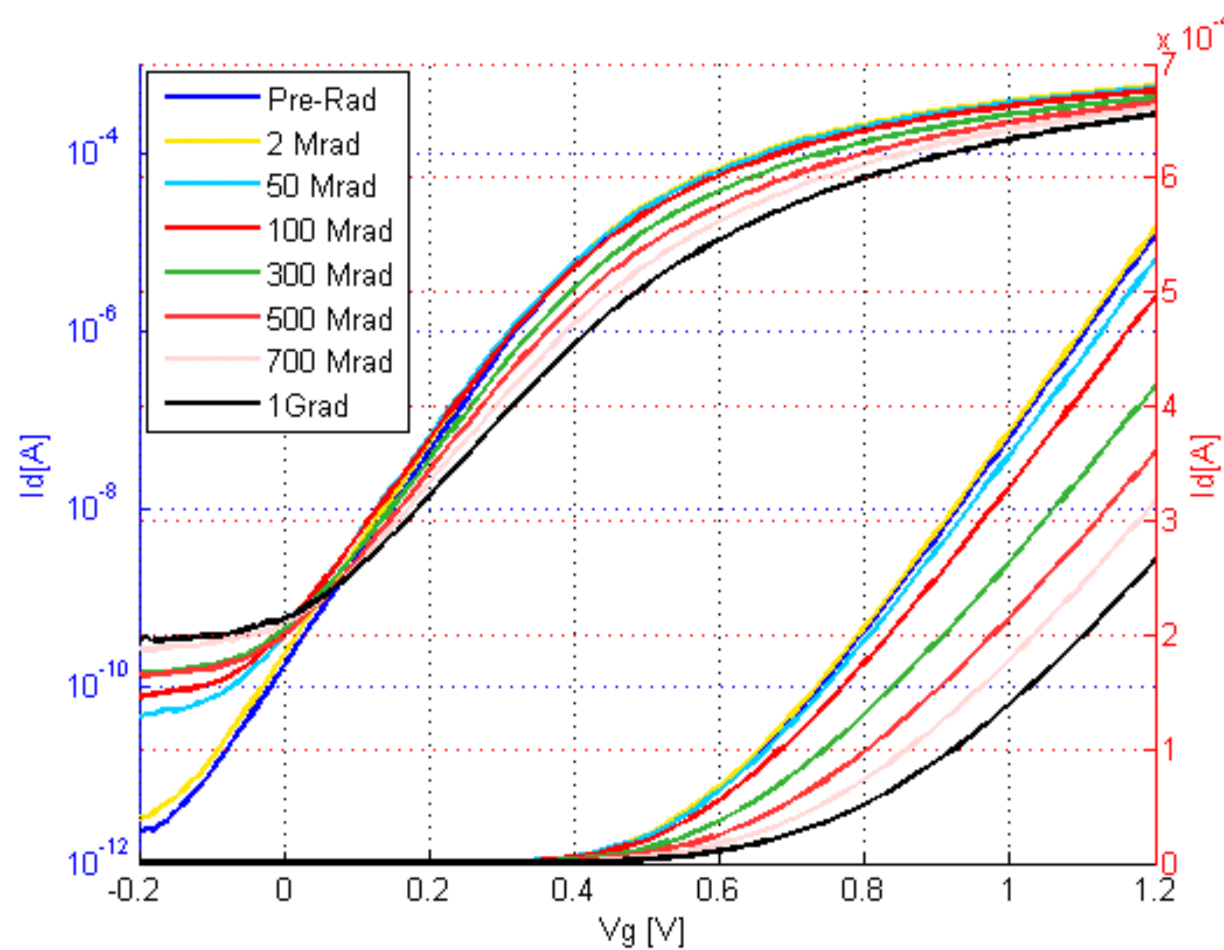
Short and Narrow channel transistors



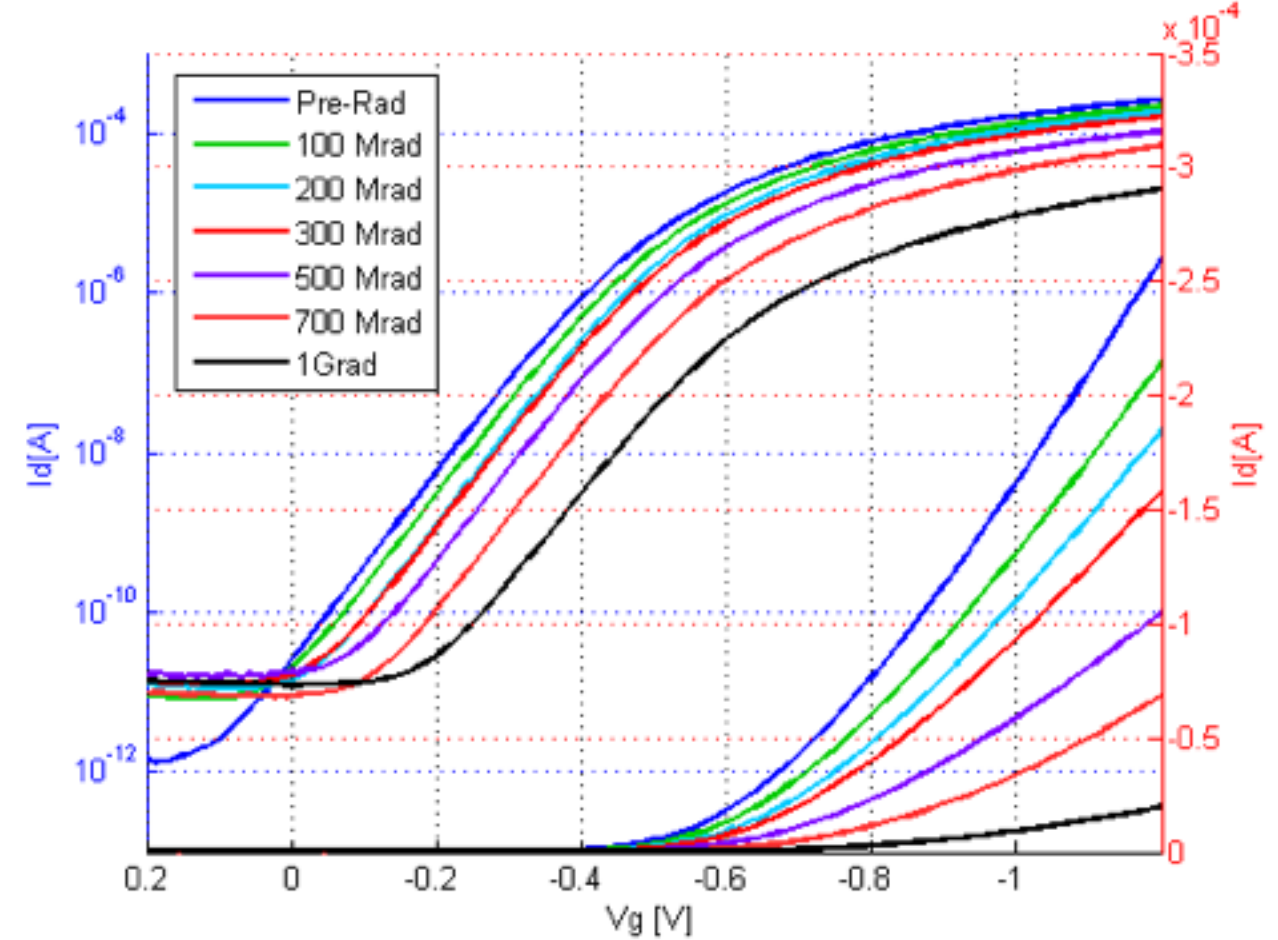
Short channel PMOS are more damaged than NMOS

Damage occurs also in ELT transistors, hence it can not be due to the STI oxide

NMOS

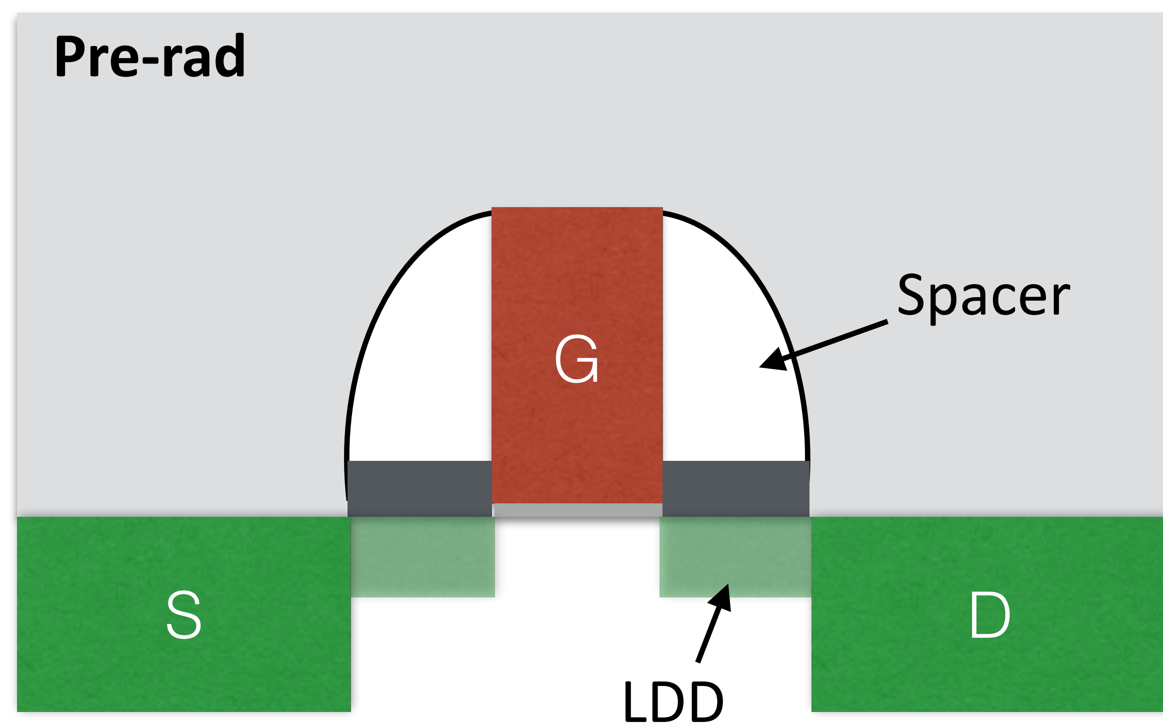


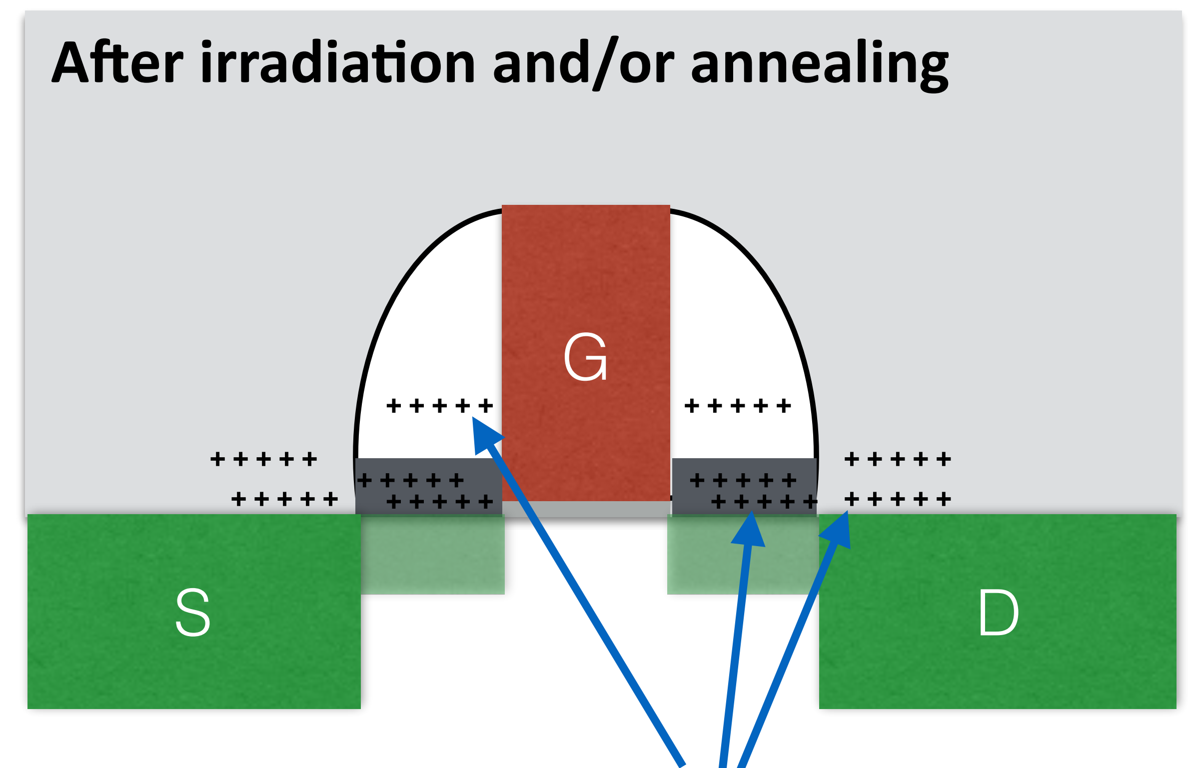
PMOS



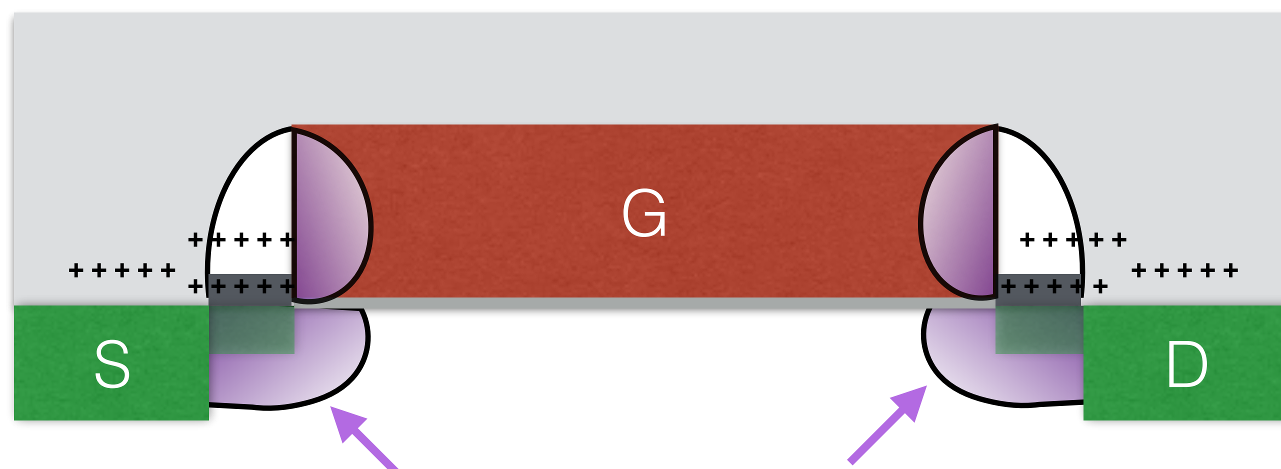
Transistors' size: W=1um, L=60nm
Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V

RISCE can be conceptually represented by this cartoon

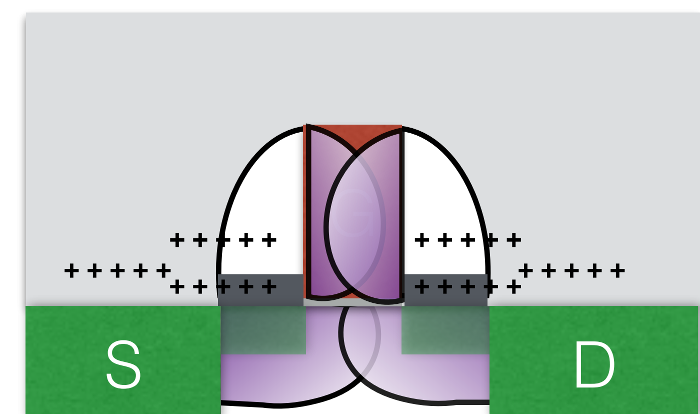




L=moderate size



L=min size



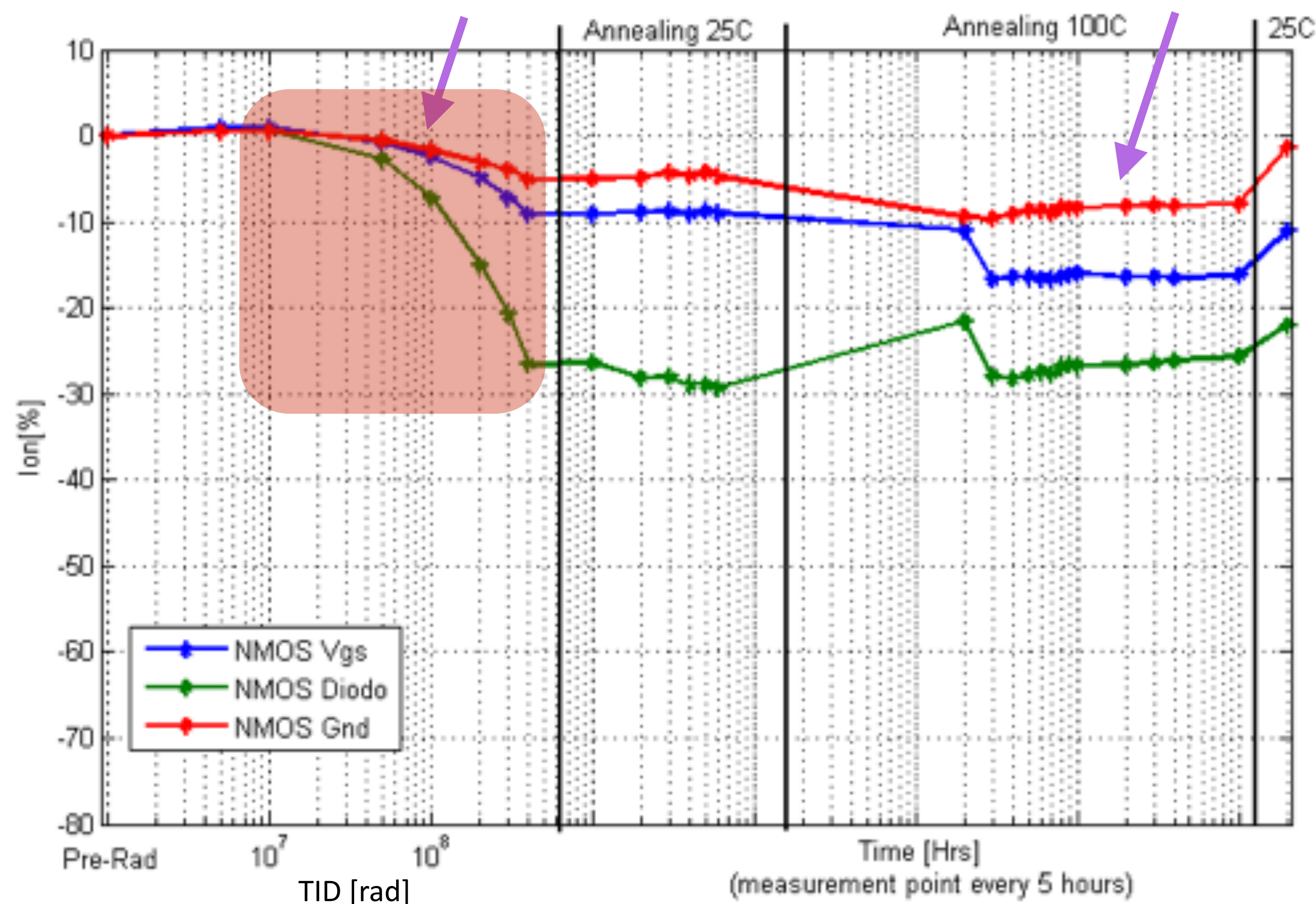
Regions strongly influenced by the trapped charge

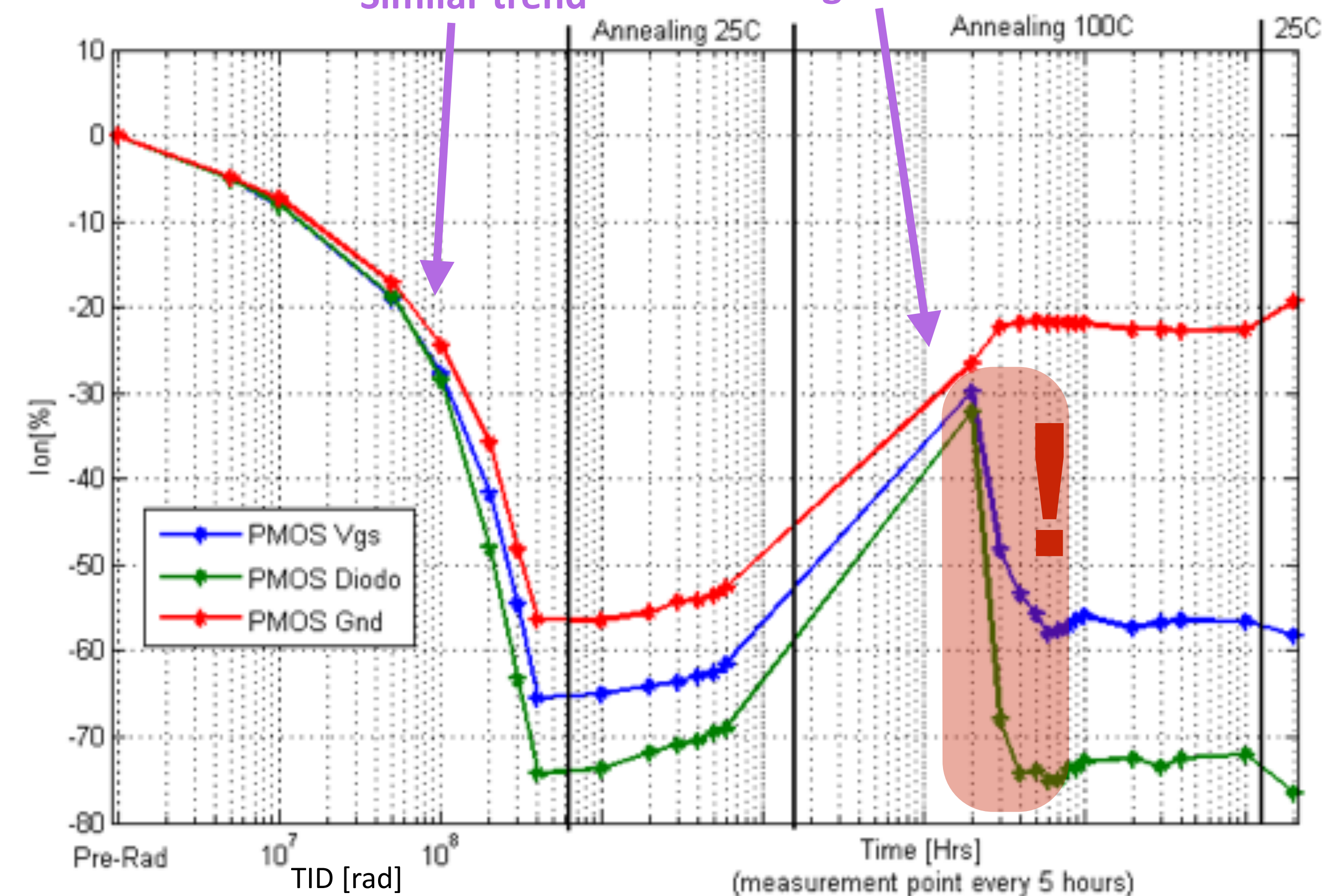
Influence of BIAS

For NMOS, RISCE is very dependent on the bias applied during irradiation

For PMOS, the bias dependence happens rather during high-T annealing

(here the irradiation T is 25C)





Transistors' size: W=0.6um, L=60nm

Irradiation conditions:

- * T = 25C
- * Bias:
  - "Vgs" => |Vgs|= 1.2V, Vds=0V
  - "Diode" => |Vgs|=|Vds|=1.2V
  - "Gnd" =>|Vgs|=Vds=0V

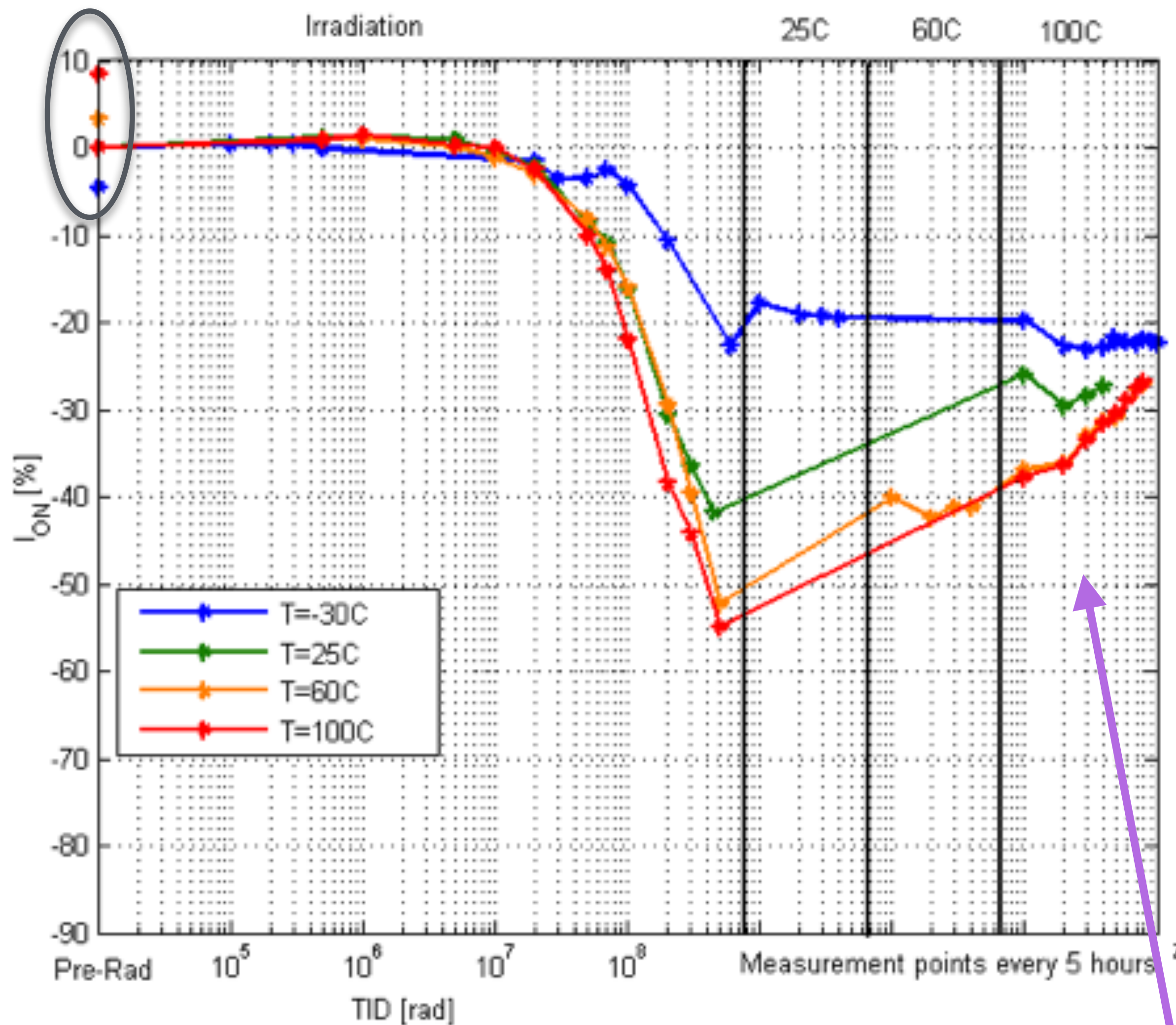
Influence of TEMPERATURE

RISCE: Radiation damage increases with temperature

Transistors are much more tolerant at -30C (and their bias dependence decreases as well)
PMOS have to be kept cold also after exposure!

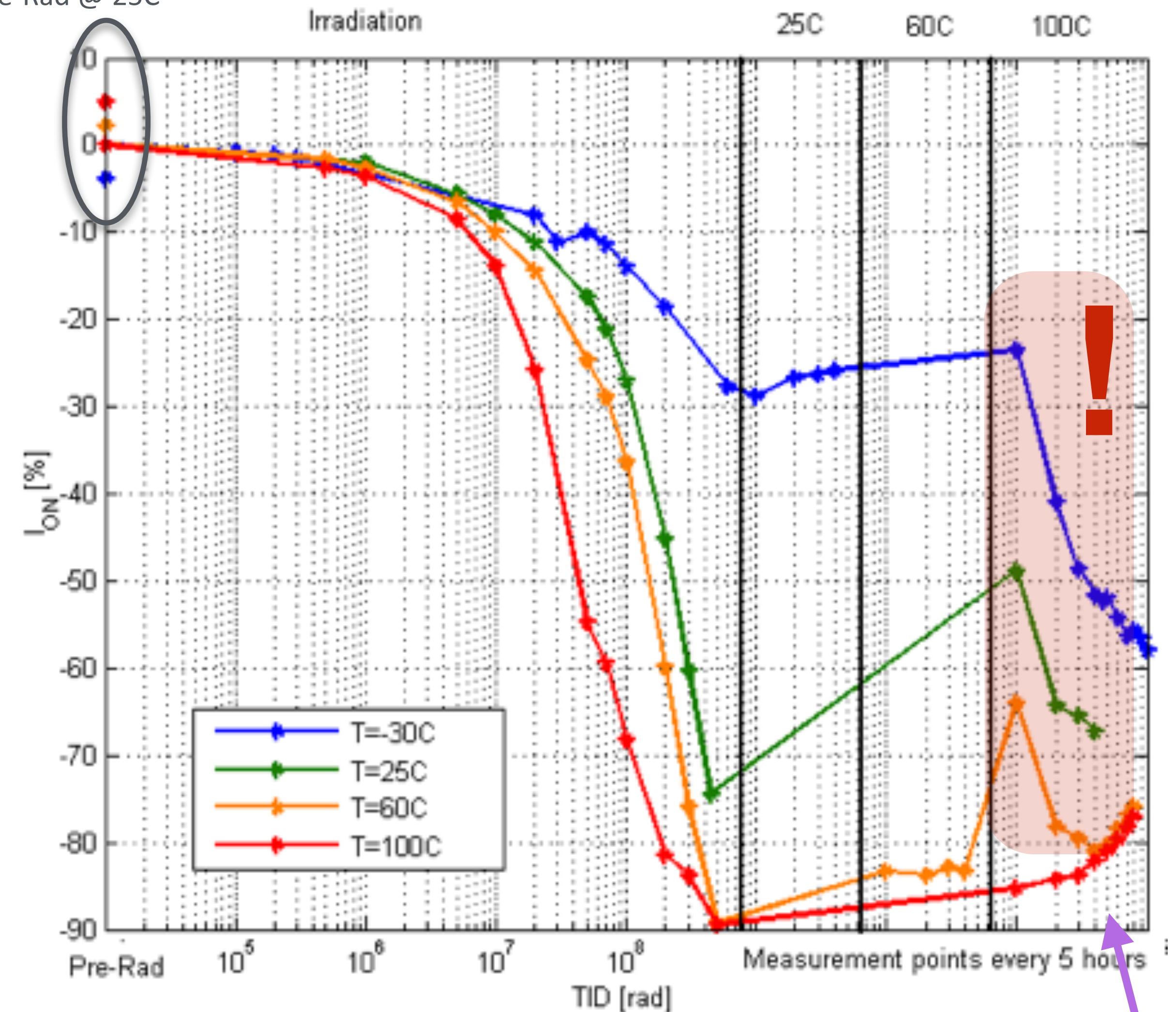
NMOS

Pre-Rad @ 25C



PMOS

Pre-Rad @ 25C



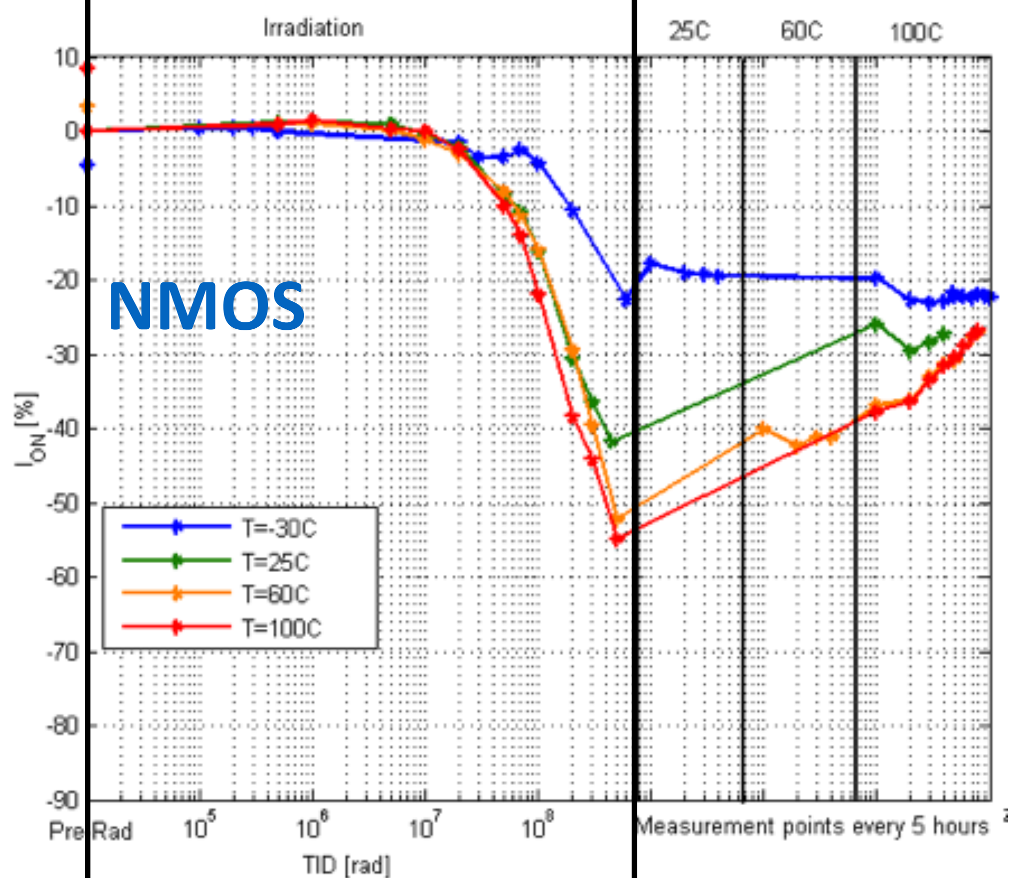
Some recovery at high T
for the most damaged

Relevant degradation at high T
for the less damaged

Transistors' size: W=0.6um, L=60nm
Irradiation conditions:
Bias: |Vgs|=|Vds|=1.2V

NMOS

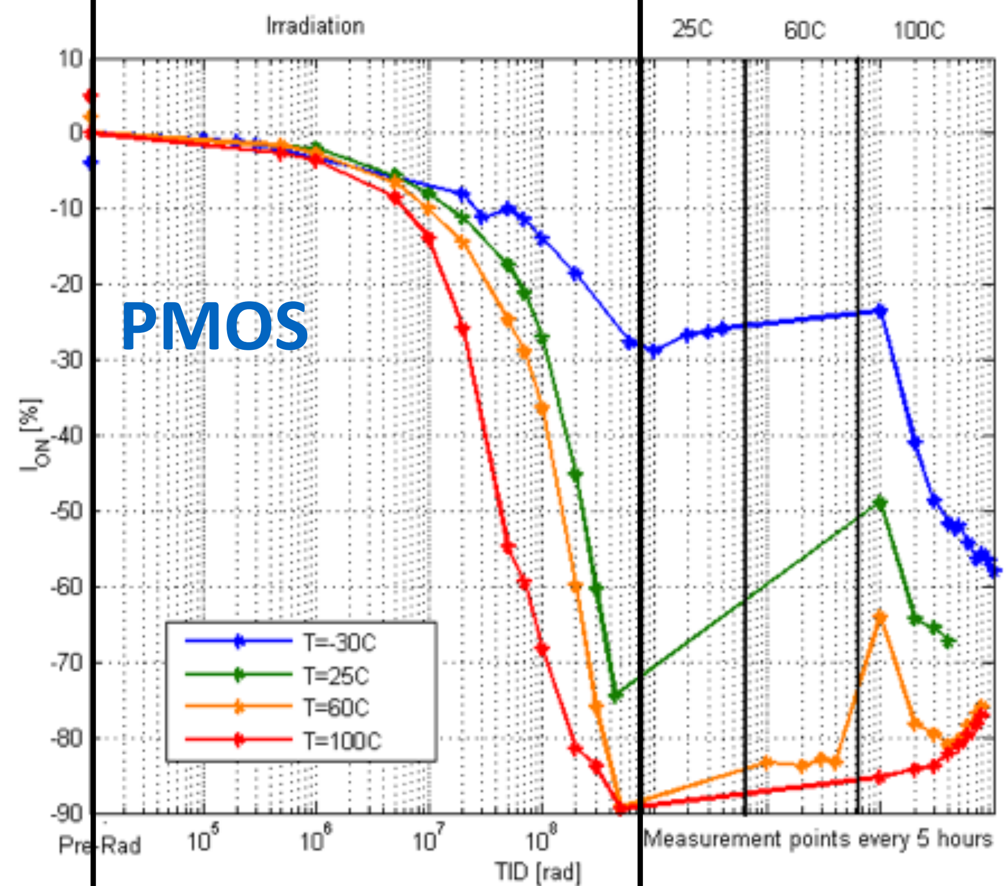
G_m	decrease	20%	no evolution
		45%	recovery
		45%	recovery
		30%	recovery



V_{th}	increase	<50mV	no evolution
		160mV	recovery
		300mV	recovery
		300mV	recovery

PMOS

G_m	decrease	40%	no evolution
		80%	recovery to -40%
		65%*	recovery to -35%*
		30%*	recovery to -20%

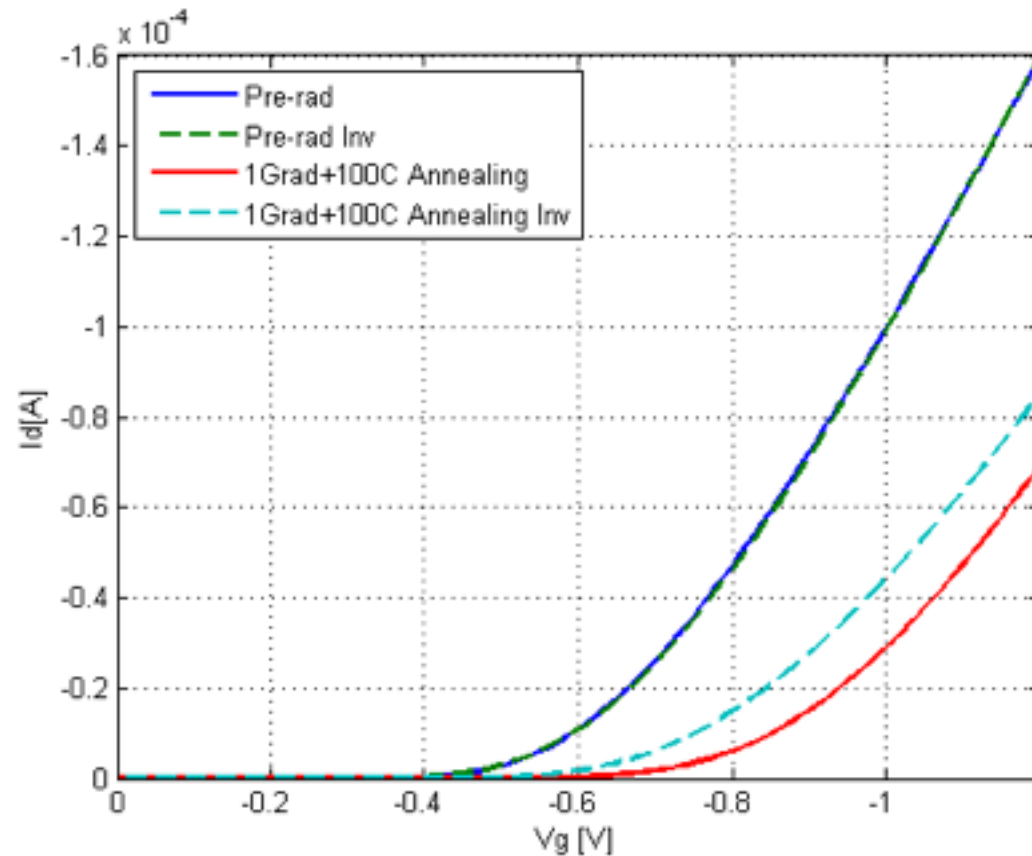


V_{th}	increase	<50mV	increase 250mV
		<50mV	increase 250mV
		370mV	recovery 150mV then increase 150mV
		470mV	recovery 50mV

* = Rough estimate (the peak G_m is out of the V_{gs} range due to V_{th} shift)

In PMOS transistors the shift of V_{th} is accompanied by a source-drain asymmetry

The damage appears to be larger at the source side



Before irradiation: transistor is symmetric

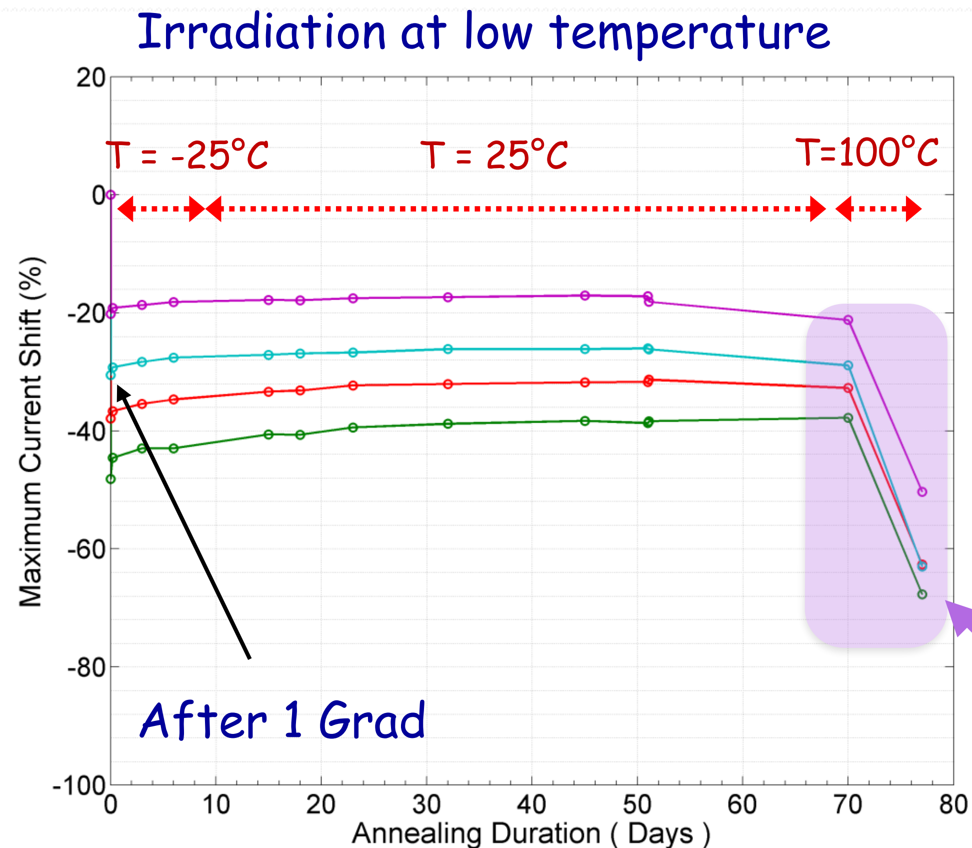
After 1 Grad and annealing at 100C: larger I_{ds} when source-drain are reversed

Transistors' size: W=1um, L=60nm
Irradiation conditions:
T=25C
Bias: |Vgs|=|Vds|=1.2V

In NMOS transistors measurements on symmetry are not consistent

No conclusion can be reached on possible radiation-induced asymmetry

The post-irradiation evolution (V_{th} shift) is clearly a thermally activated process



From M.Menouni et al., talk at the RD53 Radiation working group, Dec.14

Transistors with L=60nm and different W irradiated at -30C with "Diode" bias: |Vgs|=|Vds|=1.2V (also during annealing)

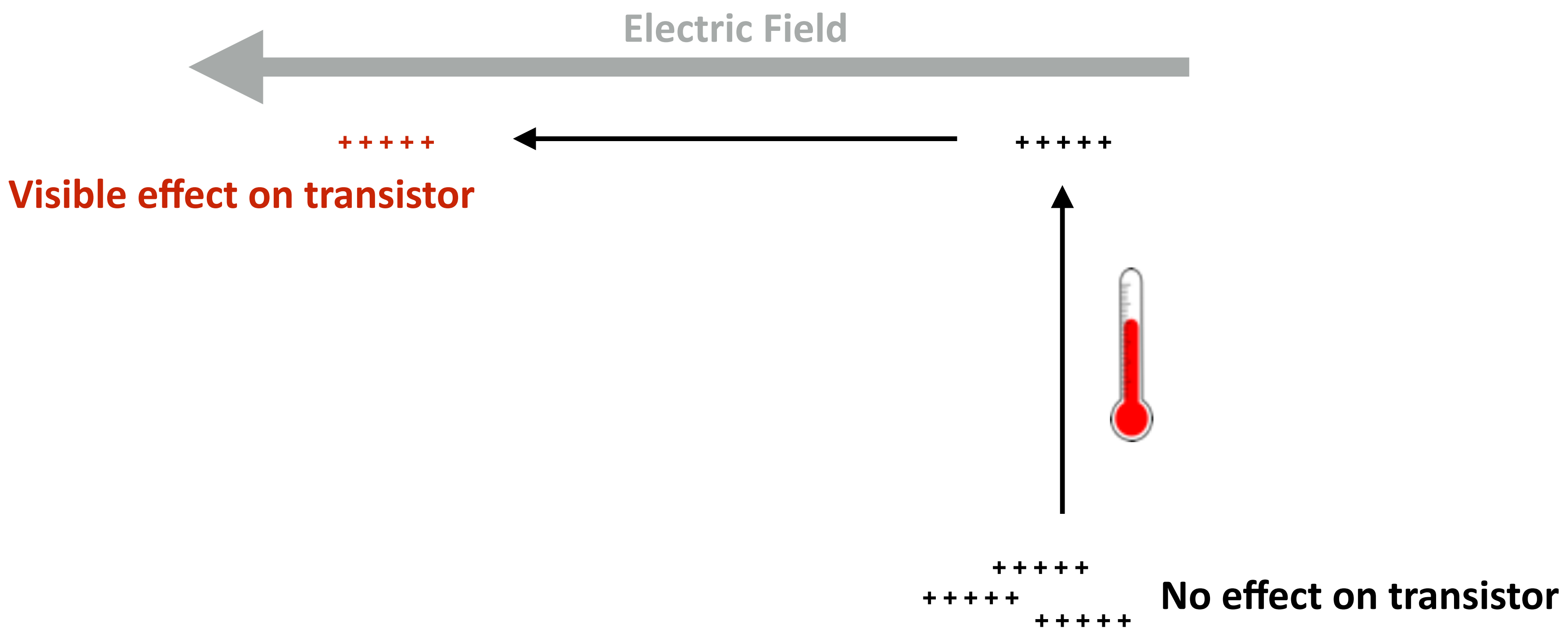
V_{th} shifts when T is raised after 70 days at room T!

Also, If no bias is applied in the first few hours when T is raised at 100°C then there is no V_{th} shift when bias is applied

Sequence				Result
irradiation	anneal 25C	anneal 100C, |Vgs|=|Vds|=1.2V		Vth shift
irradiation	anneal 25C	anneal 100C, |Vgs|=|Vds|=0V	anneal 100C, |Vgs|=|Vds|=1.2V	NO Vth shift

Thermal energy AND bias are needed at the same time for the damage to appear

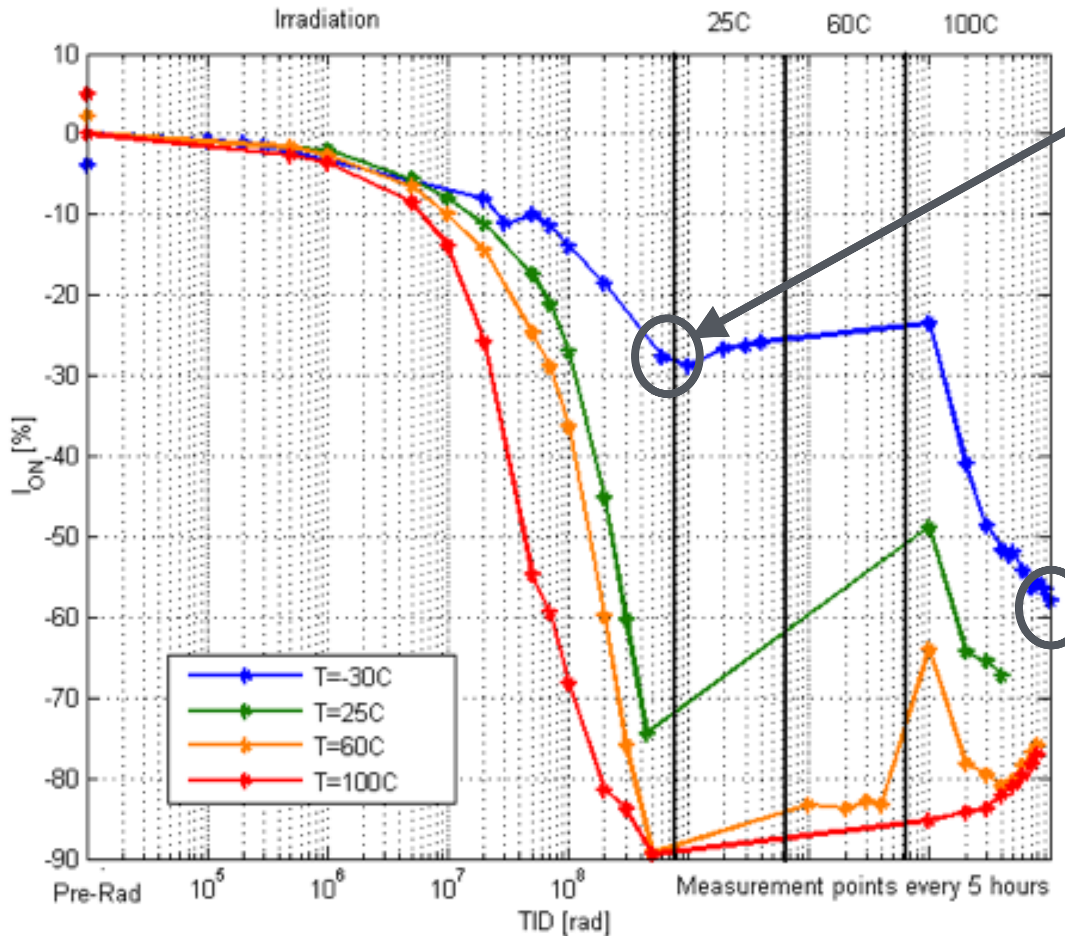
… as if thermal energy allows the migration of charges, and bias drives them in the 'right' place for the damage to appear



Thermal energy AND bias are needed at the same time for the damage to appear

What is the activation energy, and can this still happen at low T over long times???

(damage at high dose rate and low T is much smaller: is this representative of the damage in the application?)



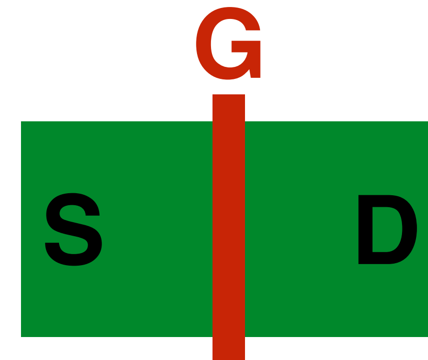
Is this representative (-28%)....

... or this (-60%)????

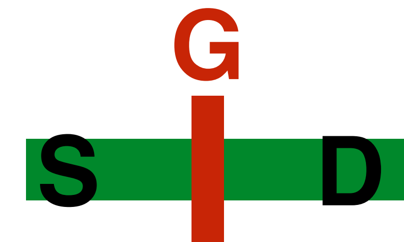
... or something else?

Narrow channel transistors

Short channel transistors

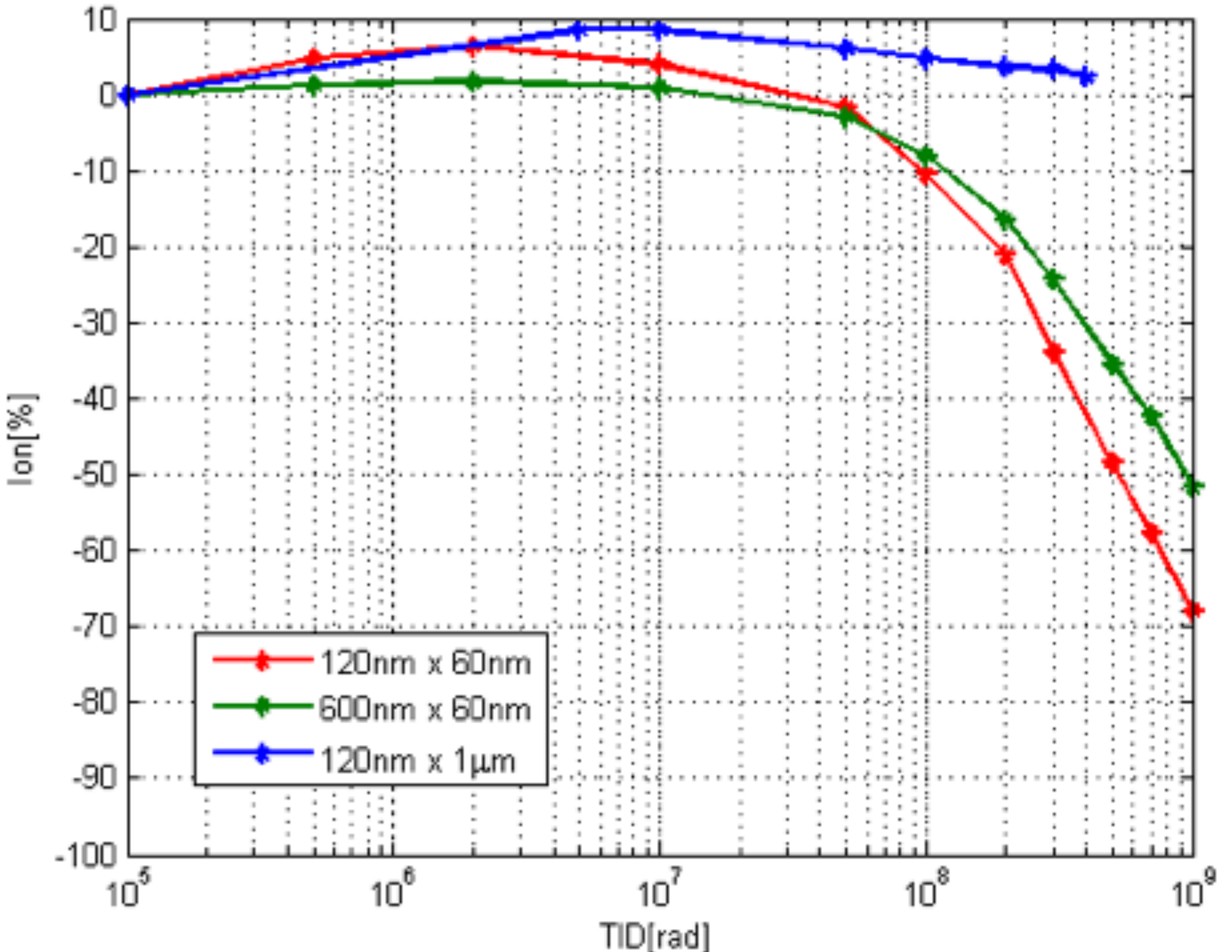


Short and Narrow channel transistors

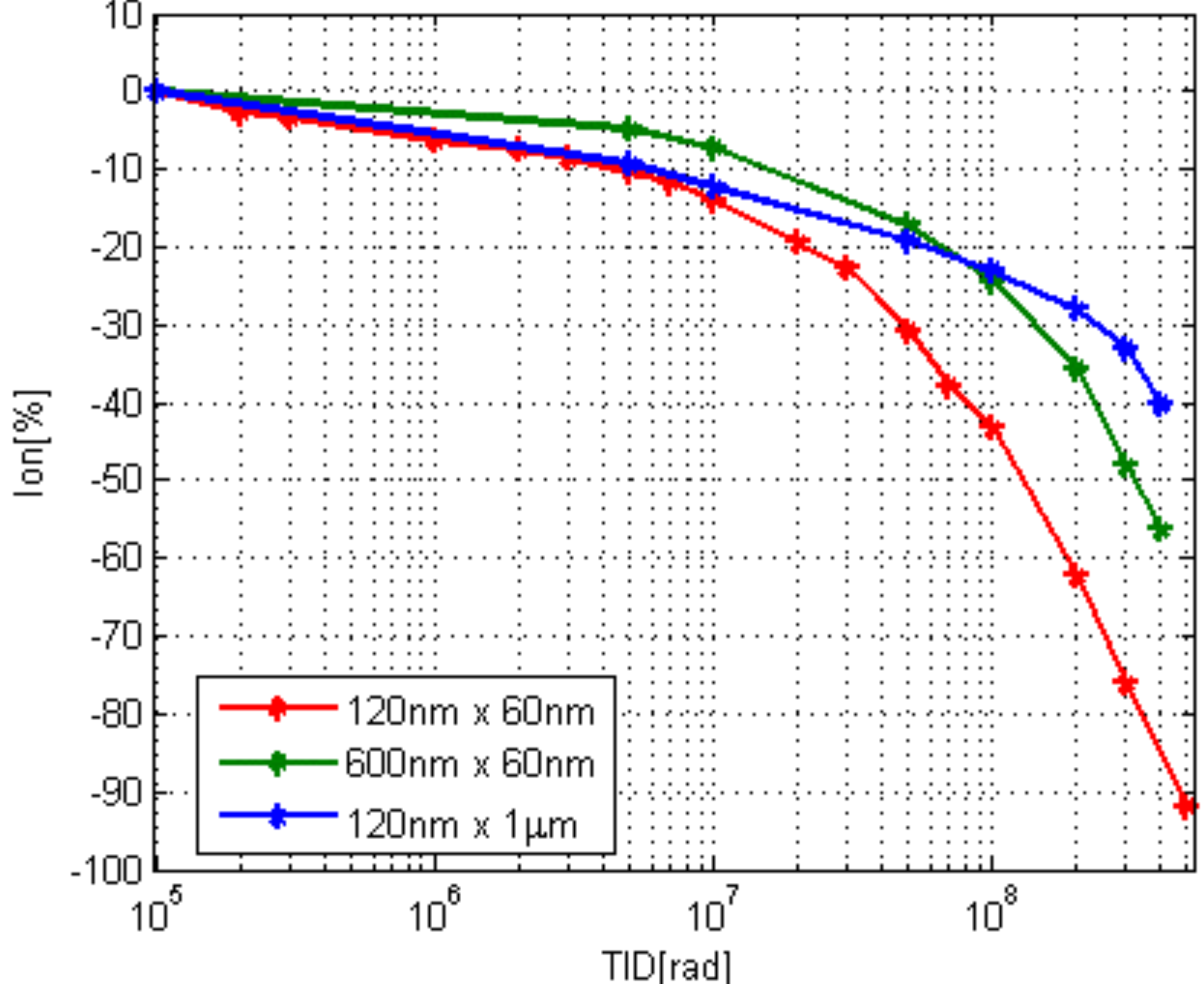


Short AND Narrow transistors are simultaneously affected by RISCE and RINCE, hence their degradation is the worst measured

NMOS



PMOS



Irradiation conditions:
* T = 25C

* Bias NMOS:
  "Diode" => |Vgs|=|Vds|=1.2V

* Bias PMOS:
  "Gnd" =>|Vgs|=Vds=0V

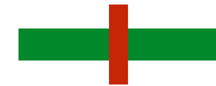
What was measured?

TID-induced degradation of the electrical performance (I_{on})

Narrow channel transistors

Short channel transistors

Short and Narrow channel transistors



Results from Negative Bias Thermal Instability stresses (combined with TID)

Results from Hot Carrier Injection stresses (combined with TID)

Variability of the TID-induced degradation

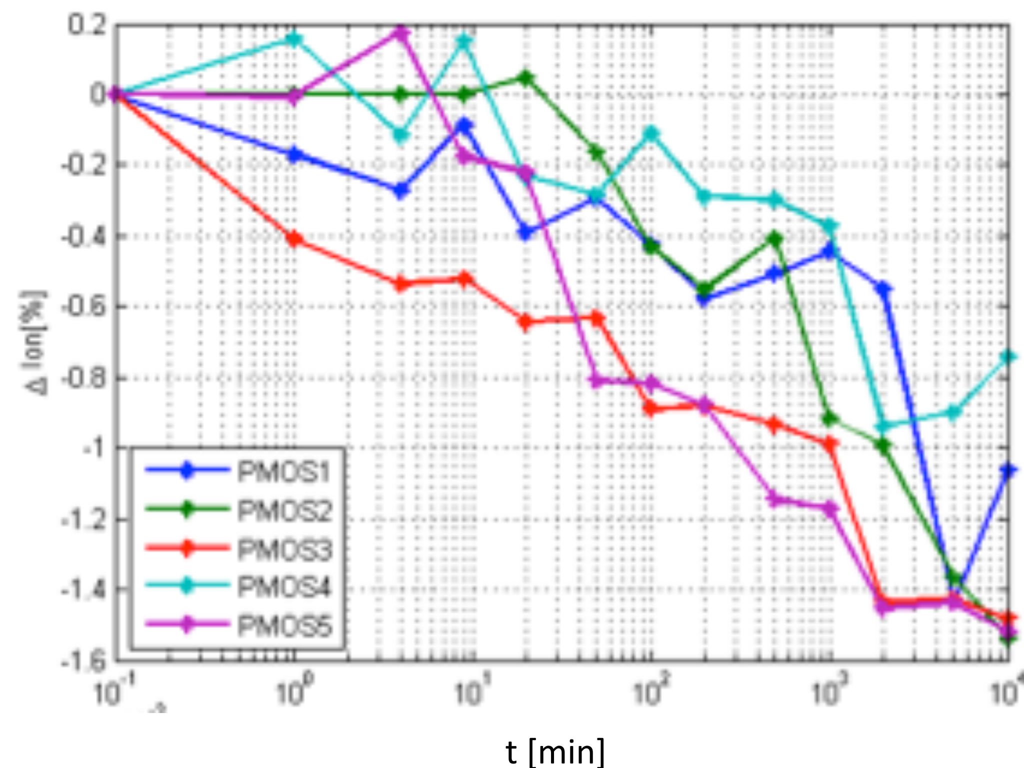
An NBTI stress is a procedure where negative gate voltage and high temperature are applied simultaneously for a long time on PMOS transistors, observing their performance degradation.

(There is a large and rapid evolution after the stress, complicating the experiment)

Fresh PMOS transistors (not irradiated), W=1um, L=60nm

Stress conditions:

- Vgs=-1.2V
- T=100C



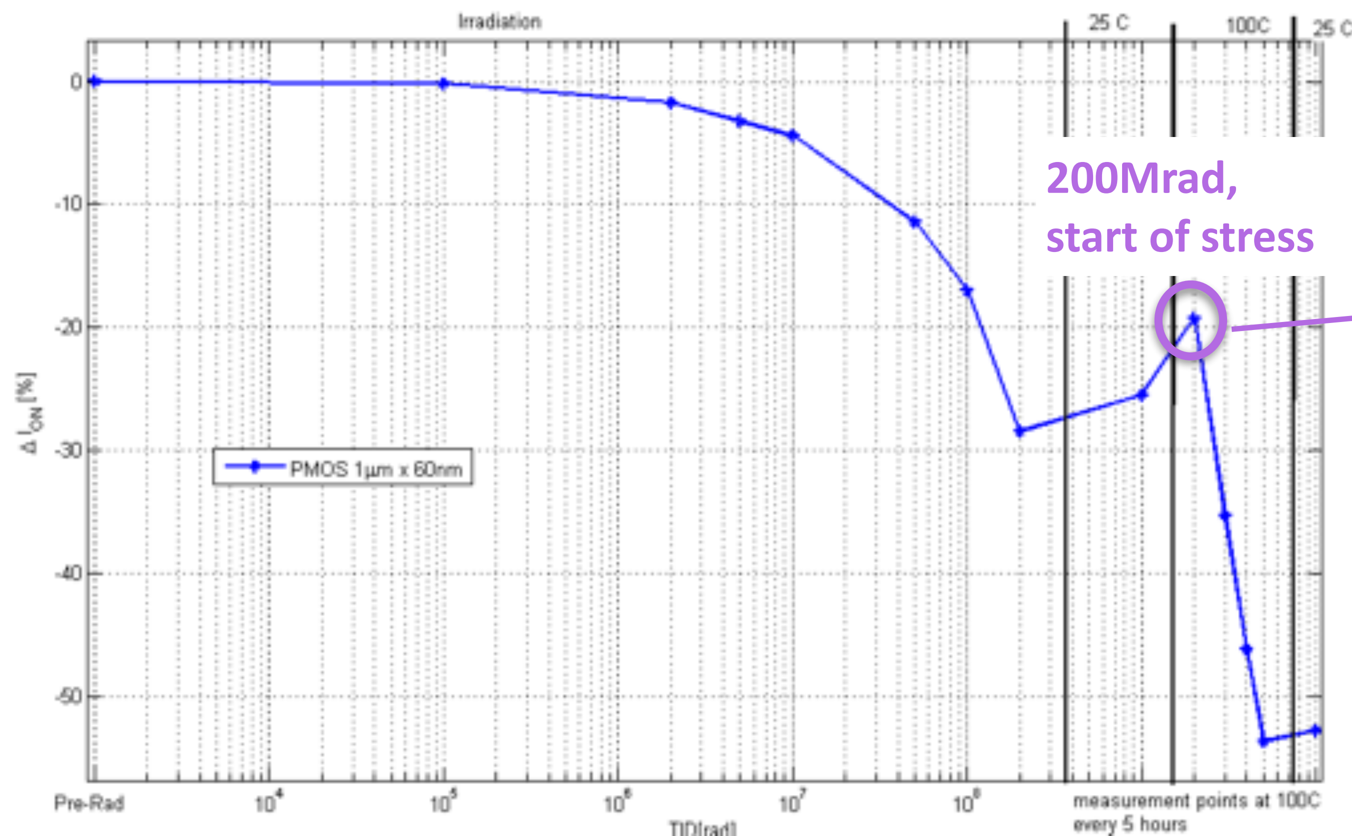
Small degradation (≈1%) after 10,000 minutes of stress (measurements taken within 3 minutes after each stress)

NBTI stresses at different T have been applied to PMOS samples irradiated to 200Mrad in the same conditions (size: W=1um, L=60nm)

(There is a large and rapid evolution after the stress, complicating the experiment)

Irradiation conditions:

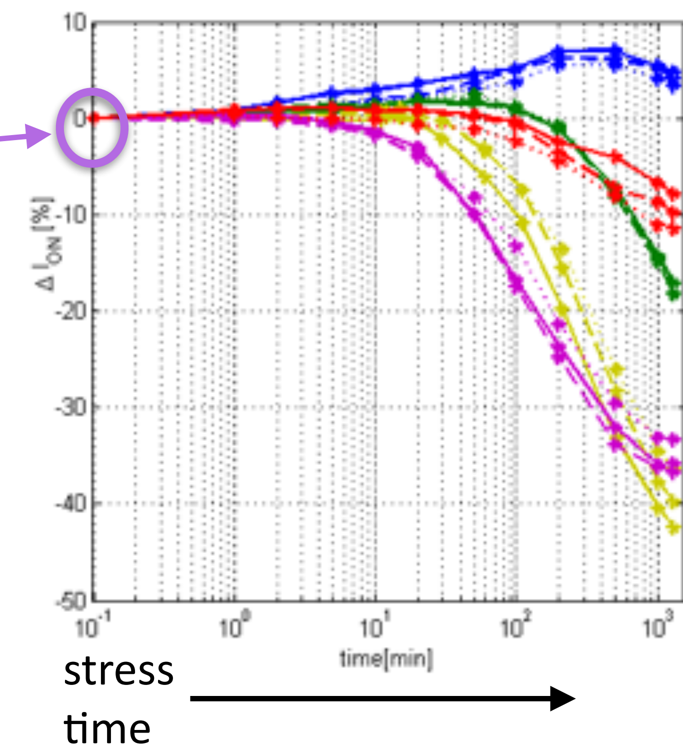
- Vgs=Vds=0V
- T=25C



Stress conditions:

- Vgs=-1.2V
- T=60 to 140C
- time=1300min

Each color is a different chip, 3 transistors/chip

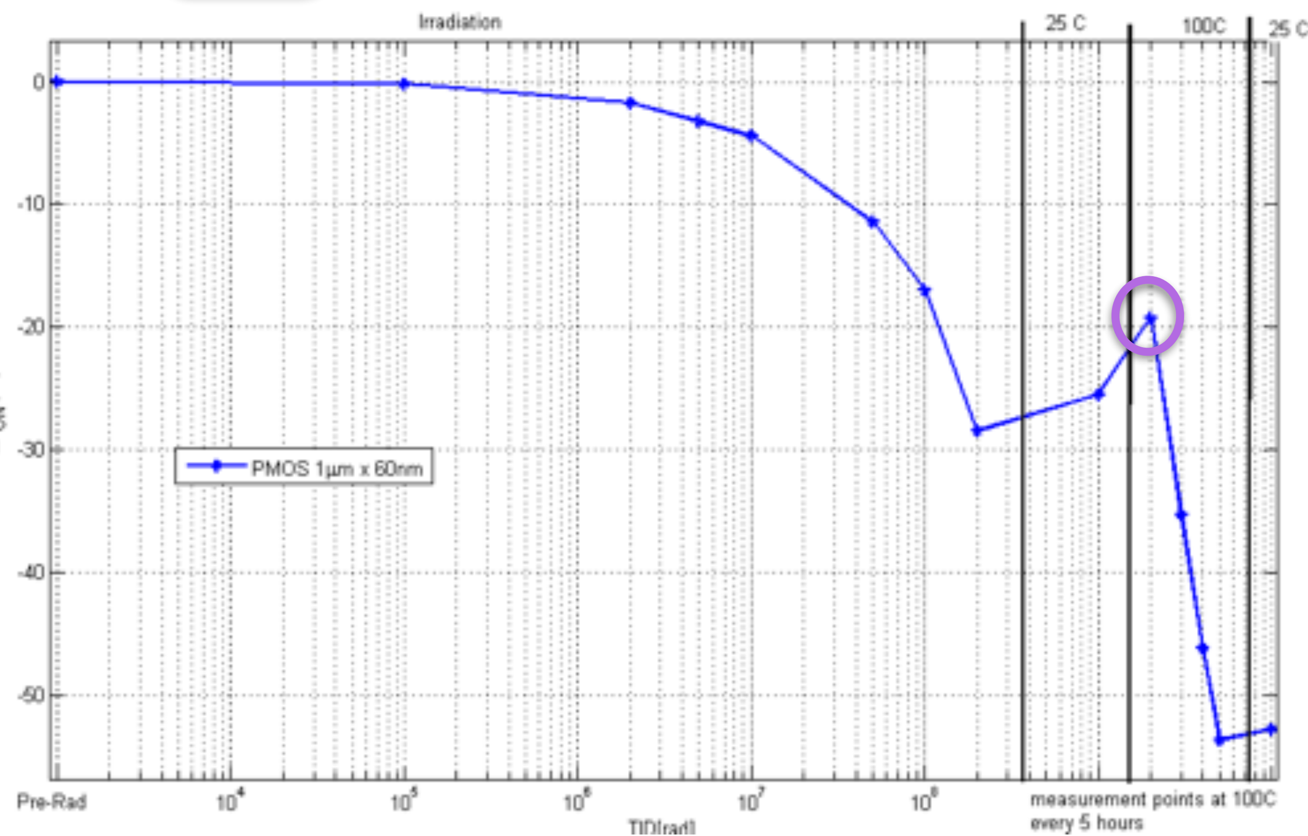


The objective of the test was the extraction of an "activation energy" for the post-irradiation evolution

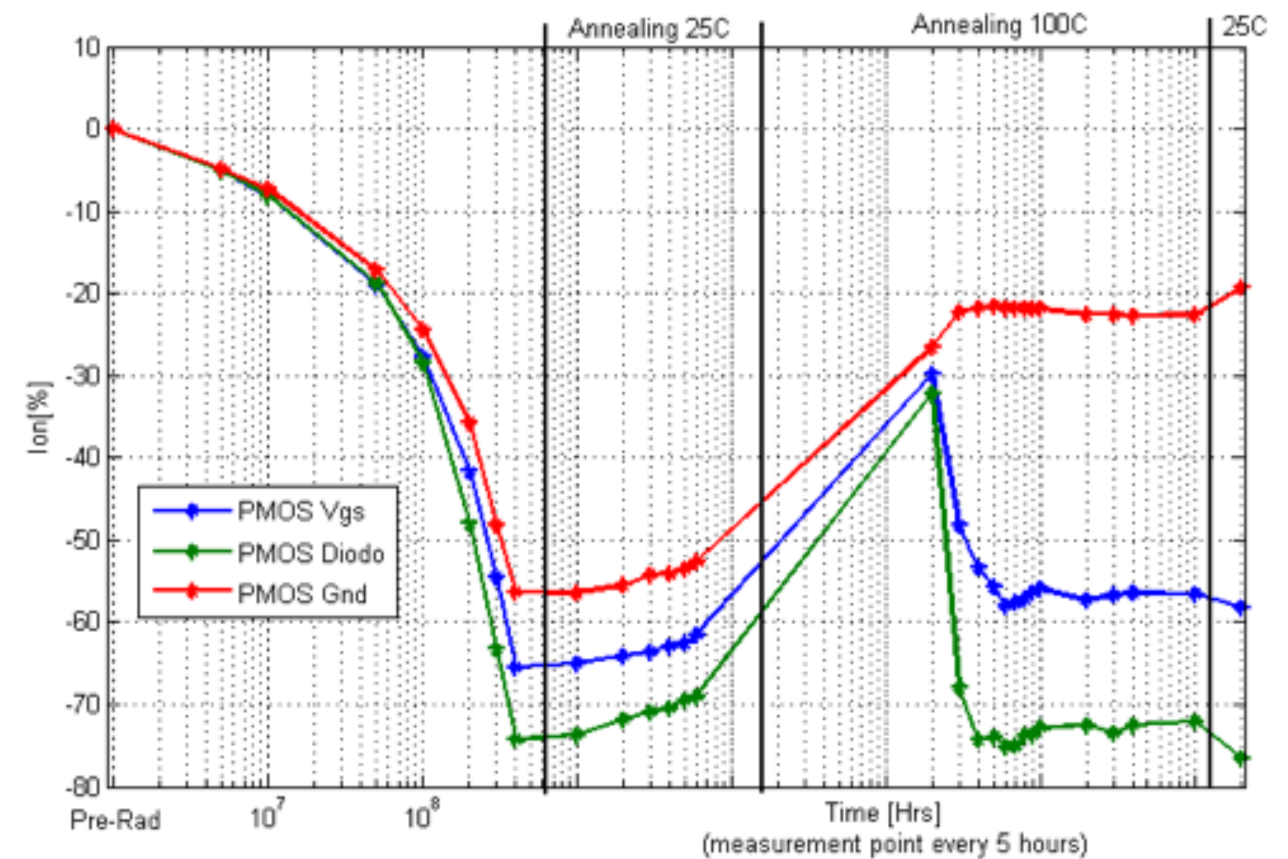
The procedure is the same used for all irradiated samples: irradiation, annealing at room T, annealing at hight T

(however now the annealing at room T is as short as possible while the high T annealing takes place at different temperatures for different samples - all other conditions being the same!)

"NBTI" study (here the stress is at 100C)



Irradiation study (here the "annealing" is at 100C)



What is normally "annealing" at 100C is now "NBTI" at different T

The evolution of the degradation is not monotonic. We can not extract an activation energy!

(More than one phenomenon is responsible for the evolution)

ΔI_{ON} [%]

time[min]

60C

140C

80C

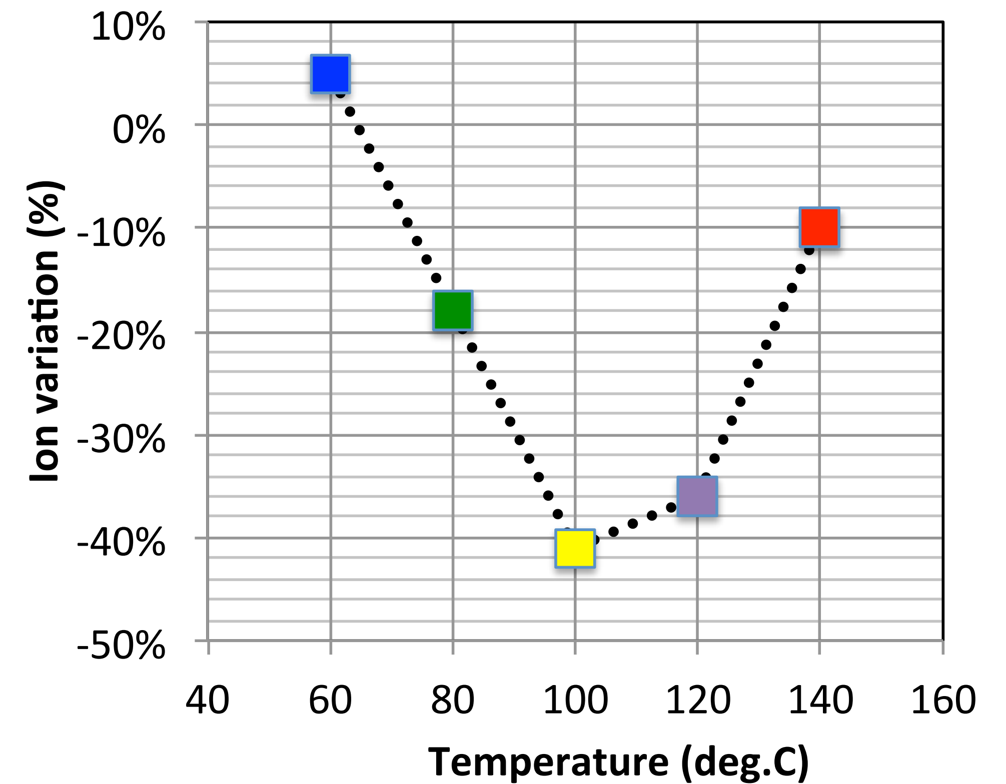
120C

100C

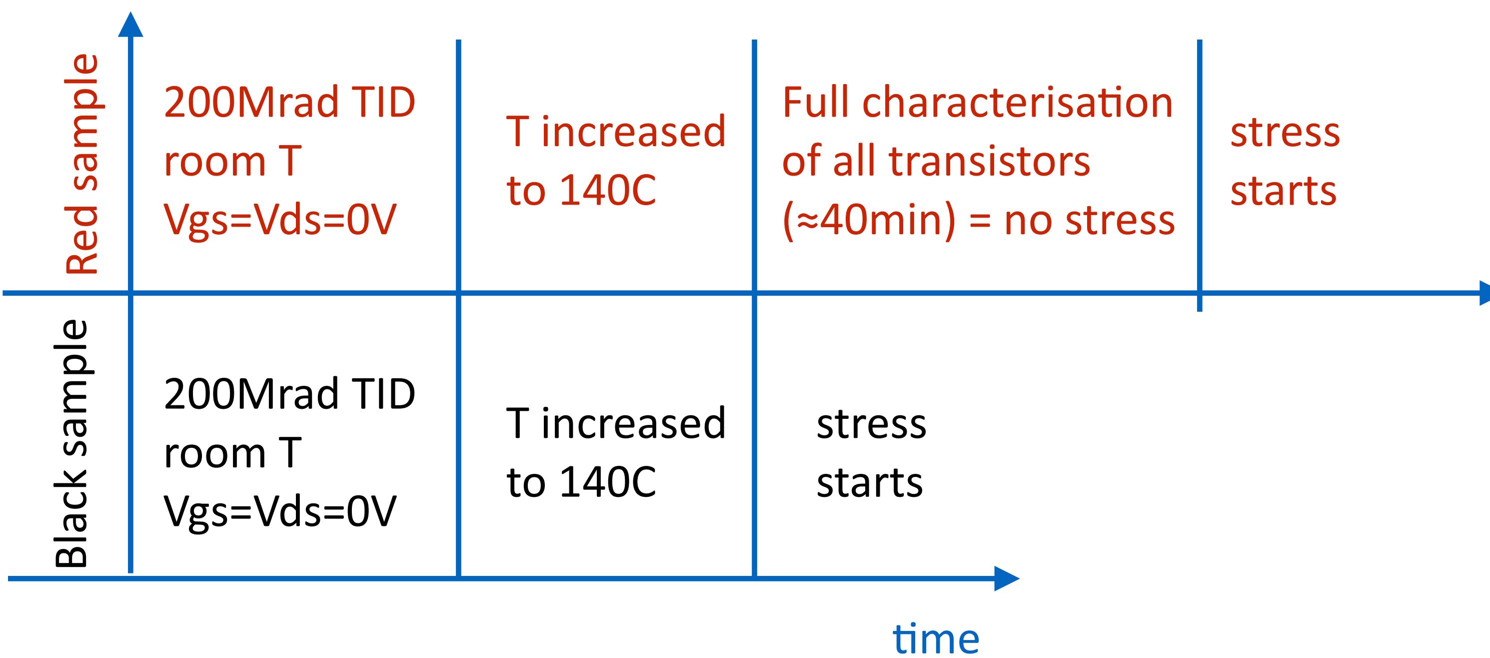
200Mrad,
start of stress

What will happen at longer times????

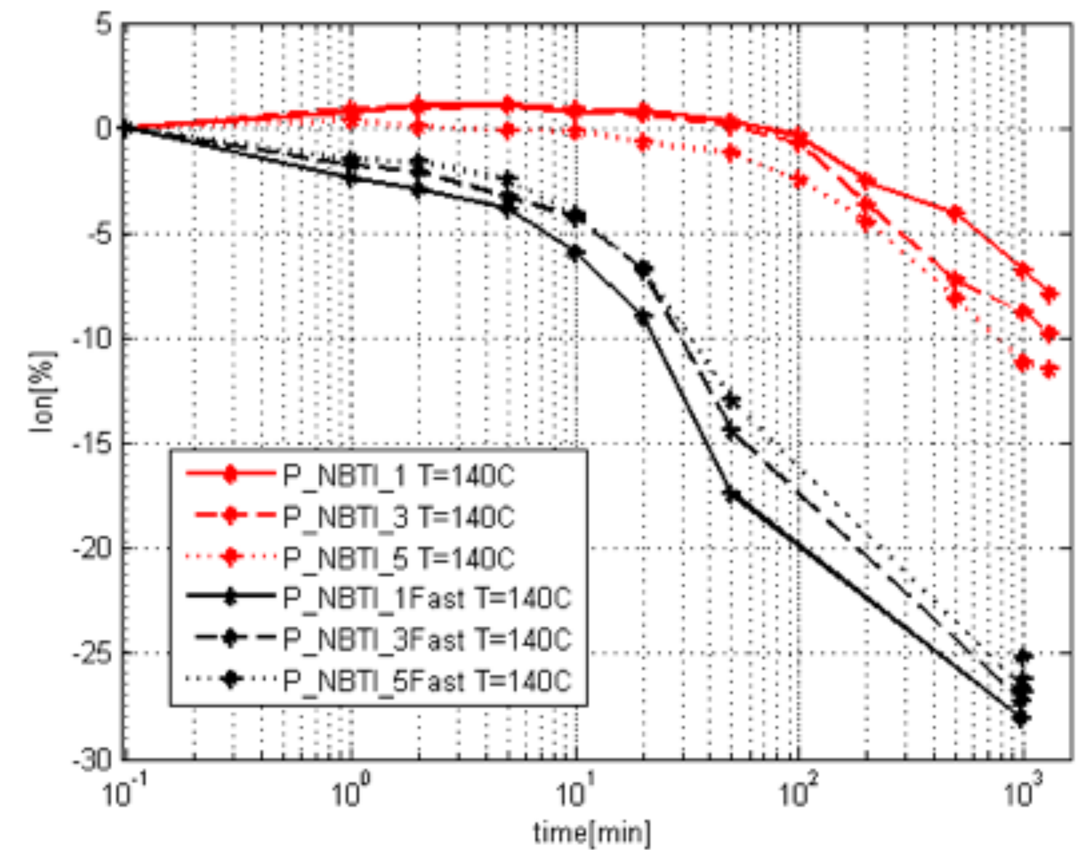
The Ion variation induced by the NBTI stress after 1300 minutes peaks at 100C



The evolution of the degradation is strongly dependent on the detailed story of the sample



The large difference in evolution is due to the red sample being kept for less than one hour at 140C before the stress!



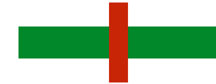
What was measured?

TID-induced degradation of the electrical performance (I_{on})

Narrow channel transistors

Short channel transistors

Short and Narrow channel transistors



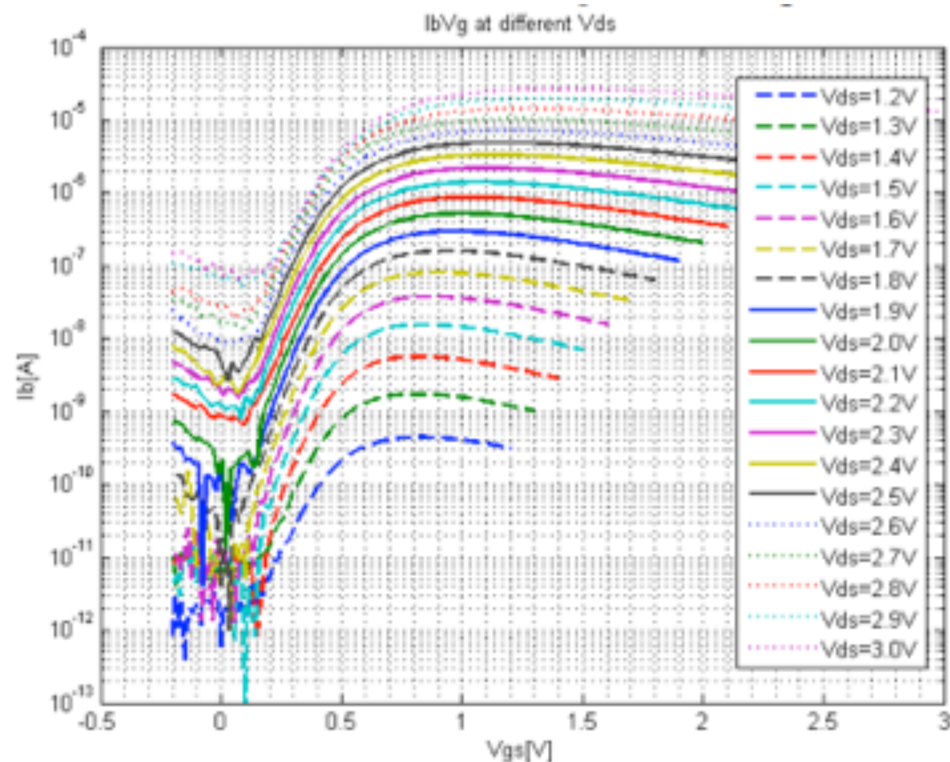
Results from Negative Bias Thermal Instability stresses (combined with TID)

Results from Hot Carrier Injection stresses (combined with TID)

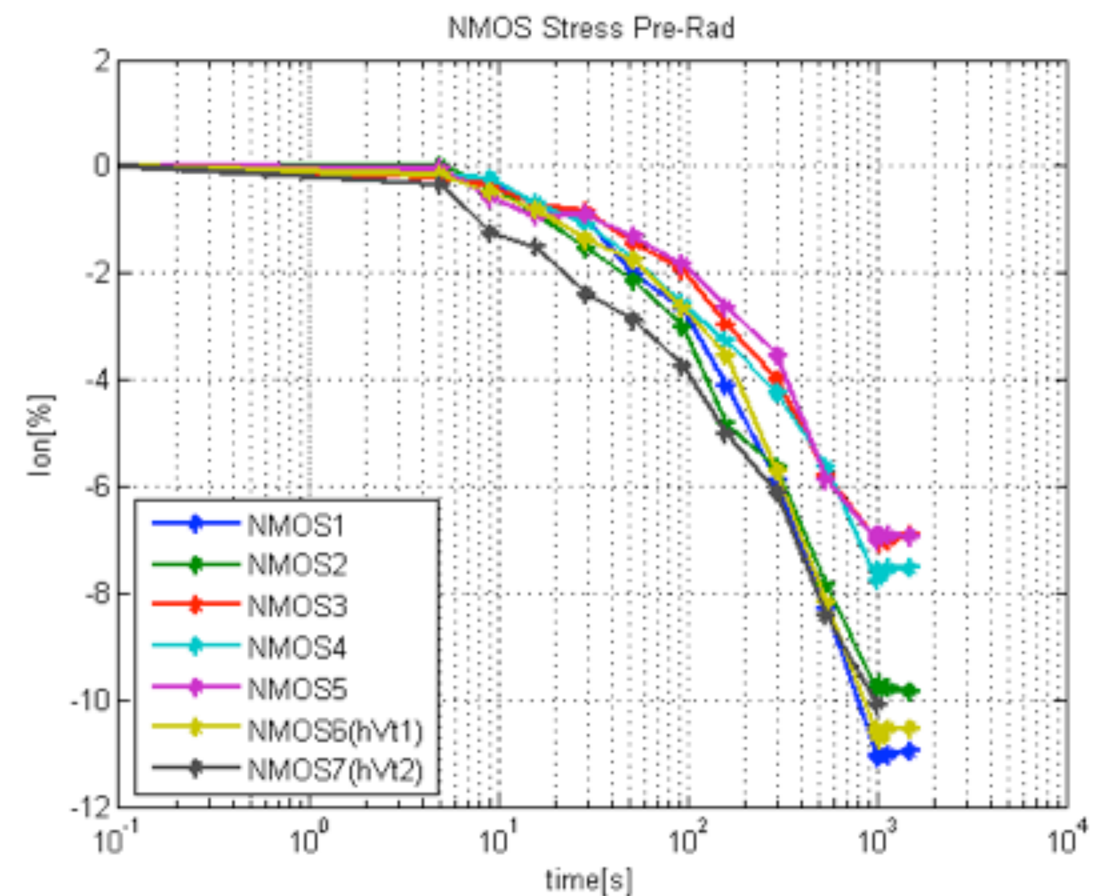
Variability of the TID-induced degradation

An HCI stress is a procedure where a pre-defined bias (normally well exceeding the nominal voltages of the technology) is applied to the transistor for a limited time, degrading its characteristics

1. Measurements to define the appropriate stress bias



2. Application of the stress and measurements of the transistor's degradation



Chosen conditions:

- NMOS: Vgs=1.1V, Vds=2.3V
- PMOS: different stress conditions used and compared: Vds=-2.6 to -3V, Vgs=-1.2 to -0.5V

A set of measurements was performed to study the correlations between TID irradiation and Hot Carriers Injection damage

Irradiation was done at room T and with 'Vgs' bias: |Vgs|=1.2V, Vds=0V
The size of the studied transistors is W=1um, L=60nm

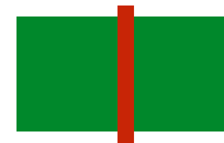
	NMOS	PMOS
First **HCI** Then **Irradiation** Only **HCI** Only **Irradiation**		
First **Irradiation** Then **HCI**	Worse HCI damage after irradiation (a few %)	HCI after irradiation leads to recovery (radiation damage is so large than anything seems to contribute to the recovery)

What was measured?

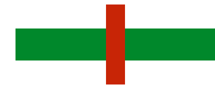
TID-induced degradation of the electrical performance (I_{on})

Narrow channel transistors

Short channel transistors



Short and Narrow channel transistors

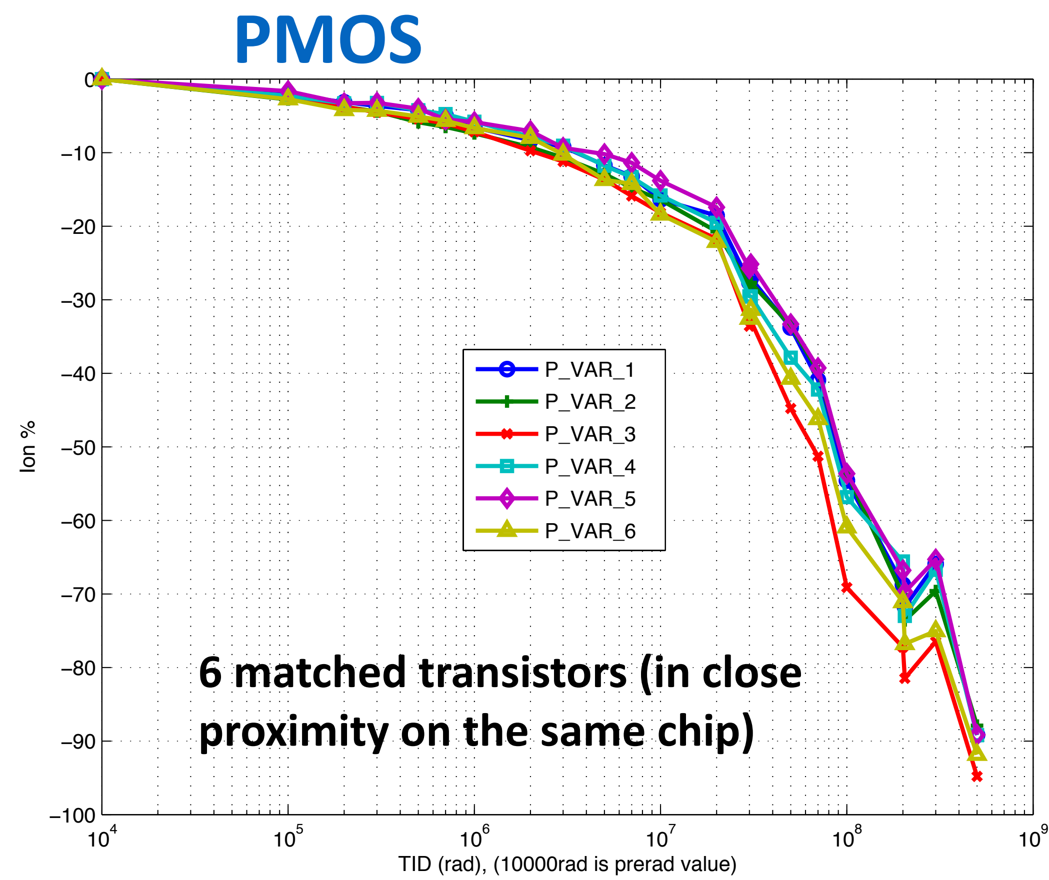


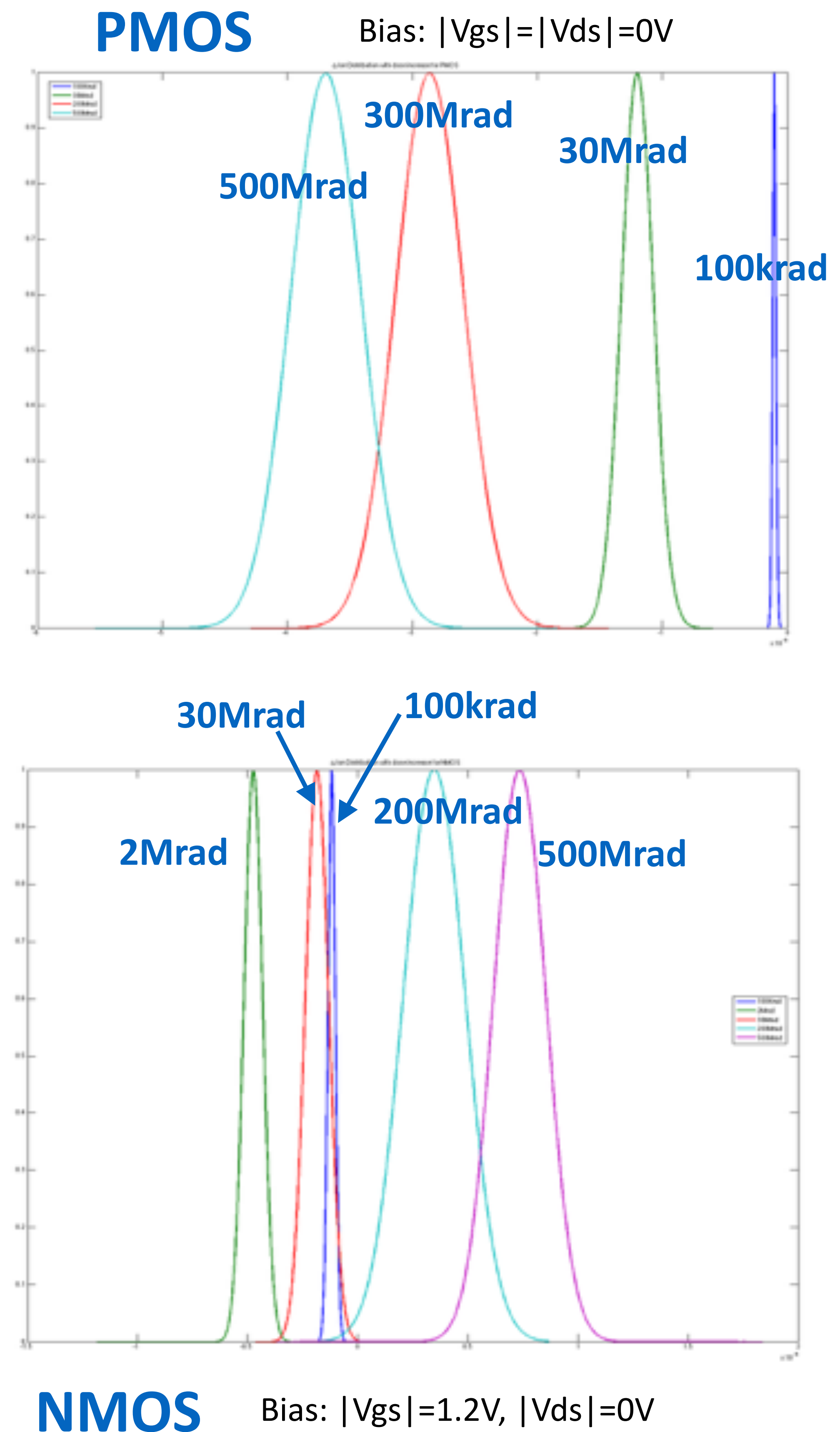
Results from Negative Bias Thermal Instability stresses (combined with TID)

Results from Hot Carrier Injection stresses (combined with TID)

Variability of the TID-induced degradation

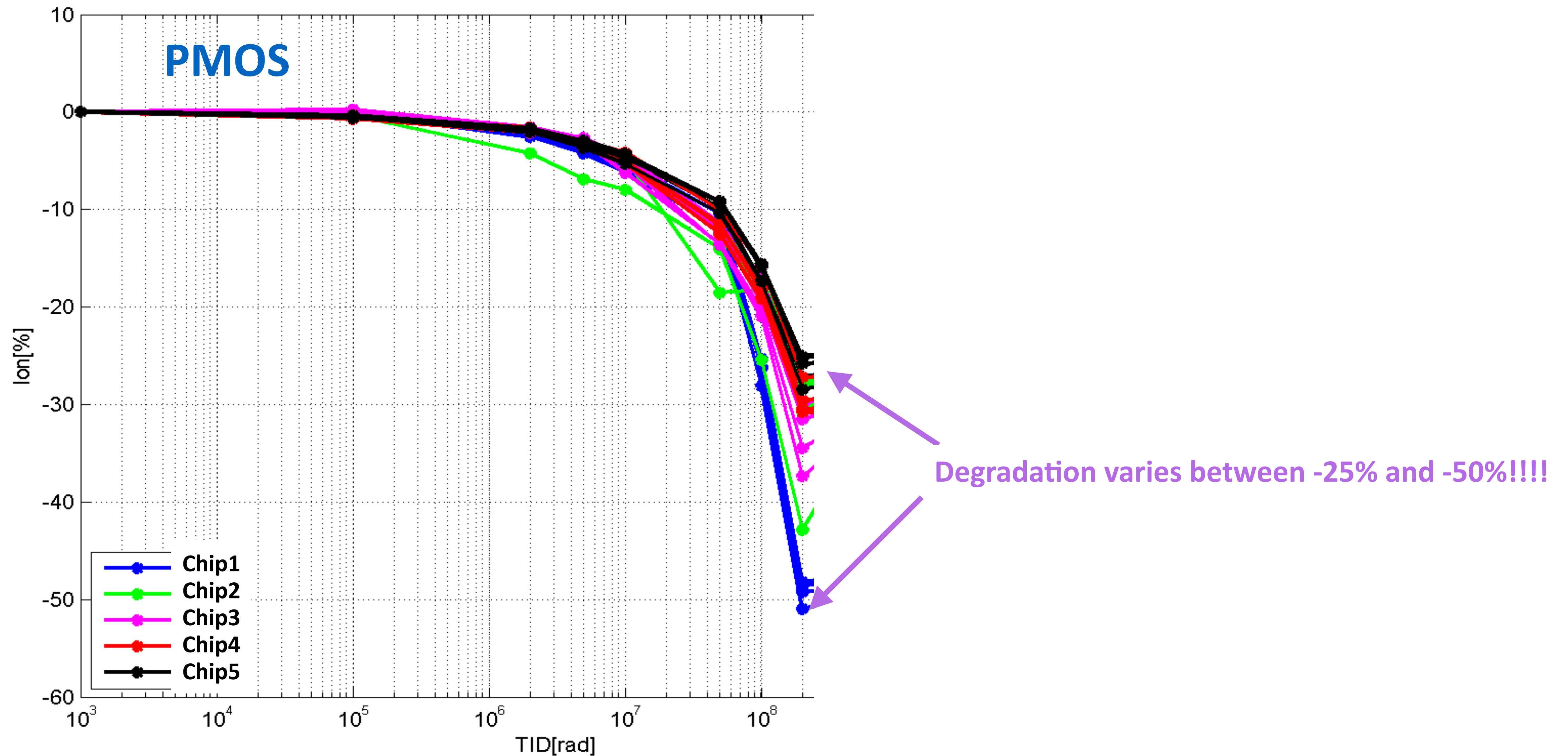
The variability of 'matched' transistors increases with TID





Transistors' size: W=160nm, L=60nm
Irradiation conditions:
T = 25C

The variability between identical transistors irradiated in the same condition on different chips is quite large!



5 identical transistors in each chip
5 chips irradiated in the same conditions
T was varied in annealing. Irradiation was in all cases at 25C
Transistors' size: W=1um, L=60nm
Irradiation conditions:
* T = 25C
* Bias: "Gnd" =>|Vgs|=Vds=0V

Short Wrap-up

NMOS: RISCE dominates, avoiding minimum L transistors guarantees limited damage (for minimum L transistors, damage can also be limited depending on the applied bias)

PMOS: both RISCE and RINCE contribute to a strong degradation. It is very difficult to predict the net radiation effects in the application: bias and temperature influence the results in an interwoven way, and more than one mechanism is involved (different activation energies)

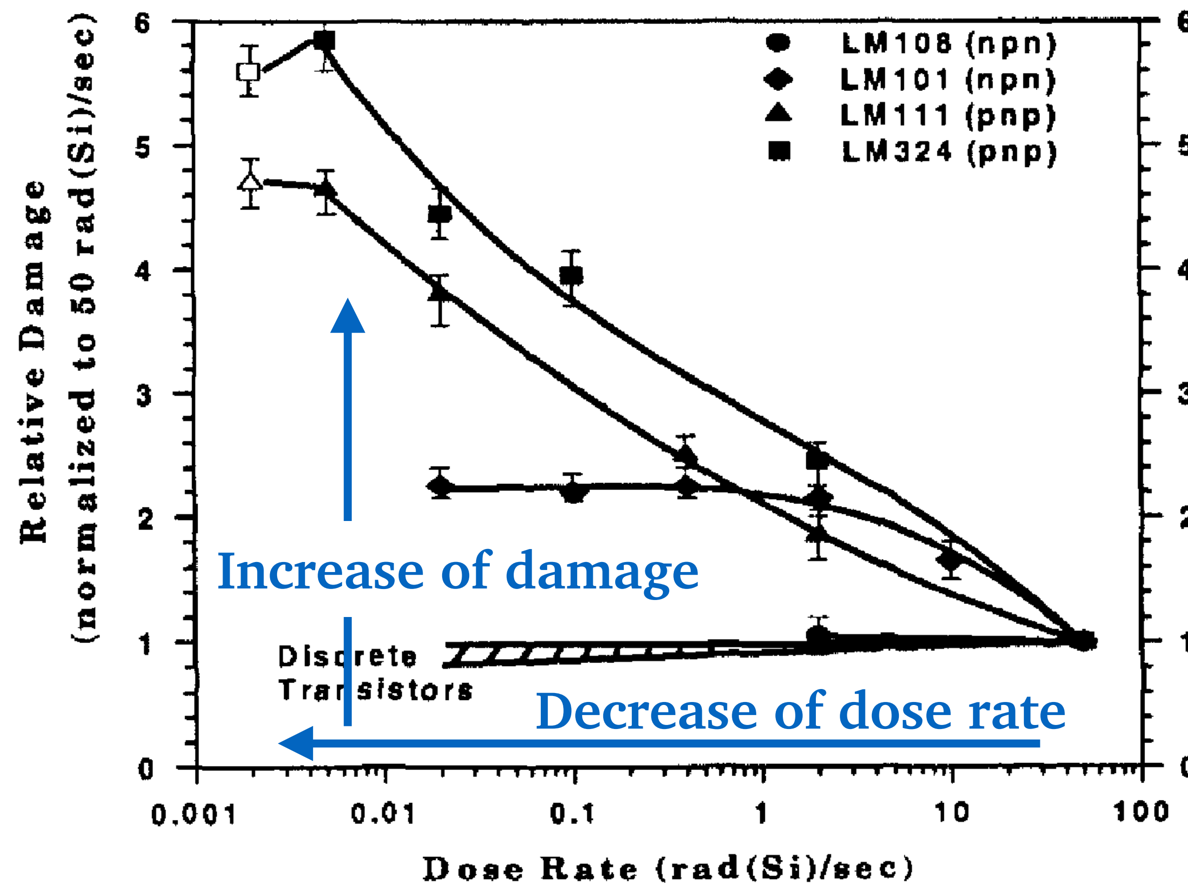
<u>Generalisation of the observed effects</u>

Comparison with 130nm from same manufacturer evidences that the effects are similar in the two nodes (although considerably less relevant in 130nm)

Comparison with another 65nm process at -30C (CPPM, Fermilab) reveals some similarities as well (comparison of the full range of effects would require irradiation and annealing at different T)

Some additional comments based on other published work in the radiation effects field

Enhanced Low Dose Rate Sensitivity (ELDRs): in a large number of bipolar technologies the TID-induced degradation increases at low dose rates



A.H.Johnston et al., IEEE Trans. Nucl. Science. Vol.41, N.6, 1994

Some of the reasons why this happens in bipolars only:

- the phenomena takes place in thick oxides of "poor quality"
- the electric field in the oxide is small

Damage increases with irradiation temperature! Qualification protocols for bipolar technologies foresee irradiation at high T to simulate the increased damage at low dose rates!

Bipolars:

- the phenomena takes place in thick oxides of "poor quality"
- the electric field in the oxide is small
- damage increases with irradiation T
- annealing at 100°C for 3-5 hours after a HDR irradiation enhances the damage making it closer to LDR

65nm RISCE (RINCE to a smaller extent):

- the phenomena takes place in thick oxides of "poor quality" (STI, Spacers)
- the electric field in the oxide could be comparable, along fringing field lines, to the one in bipolar oxides
- damage increases with irradiation T
- annealing at 100°C for 3-5 hours after a HDR irradiation enhances the damage

Could the radiation damage observed in 65nm at a dose rate of 9Mrad/hour be "enhanced" at lower dose rates (ELDRS)??

Enhanced Low Dose Rate Sensitivity (ELDRs) has been observed in CMOS, for the source-drain leakage in NMOS

The work observed this feature on TSMC technologies (0.35, 0.25 and 0.18um)

2602 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 52, NO. 6, DECEMBER 2005

Dose-Rate Sensitivity of Modern nMOSFETs

Steven C. Witczak, *Member, IEEE*, Ronald C. Lacoe, *Member, IEEE*, Jon V. Osborn, *Member, IEEE*, John M. Hutson, *Student Member, IEEE*, and Steven C. Moss, *Senior Member, IEEE*

***Abstract*—Radiation-induced edge-leakage current in minimum geometry n-channel MOSFETs from five submicron technologies is examined as a function of dose rate. Under worst-case bias, degradation of transistors from the TSMC 0.35-, 0.25-, and 0.18-μm processes is more severe following low-dose-rate irradiation than following high-dose-rate irradiation and anneal. The leakage current anneals with an activation energy of $\sim$1.0 eV, which suggests that charge trapping in the field oxide is associated with shallow defects such as E'_δ centers. A comparison of the device response to a first-order kinetics model for hole trapping and annealing indicates that the enhanced degradation results from slower annealing rates following low-dose-rate irradiation. These results suggest that space charge in the field oxide may contribute to the dose rate sensitivity by altering the spatial distribution of trapped holes. In contrast to the response of the TSMC parts, high-dose-rate irradiation and anneal bounds low-dose-rate degradation of transistors from the HP 0.50- and 0.35-μm processes. These results imply that existing qualification approaches based on high-dose-rate irradiation and anneal may not be conservative for the hardness assurance testing of some advanced CMOS devices.**

***Index Terms*—Anneal, dose rate, E'_δ center, edge-leakage current, field oxide, hardness assurance, ionizing radiation, MIL-STD-883F Method 1019.6, metal–oxide–semiconductor field-effect transistor (MOSFET), space charge.**

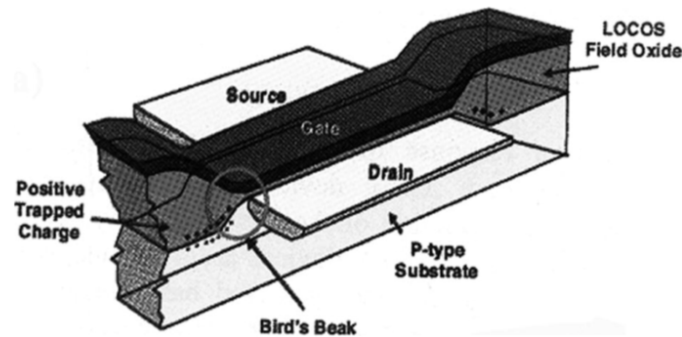
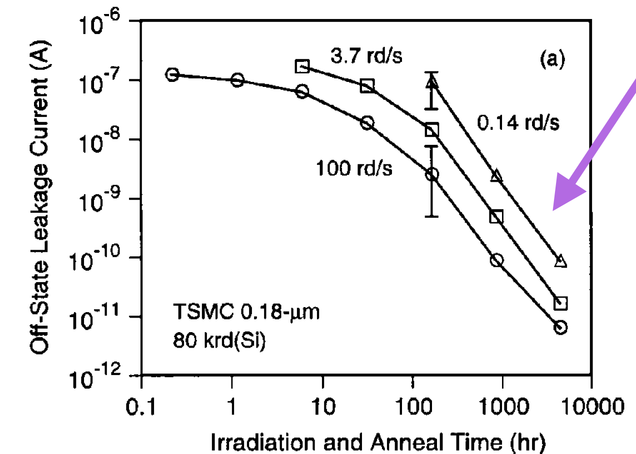
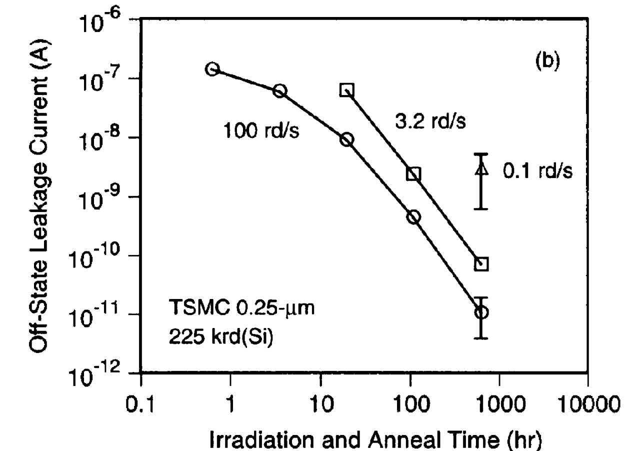


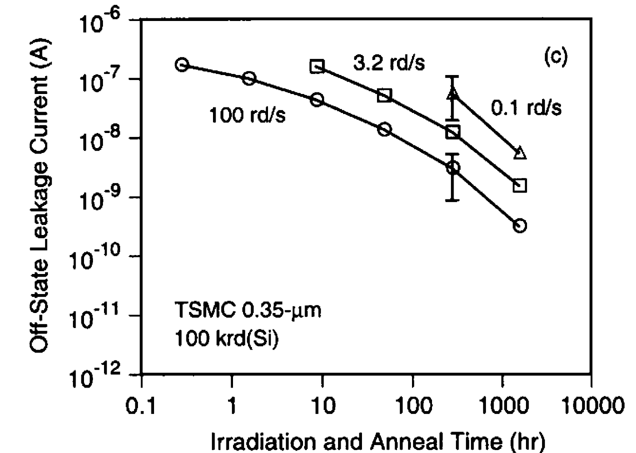
Fig. 1. Cross-section of an n-channel MOSFET isolated by a field oxide. Positive trapped charge in the field oxide can cause off-state leakage current to flow along the channel edges (previously published in [6]).

following ionizing irradiation and anneal. Under worst-case bias conditions, enhanced degradation at low dose rate compared to high-dose-rate irradiation and anneal is observed for transistors from three of the processes. A first-order kinetics model for hole trapping and annealing is used to infer that the enhanced degradation results from slower annealing rates following low-dose-rate irradiation. An activation energy for

Leakage is worse at lower dose rates!







ELDRS and NBTI have been found to possibly have a common origin…

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 52, NO. 6, DECEMBER 2005 2265

Common Origin for Enhanced Low-Dose-Rate Sensitivity and Bias Temperature Instability Under Negative Bias

Leonidas Tsetseris, Ronald D. Schrimpf, *Fellow, IEEE*, Daniel M. Fleetwood, *Fellow, IEEE*, Ronald L. Pease, *Senior Member, IEEE*, and Sokrates T. Pantelides

***Abstract*—Degradation due to irradiation is known to be associated with the presence of hydrogen in the bulk of the gate oxide, in bulk Si, and at the Si/SiO_2 interface. Previous studies have shown that the migration of protons in the oxide for positive applied gate bias and their reactions at the interface can account for the time and dose-rate dependence of the degradation. Recent experiments, however, have shown that interfacial degradation can occur even in the presence of strong negative gate bias that prevents the arrival of protons at the interface from the oxide side. This result suggests that mechanisms in addition to proton drift in SiO_2 can lead to radiation-induced interface-trap formation. Since previous work on modeling the enhanced low-dose-rate sensitivity (ELDRS) of irradiated bipolar devices was based on formation of an electrostatic barrier that hinders proton transport to the interface at high dose rates, this effect also must be examined in more detail. In this work we use results from first-principles calculations to demonstrate that hydrogen can also be released easily in bulk Si, and especially in the near interfacial area. This hydrogen moves readily to the interface under negative bias. Typical hydrogen precursors in Si are identified as H-dopant complexes. ELDRS shares thus a common origin with another critical reliability phenomenon, the negative bias-temperature instability.**

***Index Terms*—Bipolar transistors, enhanced low-dose-rate sensitivity, interface phenomena, interface traps, radiation effects.**

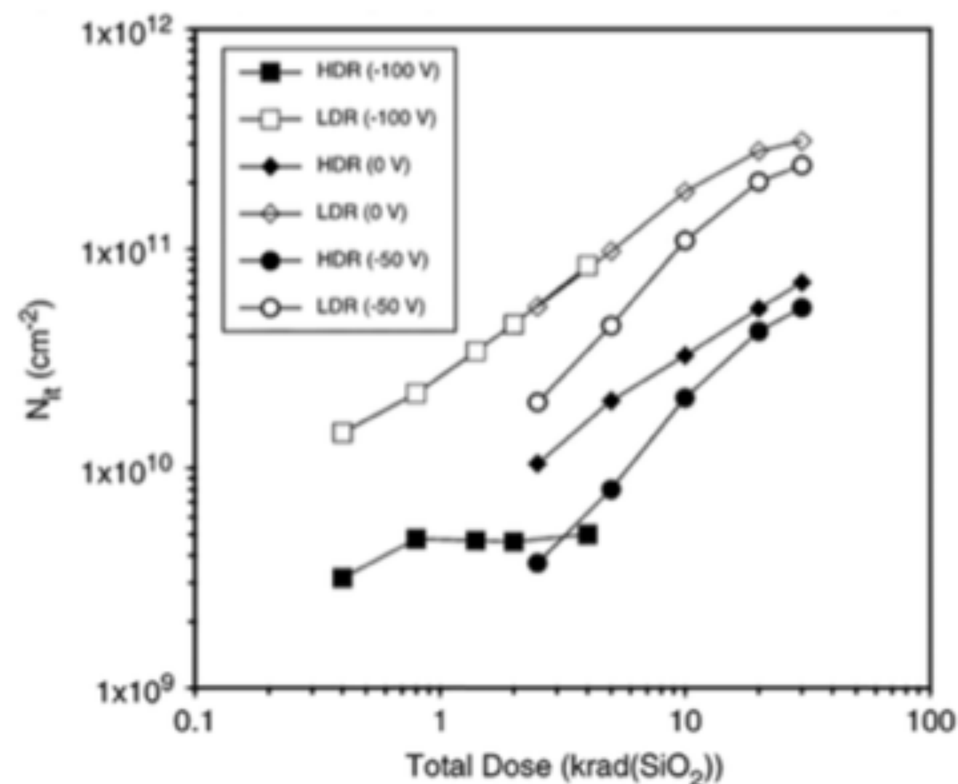
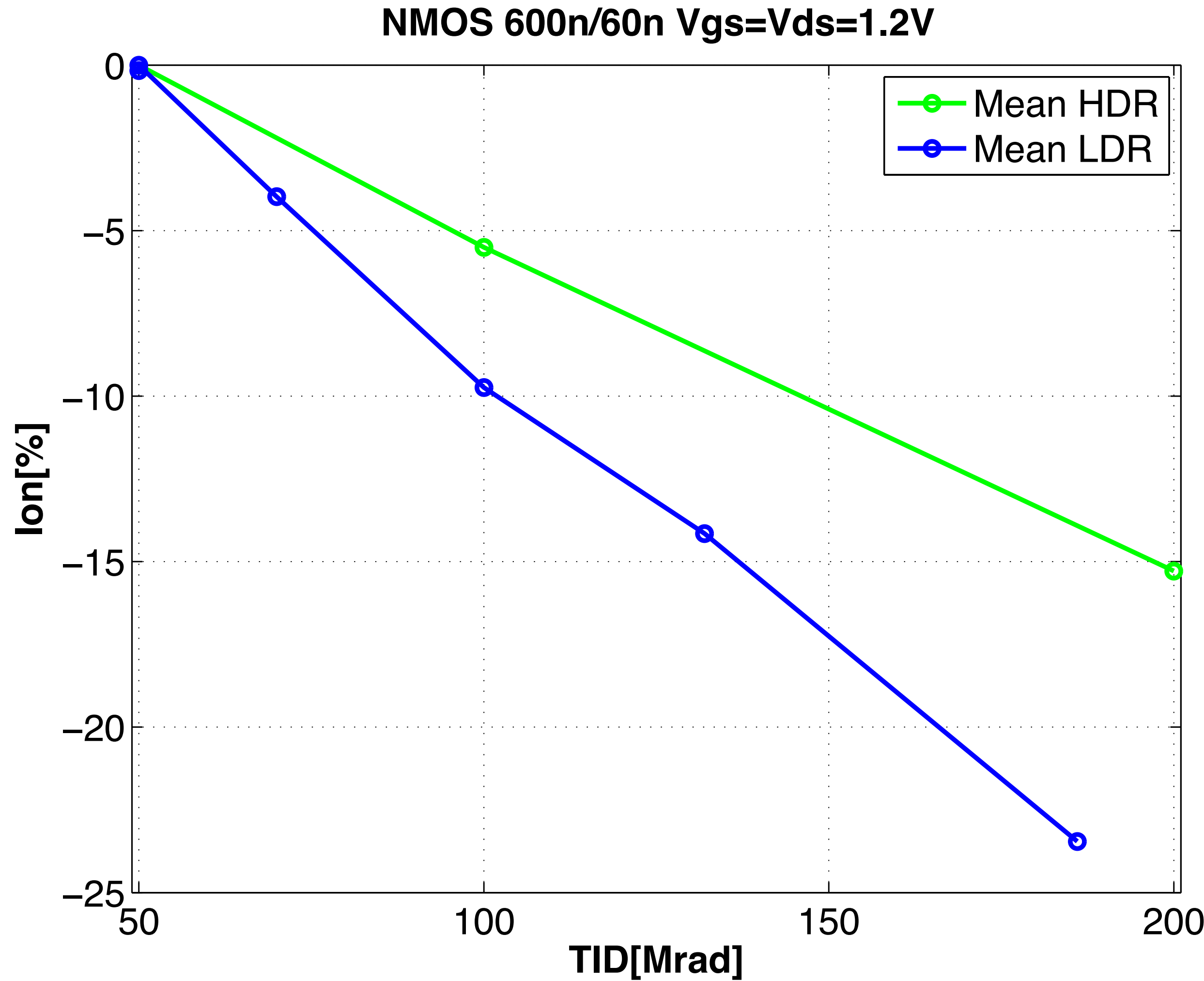
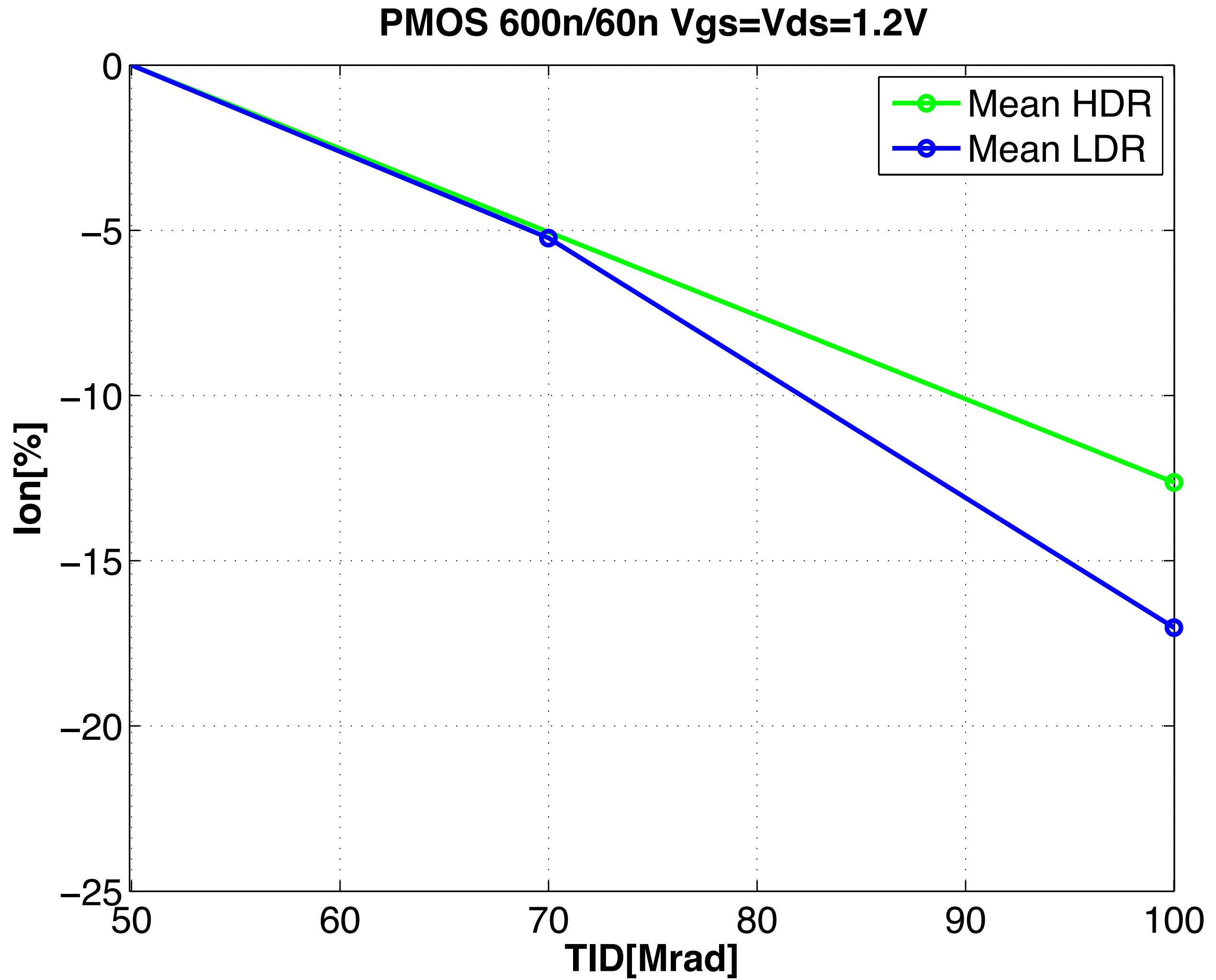


Fig. 1. Density of interface traps (N_{it}) in a gated LPNP transistor after irradiation at high (HDR) and low (LDR) dose rates under gate biases 0, -50, and -100 V (See also [5]).

The only experiment comparing damage at 2 different dose rates is compatible with ELDRS

Given the variability between transistors, this result needs confirmation by more accurate experiments





T = 25°C
HDR = 9Mrad/hour
LDR = 325krad/hour
ratio of the dose rate HDR/LDR=27.7
all samples irradiated at HDR up to 50Mrad, then either at HDR or LDR
measurements averaged over 3 samples (HDR) and 2 samples (LDR)

We do not understand it all - by far!

Difficult to imagine our community investing much more effort in this study to understand the physical mechanism (new test structures, new set of measurements with other techniques, ….)

Enough data is available to extract damage coefficients for models helping ASIC designers (effort under way at CPPM)

We do not know how/if we can predict the real degradation in the application