Readout and Data Acquisition in the NEW Detector based on SRS-ATCA

R. Esteve[a], J. Toledo[a], J. Rodríguez[b], M. Querol[b] and V. Álvarez[b]

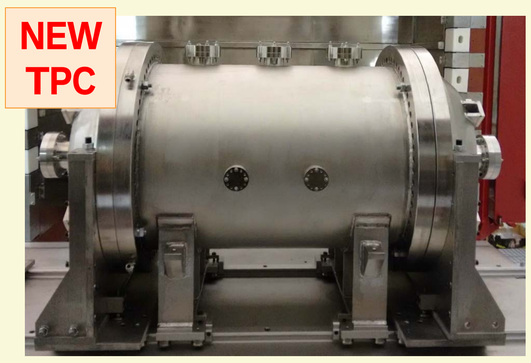
[a] *Instituto I3M, Universitat Politècnica de València, UPV, Valencia, Spain*
[b] *Instituto de Física Corpuscular, CSIC-UV, Valencia, Spain*

INTRODUCTION

The Scalable Readout System (SRS) is an IP co-owned by CERN, Universitat Politècnica de València (UPV) and IFIN-HH Bucharest. It was defined by the CERN RD51 Collaboration [1-2] as a scalable, multi-channel readout platform that could easily adapt to a wide range of front ends.

In 2014, SRS was ported to the ATCA (Advanced Telecommunications Computing Architecture) standard upon agreement with the German company EicSys. The use of certified crates with built-in and redundant cooling, power and shelf management makes it a more robust mechanical and electrical solution for prolonged operation in experiments than the original flavor.

NEXT [3] is an underground experiment aimed at searching for neutrinoless double-beta decay that combines an excellent energy resolution with tracking capabilities merging PMTs and SiPMs. NEXT-DEMO, a small-scale demonstrator, was read out using classical SRS, based on Eurocard mechanics. NEXT has adopted SRS-ATCA for its first stage, called NEW. SRS-ATCA is used for the readout, DAQ and trigger for NEW, being, to our knowledge, the first experiment operating entirely on SRS-ATCA.



ATCA SYSTEM

SRS has two main building blocks: the Front-End Concentrator card (FEC) [4], a flexible front-end interface and data concentrator, and the Scalable Readout Unit (SRU), a second data concentrator stage intended for large scale applications. Both modules are based on FPGA and can interface the DAQ PC farm via GbE links, thus reducing the DAQ and trigger systems to a network-based architecture. Custom links (named DTCC links) [5] allow to carry clock, slow controls, trigger and data over copper (four LVDS pairs over off-the-shelf HDMI or RJ-45 cable) or optical fibre.

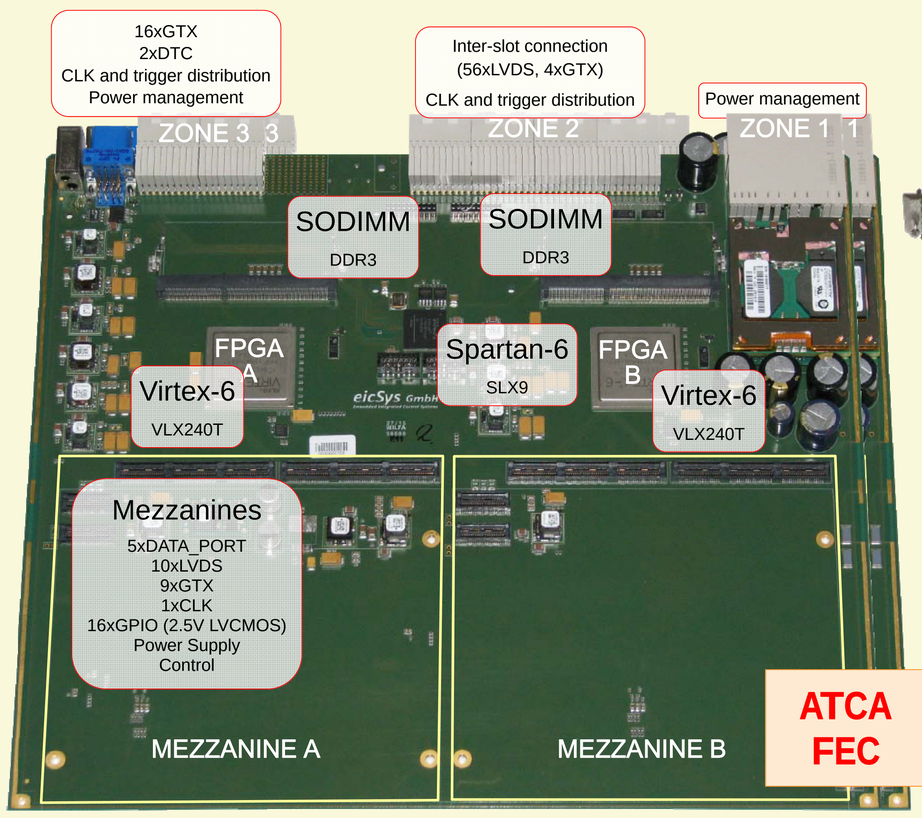
The new ATCA-FEC has two Xilinx Virtex-6 FPGAs and DDR3 memory that allow to implement data processing customized to target applications, interfaced via two on-board mezzanine connectors (up to 12 HDMI ports each). In addition, rear transition modules (RTM) provides GbE, 10 GbE and other I/O connectivity.

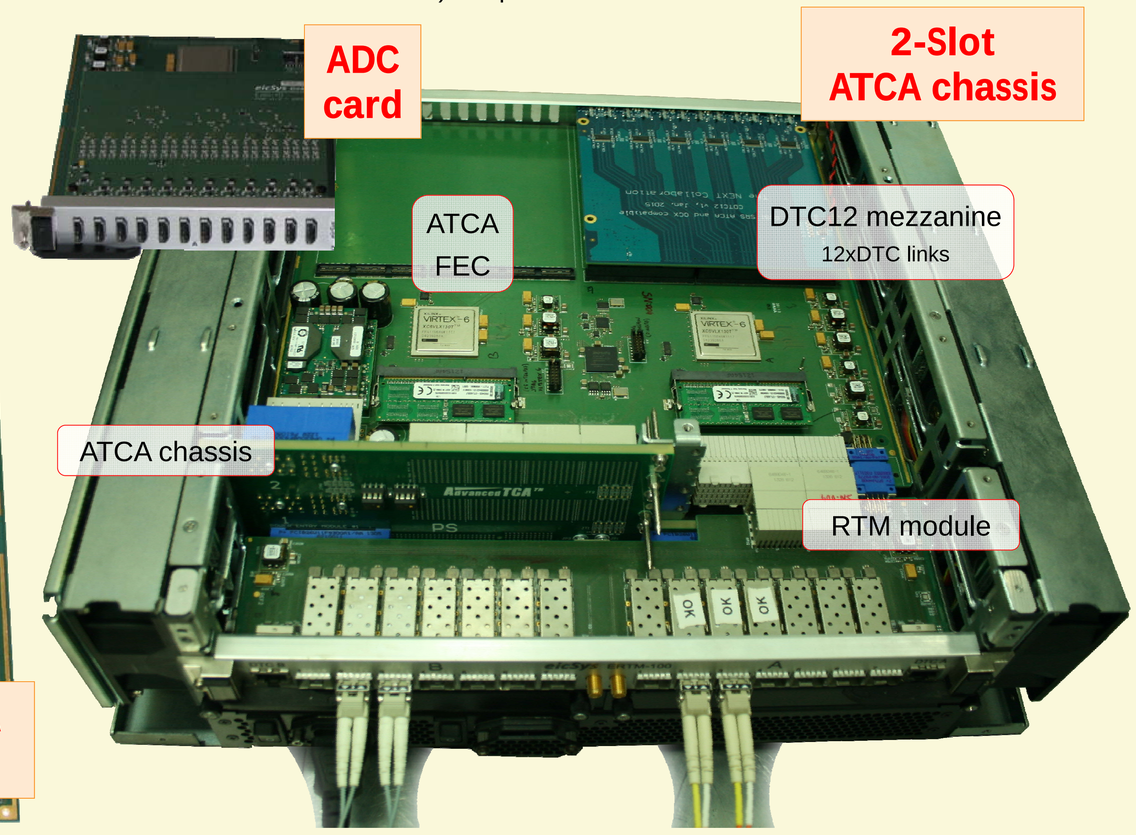
This is functionally equivalent to 2 “classic” FEC modules.

Existing mezzanines are a 24 -ch ADC card and a 12-ch copper DTCC digital link card. Optical interface mezzanines are currently in design phase.

The ATCA backplane provides data connection among FECs and power.

Different chassis sizes up 14 slots are available.

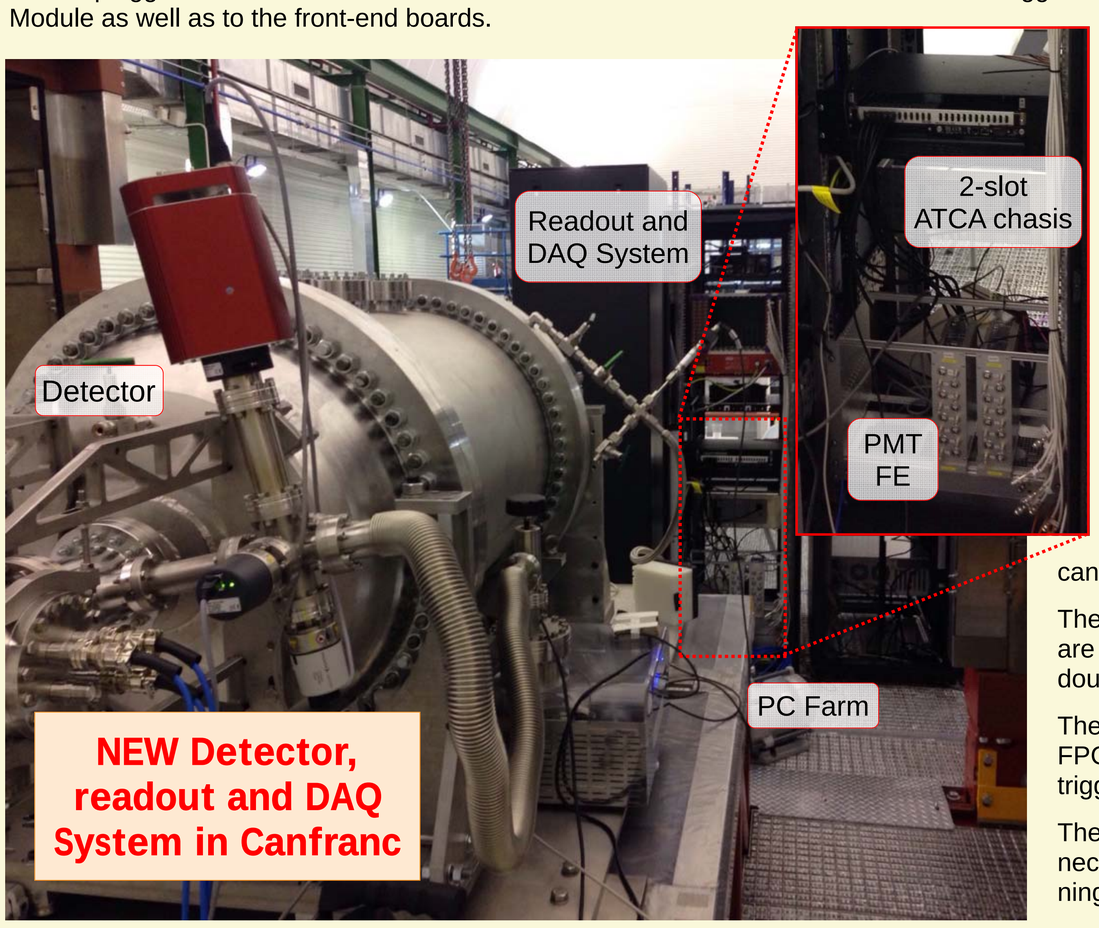


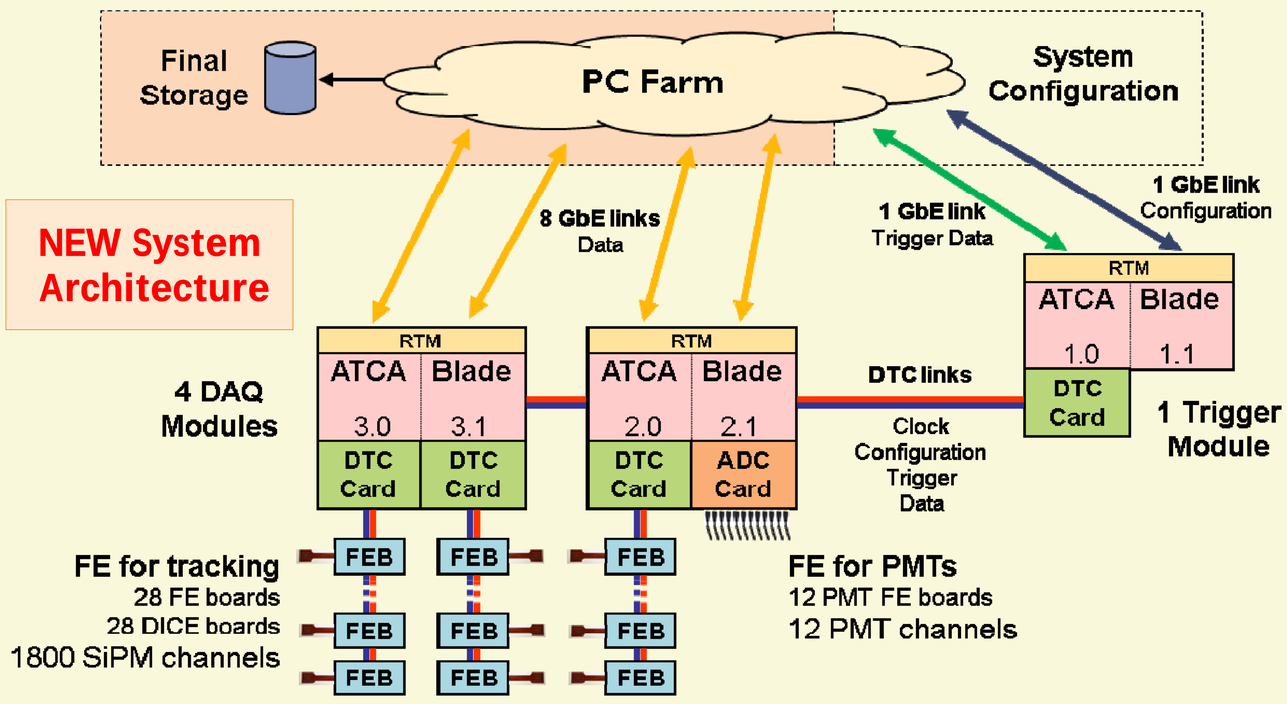


READOUT AND DAQ ARCHITECTURE

For the NEW DAQ system, up to two and a half ATCA-FECs are needed to read out the detector energy and tracking planes. Specific adapter mezzanines have been developed to interface the PMT and SiPM front-end electronics. Each ATCA-FEC interfaces the PC side via 4 GbE links over optical fibre.

Reading out the tracking plane, which consists of close to 1800 sensors laid out with a 1-cm pitch in twenty-eight 64-SiPM boards [6], requires one and a half ATCA-FEC and a total of three digital interface mezzanines. The energy plane (12 PMTs) is read out via an ADC mezzanine plugged onto half ATCA-FEC module. DTC links connect ATCA-FECs to the Trigger Module as well as to the front-end boards.





Front-end electronics work in push mode, it stores continuously incoming data in a circular buffer (up to 3.2 ms) and reads out it when a trigger accept is received. A double buffer architecture allows the reduction of the dead time. Buffers are implemented in the DDR3 memory. The ATCA-FEC in the energy plane also generates trigger candidates, based on the early energy estimation of the events received.

There are 3 DAQ modes: Raw data mode; Normal Mode 1 (event discrimination is used, considered “normal events” are sent zero-suppressed, and “interesting events” in raw mode); Normal Mode 2 (similar to Normal Mode 1, but the double buffer is only used for “interesting events”, reducing only the dead time for this type of events).

The Trigger Module (half ATCA-FEC) receives trigger candidates, implements a re-configurable trigger algorithm on FPGA and sends trigger accept commands to the DAQ Modules [7]. A NIM input in the RTM module allows external triggers if needed.

The described system has been tested and validated in a small setup with a Trigger Module and 2 ATCA-FECs connected to 12 PMTs and 12 SiPM front-end boards. A setup with the DAQ for the energy plane has been recently running in the Canfranc Underground Laboratory in Spain.

REFERENCES

[1] S. Martoiu et al., The SRS scalable readout system for micropattern gas detectors and other applications,NIM A, 2011.
[2] RD51 Collaboration, Development of micro-pattern gas detectors technologies, /http://rd51-public.web.cern.ch/rd51-public/S.
[3] V. Álvarez et al., NEXT-100 Technical Design Report (TDR), JINST 7 (2012) T06001
[4] J.Toledo, et al., The front-end concentrator card for the RD51 scalable readout system, JINST 6 (2011) C11028.
[5] A. Tarazona, et al. A point-to-point link for data, trigger, clock and control over copper or fibre, JINST 9 (2014) T06004.
[6] J. Rodríguez et al., The front-end electronics for the 1.8-kchannel SiPM tracking plane in the NEW detector," JINST 10 (2015) C01025.
[7] R. Esteve, et al, The trigger system in the NEXT-DEMO detector, JINST 7 (2012) C12001.

ACKNOLEDGEMENTS

The authors would like to acknowledge the collaboration of the membership of the NEXT experiment. The European Commision under the European Research Council 2013 Advanced Grant 339787 — NEXT, the Ministerio de Economía y Competitividad of Spain under grants CONSOLIDER-Ingenio 2010 CSD2008-0037 (CUP), FPA2009-13697-C04-04 and FIS2012-37947-C04-04. The Director, Office of Science, Office of Basic Energy Sciences, of the US Department of Energy under contract no. DE-AC02-05CH11231; and the Portuguese FCT and FEDER through the program COMPETE, project PTDC/FIS/103860/2008. The Minsterio de Economía y Competitividad and FEDER FIS2014-53371-C4-4.

next.ific.uv.es