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A time-based front-end ASIC for the Silicon micro-strip sensors of the PANDA Micro Vertex Detector

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Among the many detectors planned for the PANDA experiment that will take place at the future FAIR accelerator facility, the innermost is the Micro Vertex Detector (MVD). This detector foresees both pixel and strip silicon sensors. The readout chip for the strip sensors of the MVD, named PASTA (PAnda STrip Asic), was developed according to a time-based architecture aiming at Time over Threshold measurements through a high resolution Time to Digital Converter (TDC). A basic overview of the functionalities and a description of the main blocks of the PASTA chip will be presented. Supported by BMBF, HIC4FAIR and JCHP.

Summary

The antiProton ANnihilation at Darmstadt experiment (PANDA) is one of the key experiments at the future Facility for Antiproton and Ion Research (FAIR), presently under construction near Darmstadt in Germany. Among the many sub-detectors, the innermost one is the Micro Vertex Detector (MVD) that will be made out of both pixel and strip sensors. The first kind will cover two inner barrels surrounding the interaction point and six forward disks; for the two outer barrels and the outer rim of the last two disks, silicon micro-strip sensors will be used. Since one of the most challenging features of the PANDA experiment is the triggerless data acquisition, it became necessary to design an ASIC with a free running readout suitable to handle the high data rates, up to 20 MHz, of PANDA. The PASTA (PAnda STrip Asic) chip has been thus developed. The chip provides both precise time-stamping and charge information through the Time-over-Threshold (ToT) technique. This choice has several benefits from the design point of view. First, it allows to preserve the linearity of the charge measurement also in presence of large signals that saturate the front-end amplifier. The first stage of amplifier consists of a preamplifier able to interface with both n-type and p-type strips and a second stage where a constant current discharges a feedback capacitance to extract a linear ToT information. To minimize the channel dead-time, the average width of the ToT pulse must be kept below 300 ns, while the desired charge dynamic range is 9 bits. Therefore, to avoid very fast clocks, the leading and trailing edges of the ToT signal are captured with a time-to-digital converter, employing a readout architecture inherited by an ASIC (TOFPET [1]) previously developed by other groups in the context of a medical physics application. The chip runs with a clock that can be changed from 40 MHz to 160 MHz. Analog techniques are used to interpolate the clock signal, providing a time resolution that can be adjusted between 50-500 ps. Each channel features a dual threshold discriminator to improve the time-walk performance. A 64 channel prototype has been submitted in a 110 nm CMOS process, with a modularity already optimized in view of the final application. The circuit dissipates below 4 mW per channel and occupies a silicon area of 3.4 mm x 4.5 mm.
A key feature introduced in the digital part of PASTA is related to the radiation hardness. Single Event Upset (SEU) protection systems were implemented utilizing triple-mode redundancy and Hamming encoding.
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[1] F. Gonçalves, A. Rivetti, G. Mazza, J. C. Silva, R. Silva, J. Varela, M. D. Rolo, R. Bugalho. A 64-channel asic for tofpet applications. 2012.

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