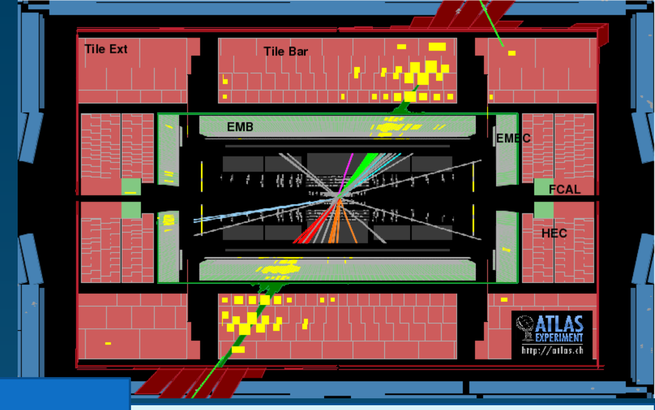
The new Front End Electronics for the ATLAS Tile Calorimeter Phase 2 Upgrade

Agostinho Gomes (LIP and FCUL, Lisbon, Portugal) on behalf of the ATLAS Tile Calorimeter System



Requirements and motivation

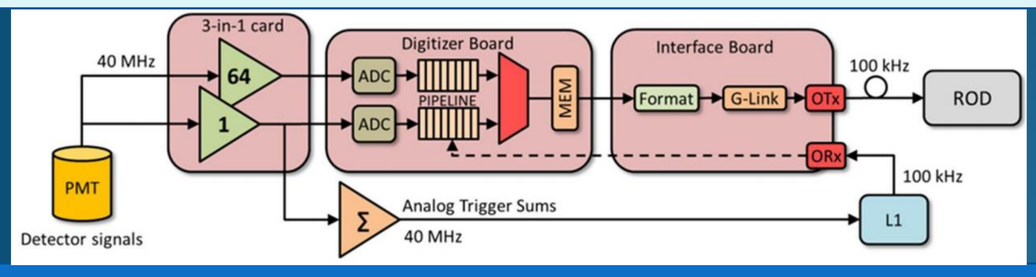
- LHC upgrade in 2023 aims to a factor (5-10) luminosity increase
- Increased luminosity demands for a better precision and finer granularity in the trigger. The effect of pile-up (consecutive interactions in the same cell, pulses piling up) is one major concern with the increased luminosity
- Better radiation tolerance for increased luminosity
- Better performance in signal dynamic range and resolution
- Ageing of components(>10 years already)
- Improve the reliability and reduce maintenance needs

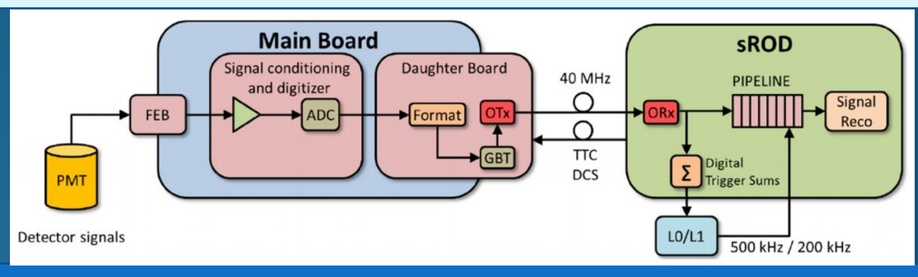
Tile Calorimeter

- ATLAS central hadronic calorimeter made of steel and plastic scintillator tiles
- The scintillators are readout on both sides by two PMTs using WLS fibres
- Divided in 4 partitions, each one composed of 64 modules
- PMTs and Front End electronics mounted in 3m long drawers at the outer radius of the modules
- Measures hadrons and jet energy and direction

Read-out Architecture Upgrade

	Present System		Upgrade System	
Level I trigger signals:	Analog tower sums over 90m cables	→	Fully digitized signal	⇒ Better decisions
Pipeline memory:	On detector	→	Off detector	⇒ Better performance + Radiation hardness
Read-out modularity:	1 + 1 links, 48 PMTs	→	4+4 links, 12 PMTs in a minidrawer	⇒ Better reliability
LVPS modularity:	1 unit for 48 PMTs	→	8 units, 12 PMTs	⇒ Better reliability
HV modularity:	2 units, 24 PMTs	→	4+4 units, 12 PMTs	⇒ Better reliability





Tile Calorimeter Electronics Upgrade Design

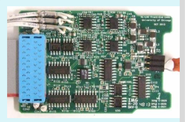
Front End Cards

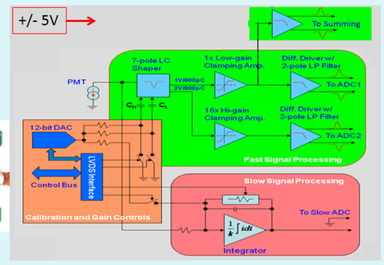
Process PMT signals
Slow integration for Cesium calibration
Charge injection calibration

Three Front End Strategies:

3-in-1

Improves current design
- 17-bit dynamic range, 12-bit resolution
- Passive pulse shaping
- Bi-gain amplification (1x, 32x)
- Charge Injection (CIS) and Cesium calibrations



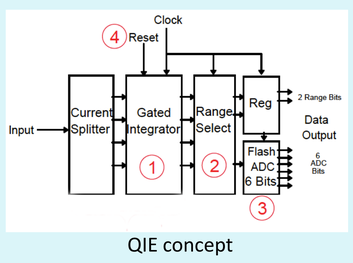


3-in-1 concept

QIE

Charge integration in an ASIC chip
- No pulse shaping
- Signal digitization

See G. Drake poster "QIE12: A new High Performance ASIC for the ATLAS TileCal Upgrade"

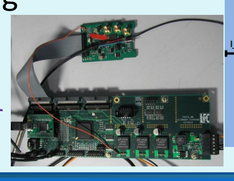


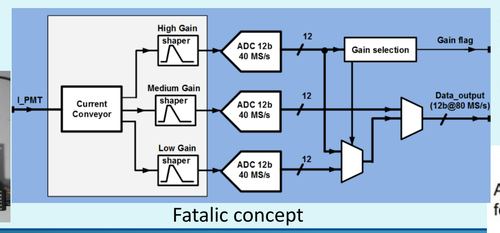
QIE concept

Fatalic

Current conveyer in an ASIC chip
- Tri-gain (1x, 8x, 64x)
- Active pulse shaping
- Signal digitization

See L. Royer talk "FATALIC: A Dedicated Front End ASIC for the ATLAS TileCal Upgrade"

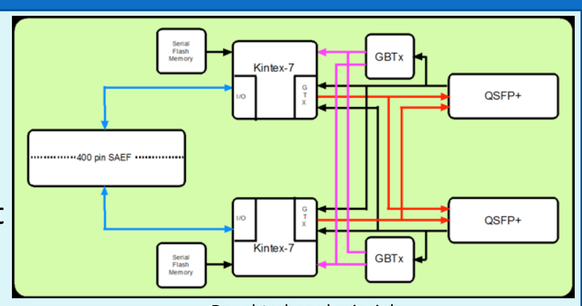




Fatalic concept

Daughterboard

- Data concentration and DCS control of minidrawer
- 2x redundancy data transmission to sROD
- On detector electronics timing management via GBTx
- 8 links, each runs up to 10.24 Gb/s



Daughterboard principle

See C. Bohm talk "A radiation tolerant Data link board for the ATLAS TileCal upgrade "

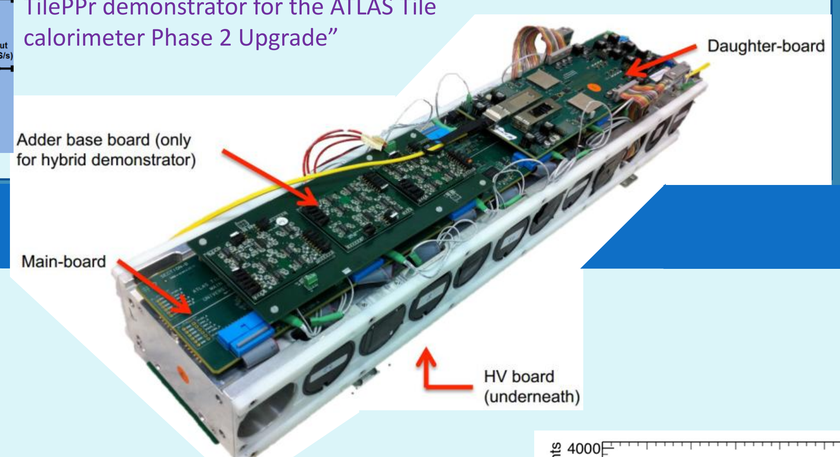
Mainboard

Interface 12 Front End cards and 1 Daughterboard
- 24-channel 12-bit 40Mb/s ADCs
- Control of CIS and Cesium calibrations
- Monitoring ADC timing to comply with the geometric location delays of PMTs

Tile PreProcessor (sROD)

Back to Front-End communication
- 32 minidrawers per board
- Interfaces DCS and TTC through ATCA
- 40 MHz digitized signal to L0 trigger

See F. Carrió poster "Performance of the TilePPr demonstrator for the ATLAS Tile calorimeter Phase 2 Upgrade"



Low Voltage Power Supply (LVPS) redesigned

- Uses reliable components
- +10V in 8 identical bricks to supply 4 minidrawers
- More modular and redundant
- Point of Load Regulators

High Voltage regulation

Two HV strategies for individual PMT control:

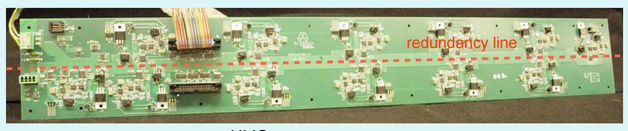
Remote HV

- Regulation off-detector
- External individual HV for each PMT

See F. Vazeille poster "Performance of the remote HV power supply for the Phase 2 Upgrade of the ATLAS Tile calorimeter"

Local HV

- Regulation in-detector in rad hard HVOpto board
- Improved radiation hardness and new monitoring system



HVOpto prototype

Active dividers used to assure good PMT linearity in cells with large minimum bias currents

Demonstrator prototype status

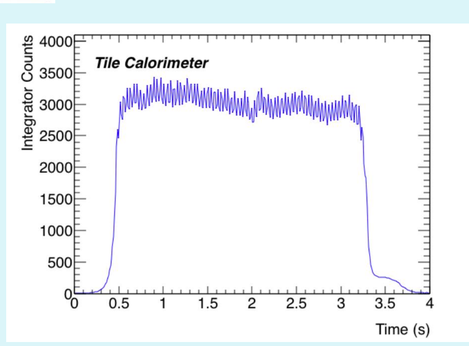
Demonstrator is a hybrid prototype to be integrated into ATLAS for evaluation of the new architecture
- Full compatibility with current system, provides analog and digital trigger
- sROD prototype receives TTC/CANbus commands and sends data to the current ROD

Radiation hardness
- Most of the components in use in the prototypes are already ok for Phase 2 luminosities

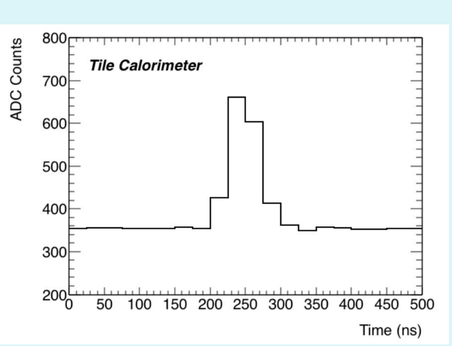
Phase 2 interface
- Increased control of configuration, calibration and readout
- New mobile testbench (Prometeo) under development

Infrastructure, DCS and calibration
- SuperDrawer is operational and interfaced with DCS
- Legacy control of HV + LVPS and monitoring of voltages, currents and temperatures
- Calibration systems (charge injection, Laser/LED pulses, pedestal, Cesium source) used to study performance

Test beam in preparation at CERN to test demonstrator in October 2015



Phase 2 demonstrator integrator response to a moving Cesium source for a D6 cell showing the peaks corresponding to the positions of the 75 tiles of the cell.



Phase 2 demonstrator low gain response to a Laser pulse in the hundreds of GeV sampled at 40 MHz

Summary and conclusions

The Tile Calorimeter Phase 2 Upgrade design is well advanced and a demonstrator module has been produced. Revision of many components is ongoing to improve performance. Control and calibration tests are implemented in the demonstrator that is interfaced with the legacy communication systems. A test beam will take place in October 2015 and in December 2015 or 2016 the demonstrator will be inserted in ATLAS.