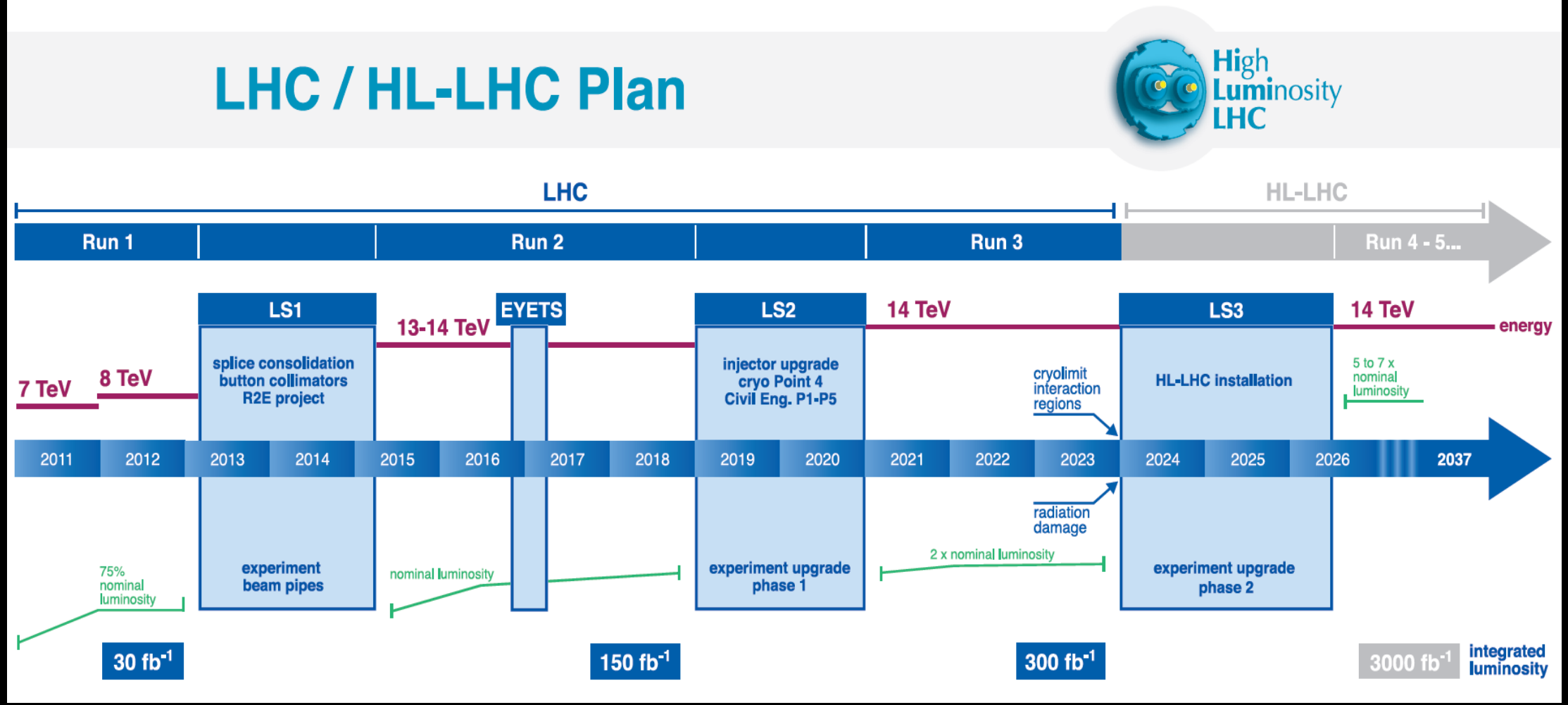
Development of ATLAS Liquid Argon Calorimeter Read-out Electronics for the HL-LHC

Mitch Newcomer

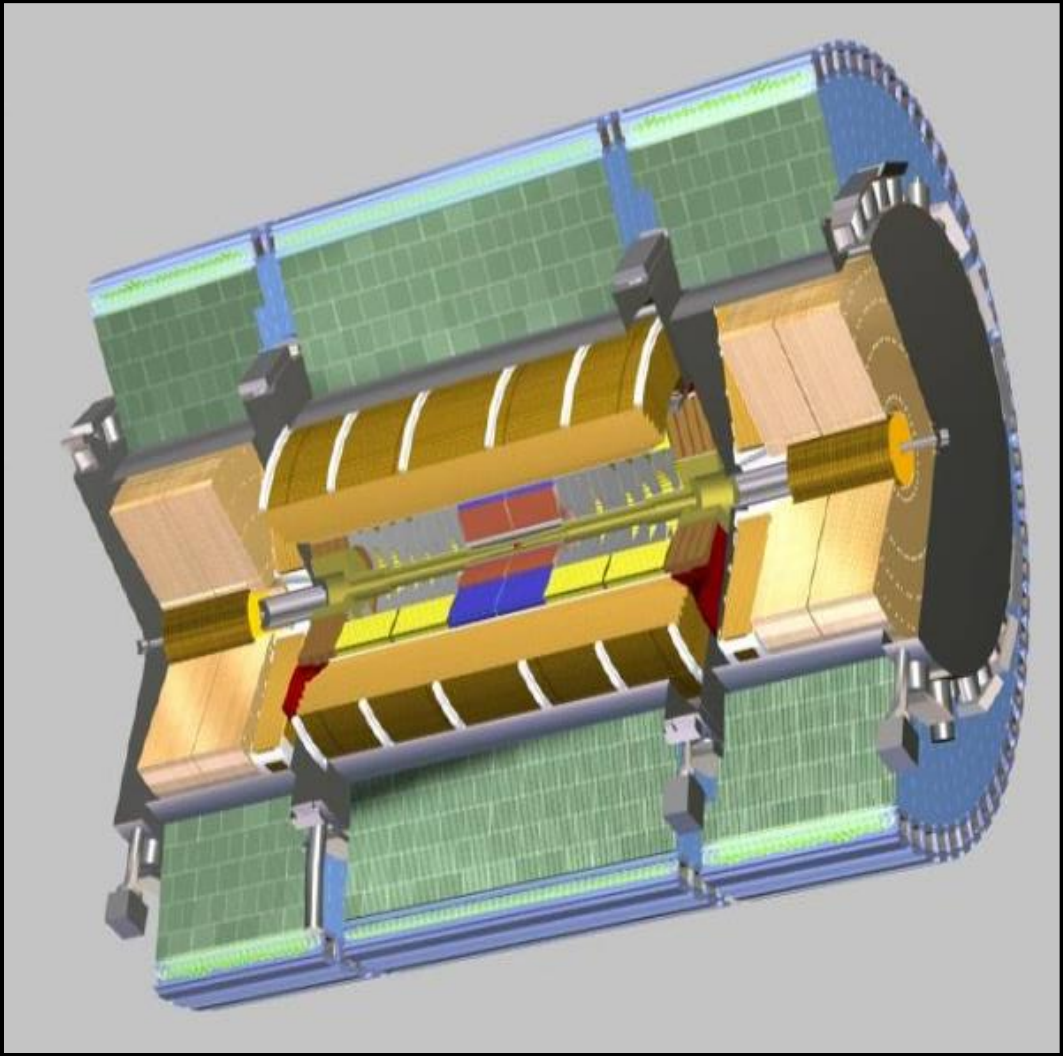
For the ATLAS LAr collaboration

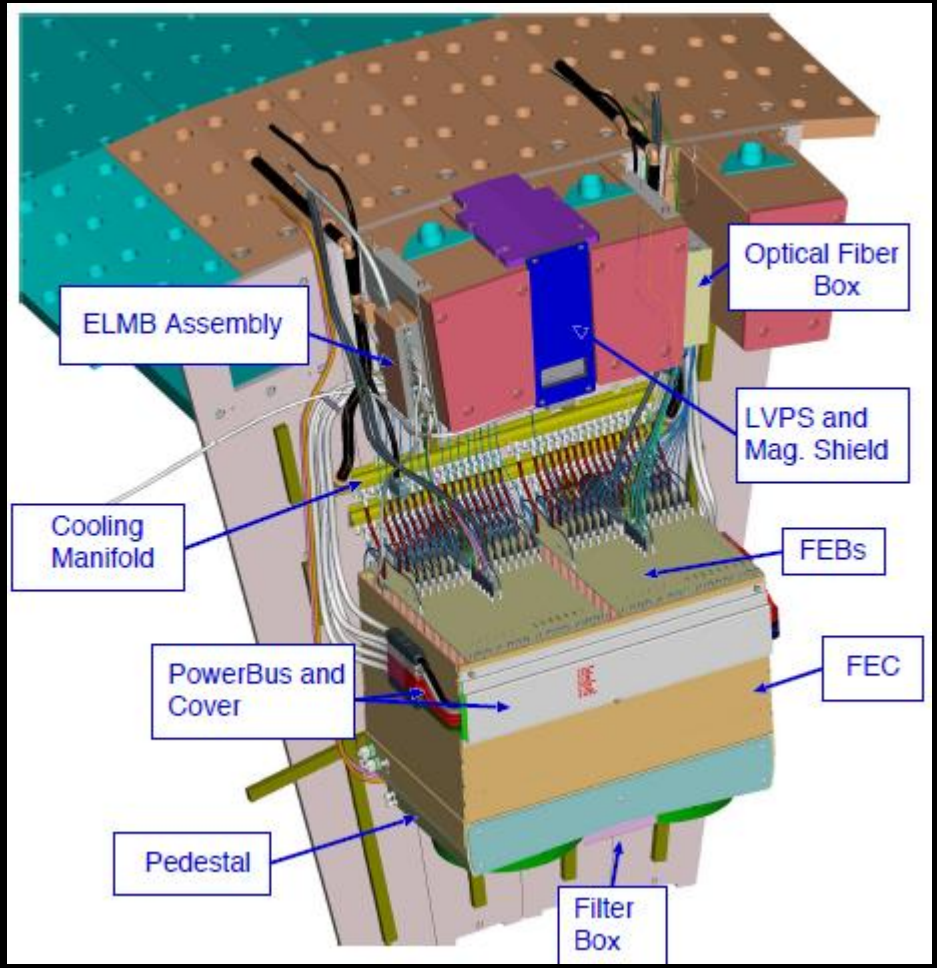
September 2015

LHC / HL-LHC Plan



ATLAS Detector Locations LAr locations

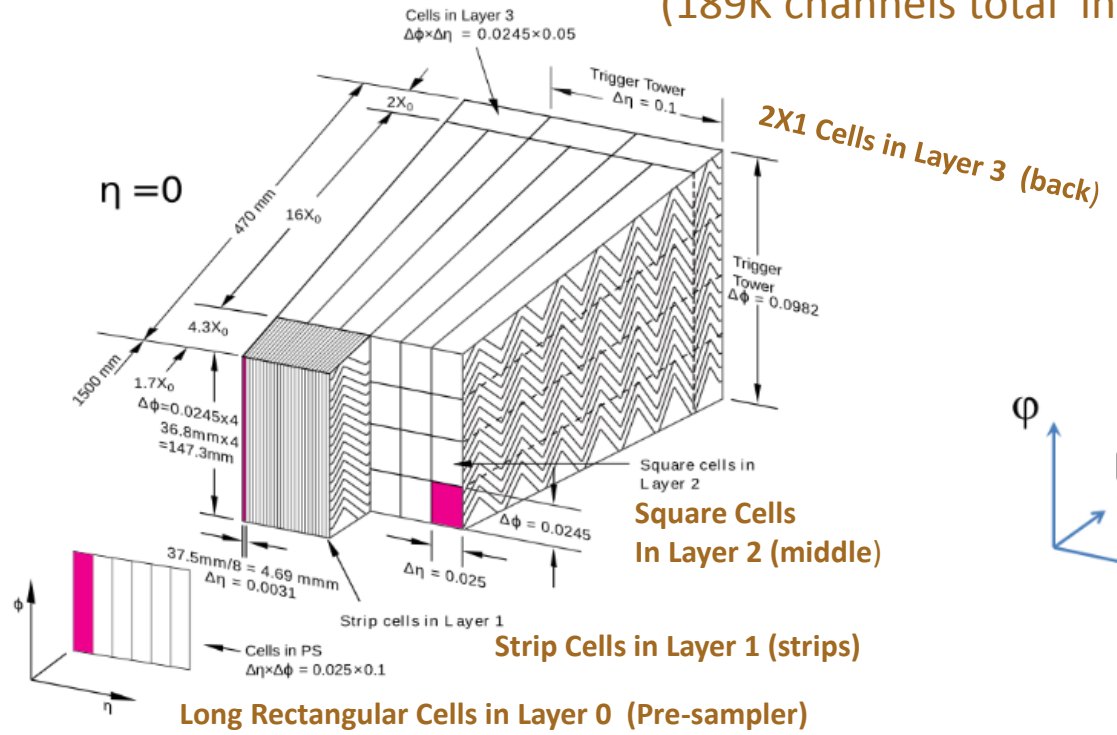




Tower Geometry of the LAr EM Barrel

110K Channels EM Barrel

(189K channels total in the ATLAS LAr)



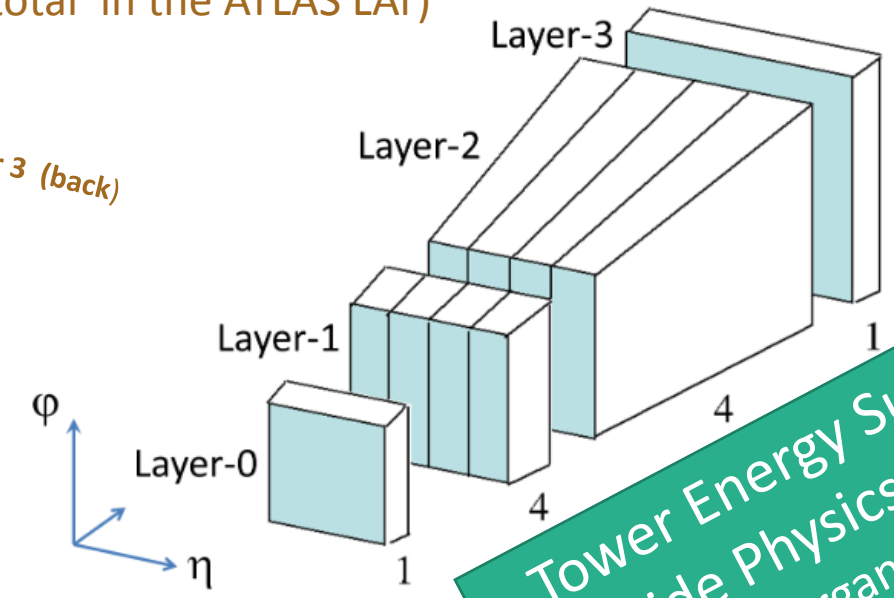
2X1 Cells in Layer 3 (back)

Square Cells
In Layer 2 (middle)

Strip Cells in Layer 1 (strips)

Long Rectangular Cells in Layer 0 (Pre-sampler)

Figure 1. The segmentation of the readout cells in the LAr EM Barrel calorimeter.



Tower Energy Sums
Provide Physics Input
Phase 1 Organization

Figure 2. The segmentation of the Super-Cells of the EM calorimeter.

ATLAS LAr Warm Electronics

Diverse Readout Requirements

	Description
tdr	Drift time
I0/E	Layer Energy Conversion Factor
Imax	Max current in a Layer “Cell”

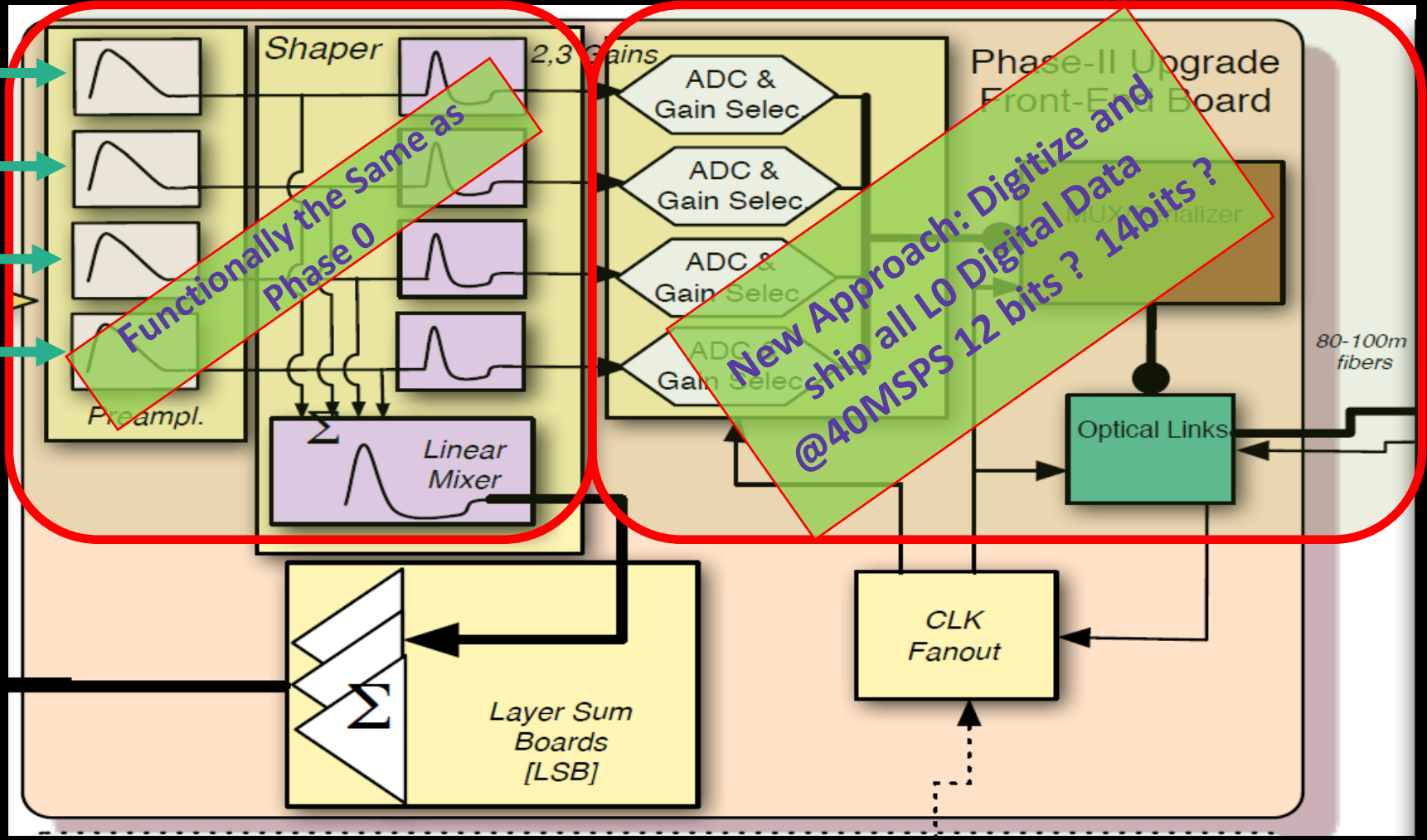
Calorimeter	Layer	tdr (ns)	I0/E (mA/GeV)	Imax (mA)	Cd (pF)
	Presampler	420	0.9-0.7	0.1	160 - 220
Barrel centre	Strips	450	2.7	0.2 - 0.3	250
0<|h|<0.8	Middle	450	2.7	4.5 - 6	1300
	Back	450	2.7	1.5 - 3	300 - 1000
	Presampler	420	0.85	0.1	220 - 400
Barrel edge	Strips	450	3.1	0.3 - 0.4	220
0.8<|h|<1.5	Middle	450	3.1	6 - 9	1600
	Back	450	3.1	3 - 4.5	650 - 2000
End-cap	Presampler				
Outer wheel	Strips	600 - 250	2.4	0.3	250
1.4<|h|<2.5	Middle	600 - 250	2.4	7.5	1000 - 400
	Back	600 - 250	2.4	5	2000 - 500
End-cap	Middle	600 - 400	1.9	8	2000 - 1000
Inner wheel	Back	600 - 400	1.9	4	500 - 600
2.5<|h|<3.2					

Phase II LAr (warm) Front End electronics

LAr Detector
@ 87K (Cold)

4 segments of one layer of:
Presampler
Strips
Middle
or
Back

Front End Board Readout Organized by layer



Local Tower Sums to Trigger Electronics: Liquid Argon Trigger Digitizer Boad (LTDB)

Local Tower Sums to Trigger Electronics

LAr Phase II upgrade Front End Electronics

Objectives

1. Maintain energy resolution and electronics *noise* contributions at the current level of <100nA (Cdet = 1nF) Equivalent input noise*
2. Maintain 16 to 17 bit total dynamic range.
   - If possible increase the range of the gain scales to go from 3 scales to 2. With acceptable linearity. (0.1% in the current LHC detector)
3. Digitize all 128 channels per FEB at 40MHz or higher.
4. Ship L0 data from all channels off detector.
5. Selectable Input impedance 25 or 50 ohms (+/-1.5%)
6. Keep the power to Phase 0 levels (150mW/ch) or lower.

*should not compromise low rate resolution. May be many months or intentional Low Rate operation.

Primary Front End Design Parameters

Detector Simulations

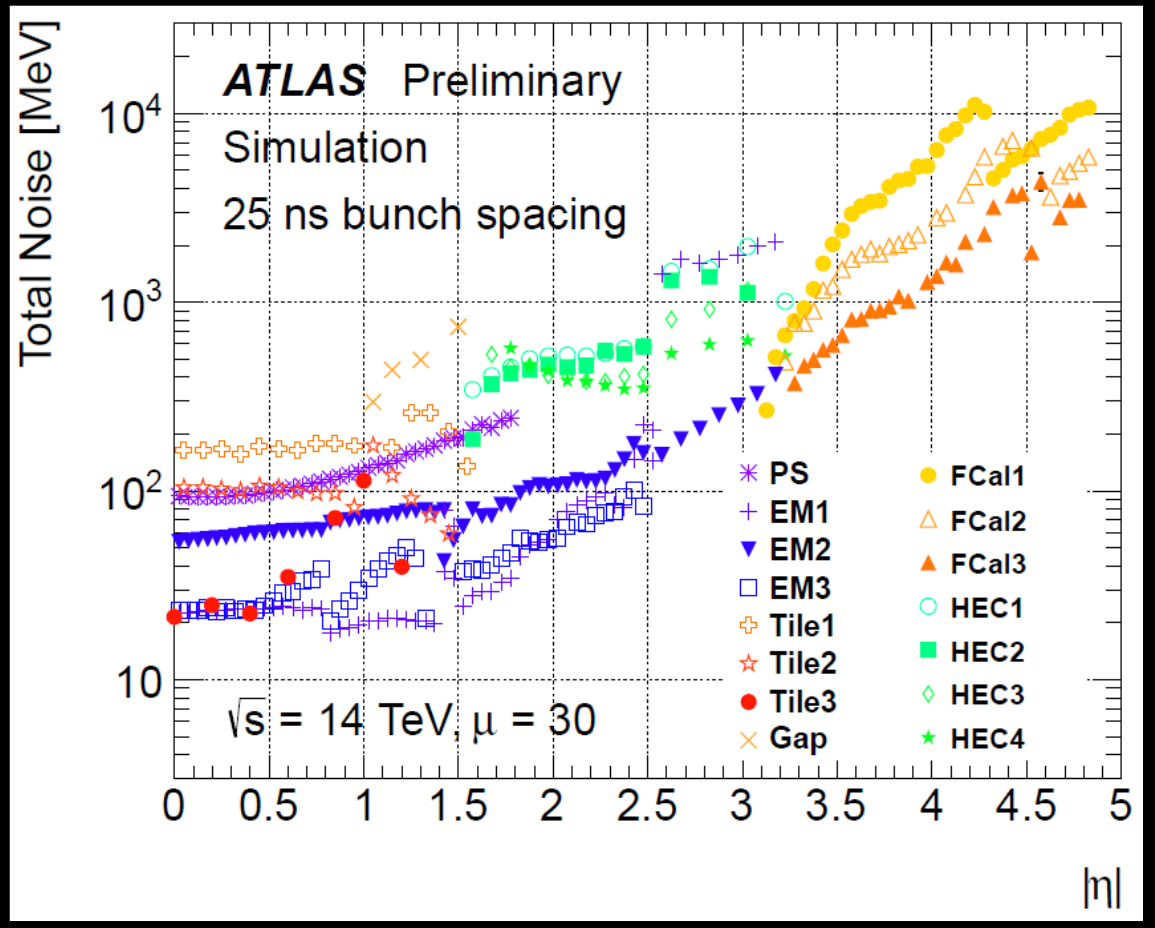
- Background Noise
- Number of Gains → Energy Cluster δE dominated by lowest gain in sum.
- Linearity of Gain Scale – .1% INL end to end or .1% with a soft saturation.
- Utilization of Gain Scale - quantization of noise.
- Digitization rate 40 Mbps

Technology / Complexity / Manufacturability / Implementation

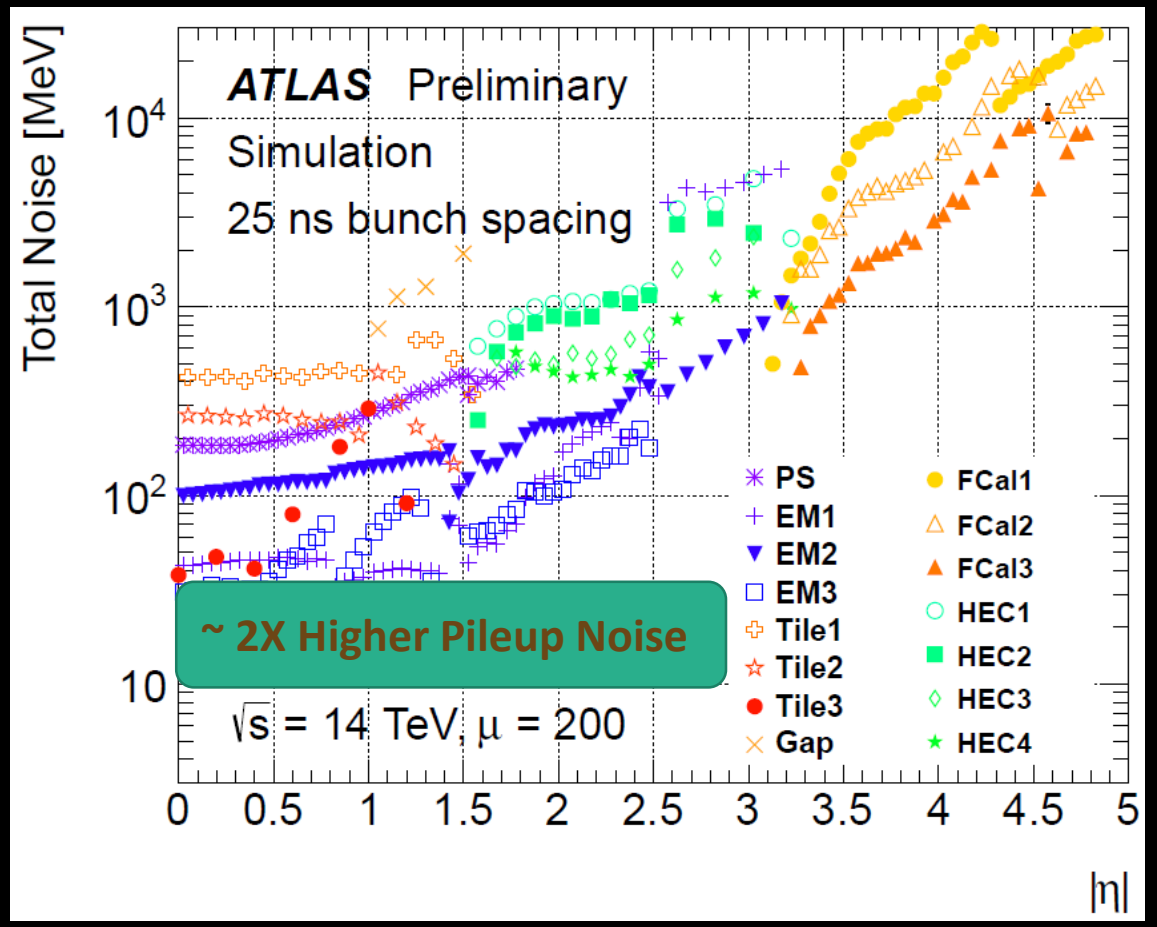
- Power Allocation - Max ~ 125W / 128 channel board ~ 1W/channel
- Number of active and support components
- System Noise

Simulated Noise in the EM and Tile Calorimeter

25ns Bunch Crossings, 500ns live time for LAr signals



$L = 1.1X10^{34}$



$L = 7.25X10^{34}$

Specification Issues under consideration for Phase II upgrade

Number of gains / gain ratio I

Can we move to a 2 gains option ?

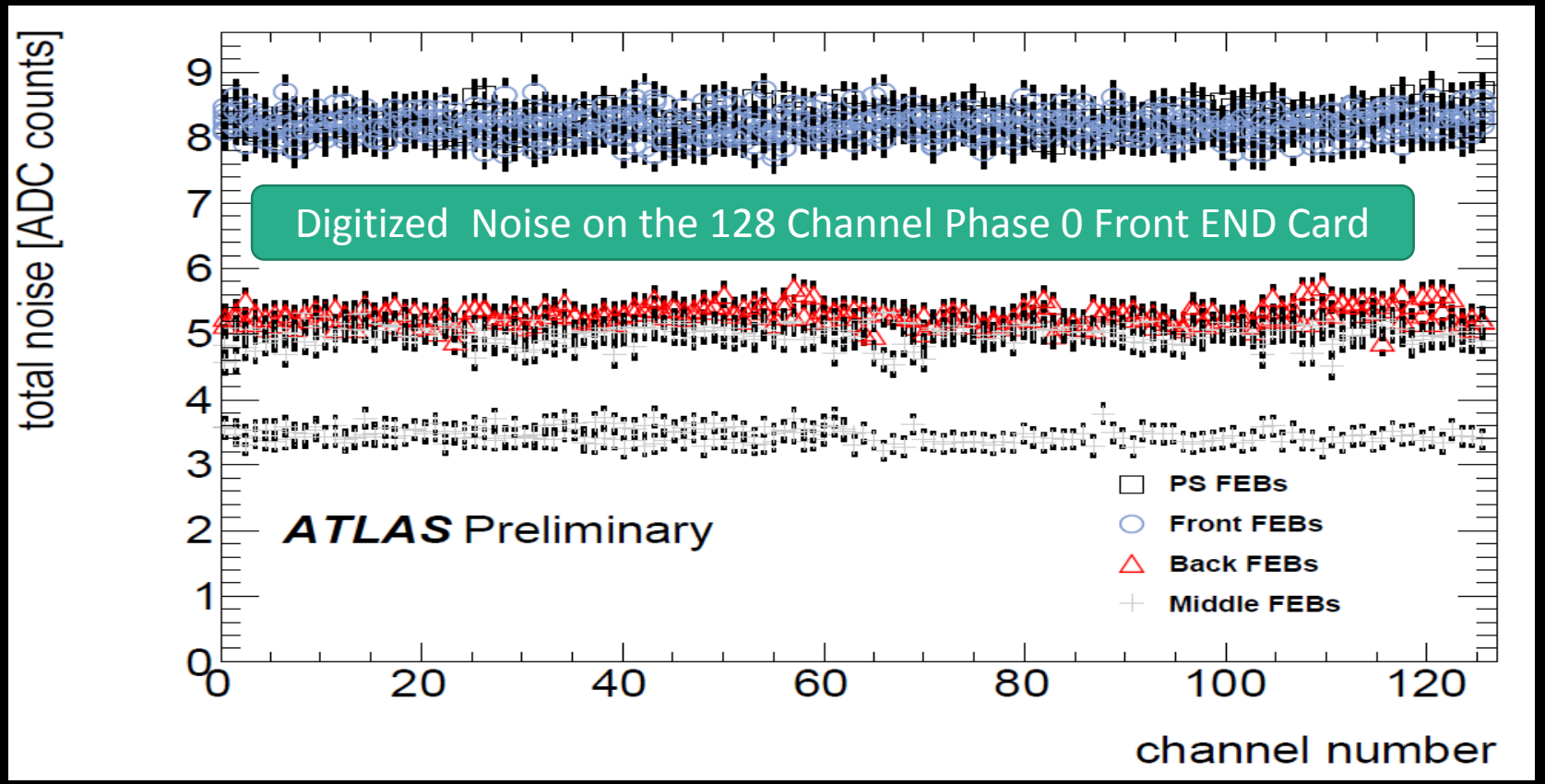
- LSB could be twice larger (current noise is 4 ADC counts)
- Can we do it with 12-bit ADC ? 14-bit (12-bit effective) ?
- Can we have all precision physics (inc. $H \rightarrow \gamma\gamma$) in the high gain ?
- Is PS noise ok, if HV is reduced ?

⇒ Studies ongoing on $H\gamma\gamma$ MC

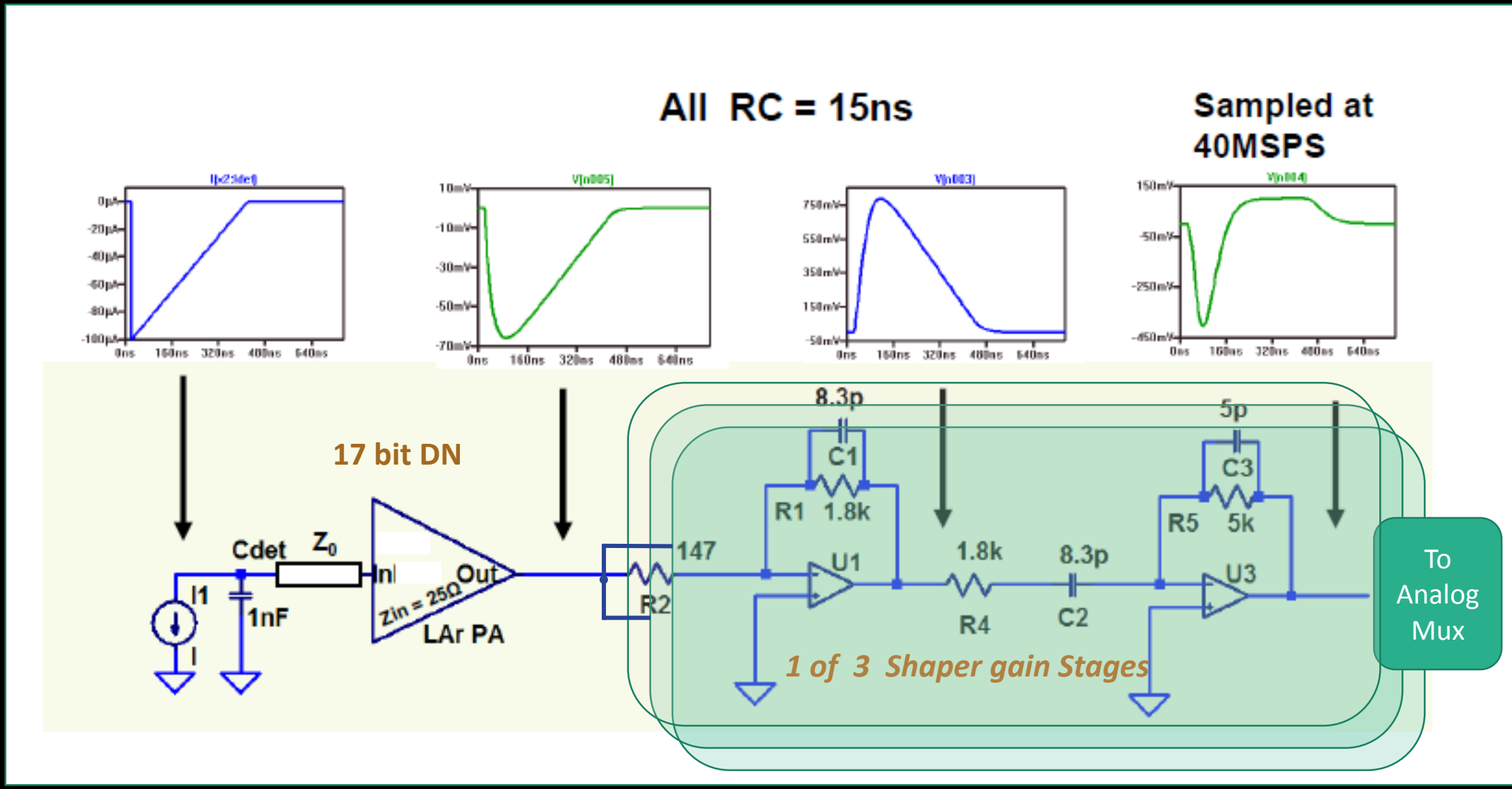
"Progress on requirements and design for the Phase-II analogue front-end"
***Nicolas Morange (LAL)**, at BNL June 3, 2015*

How many ADC bits are needed for Noise ?

Reclaim 2 bits and gain a factor of 2 in Dynamic Range ?



LAr Analog Front End (Phase 0 Approach)



HL-LHC Front End Implementations Under Study

Multi-ASIC/technology Solutions **ASIC 1** **ASIC 2**

- Preamp, **CR-(RC)^2** shaping* **ADC driver** → **ADC**
- Preamp, **RC** only shaping ADC driver→ **80MHz ADC Digital Filtering**

→ **Each above requires a data mux ,serializer and fiber driver**

One ASIC (65nm) System on a Chip Solution**

- **Preamp, CR – (RC)$^{n-1}$ shaping → ADC → serializer → fiber driver**
- **# gain Stages?**

**Collaborative Investigation BNL and LAL

Analog Front End Interface to ADC

Intimate connection to the choice of ADC parameters

- Least Count for noise estimation
- Effective number of bits ENOB .vs. Total number of ADC bits?
- ADC Gain LSB unit.
- DC ADC linear input Range → Differential -V to +V ? 0 - V ? (not likely)

→ Dynamic Range Required for Electronics Front End.

→ Pre Offset of analog output.

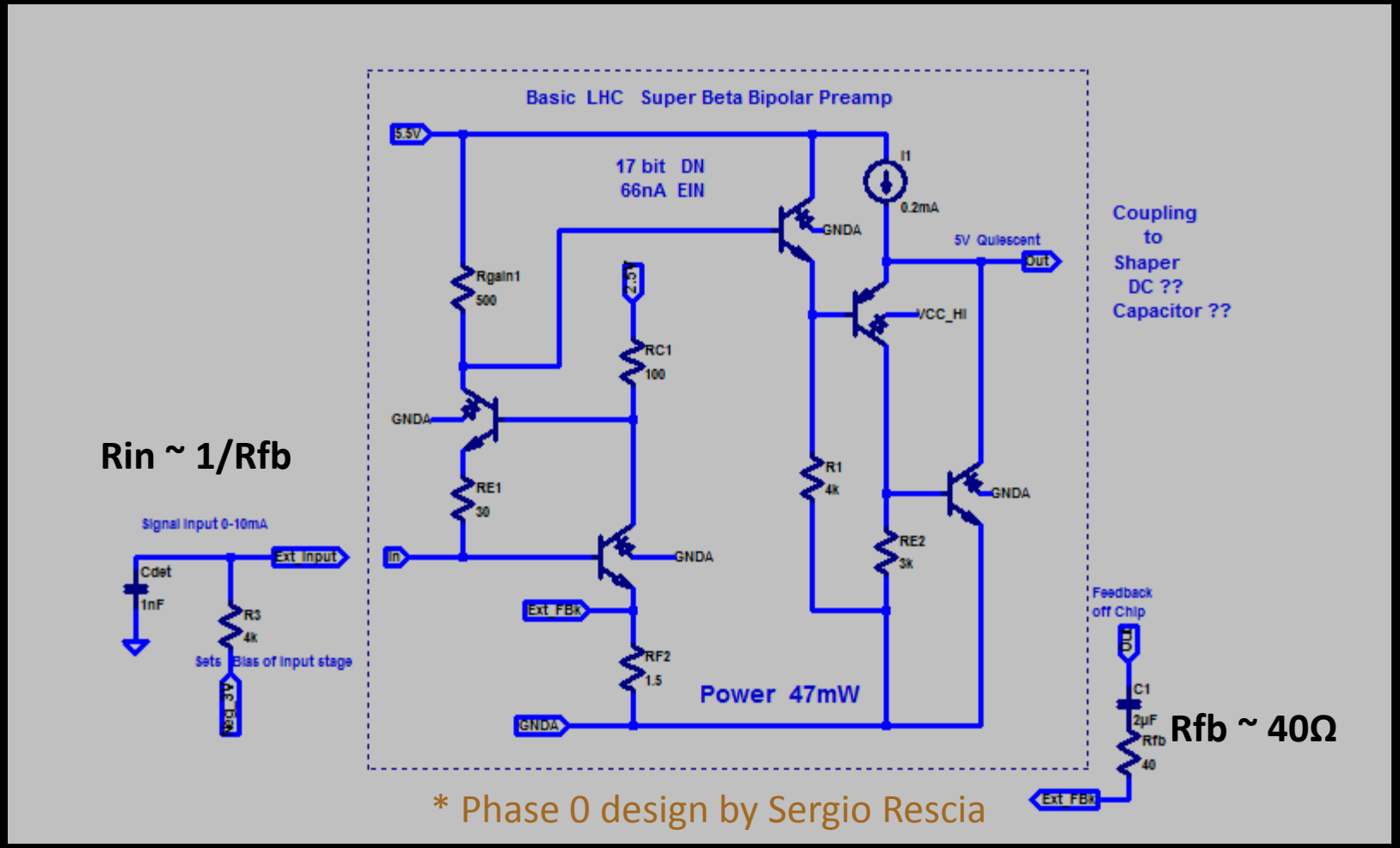
Ultimately these parameters determine the analog power requirement and the number of gain stages

Basic Bipolar Preamp Configurations

Input Termination Resistance	Max C detector	Max Input Time Const	Gain of Preamp	Max Input Current	Noise after CR-(RC)2 Cdet Max	Power
50Ω	200pF	10ns	1KΩ	3mA	32nA	34mW
25Ω	1.5nF	37.5ns	500Ω	10mA	100nA	47mW

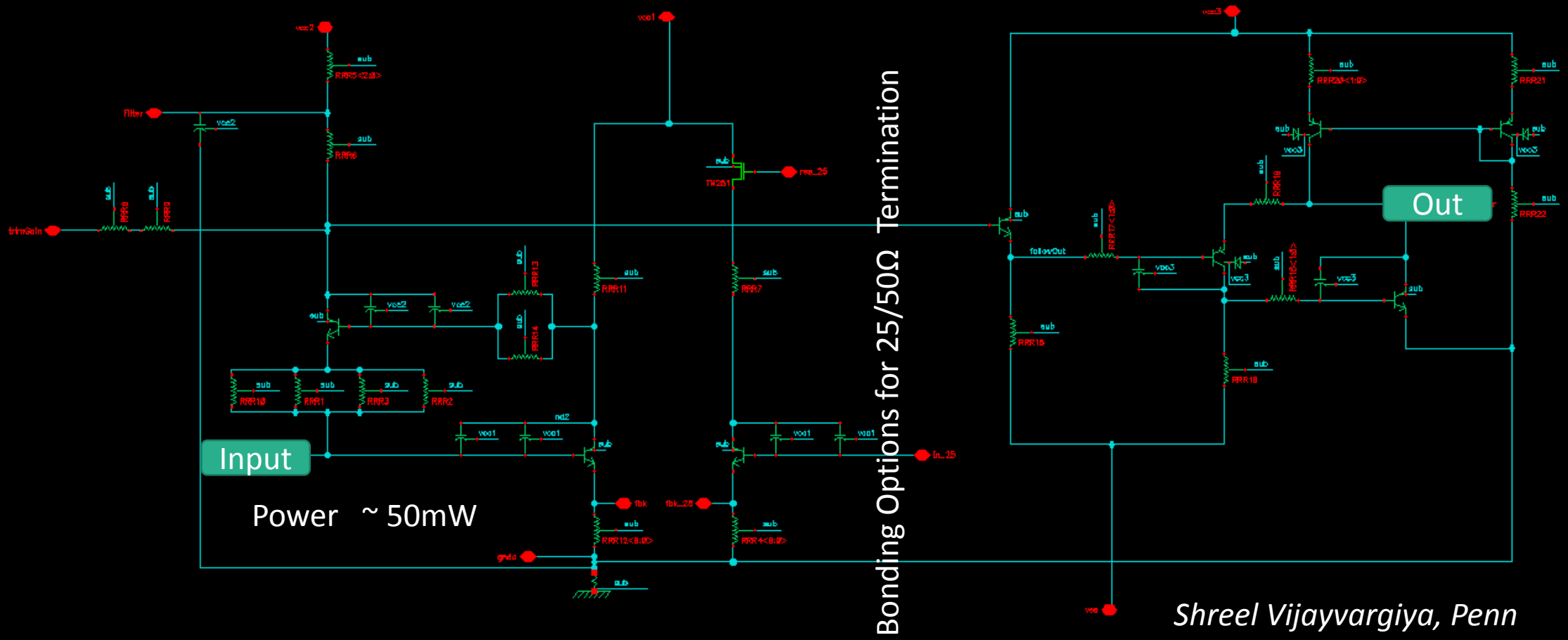
25Ω Preamp noise with shaping 66nA with 1nF Cdet

Phase 0 ATLAS LAr Bipolar Super Beta Preamp



Preamp Versions

Si Ge Bipolar Phase II version Slightly Modified Phase 0 version to allow for 25 (gain 500) or 50 (gain 1K) configuration



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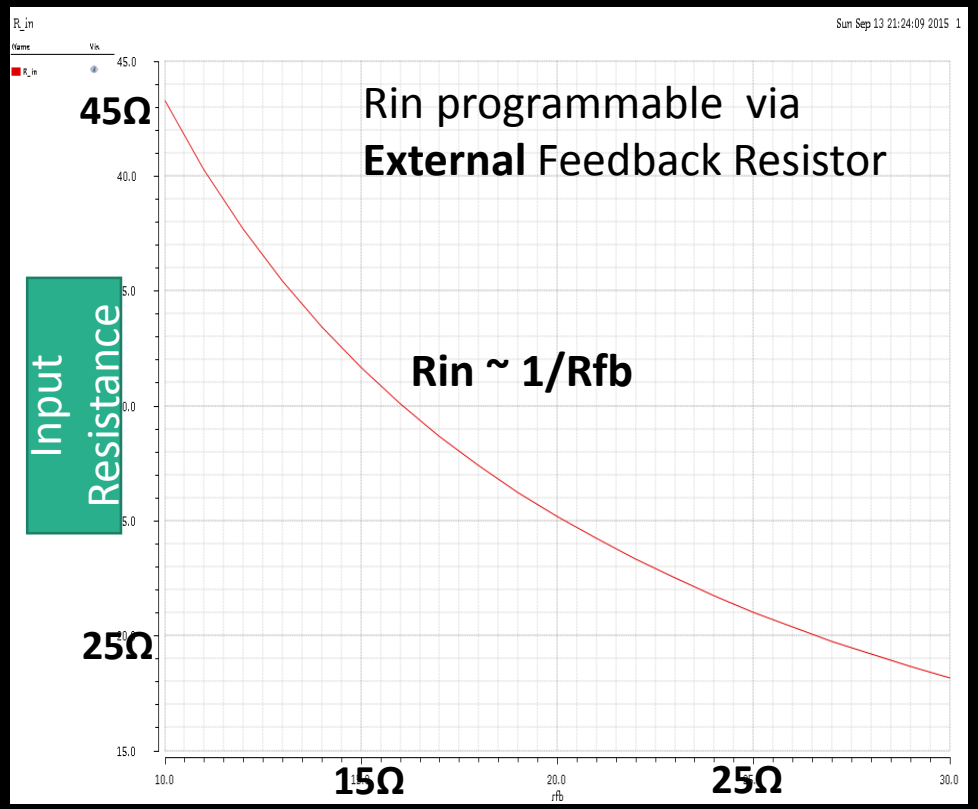
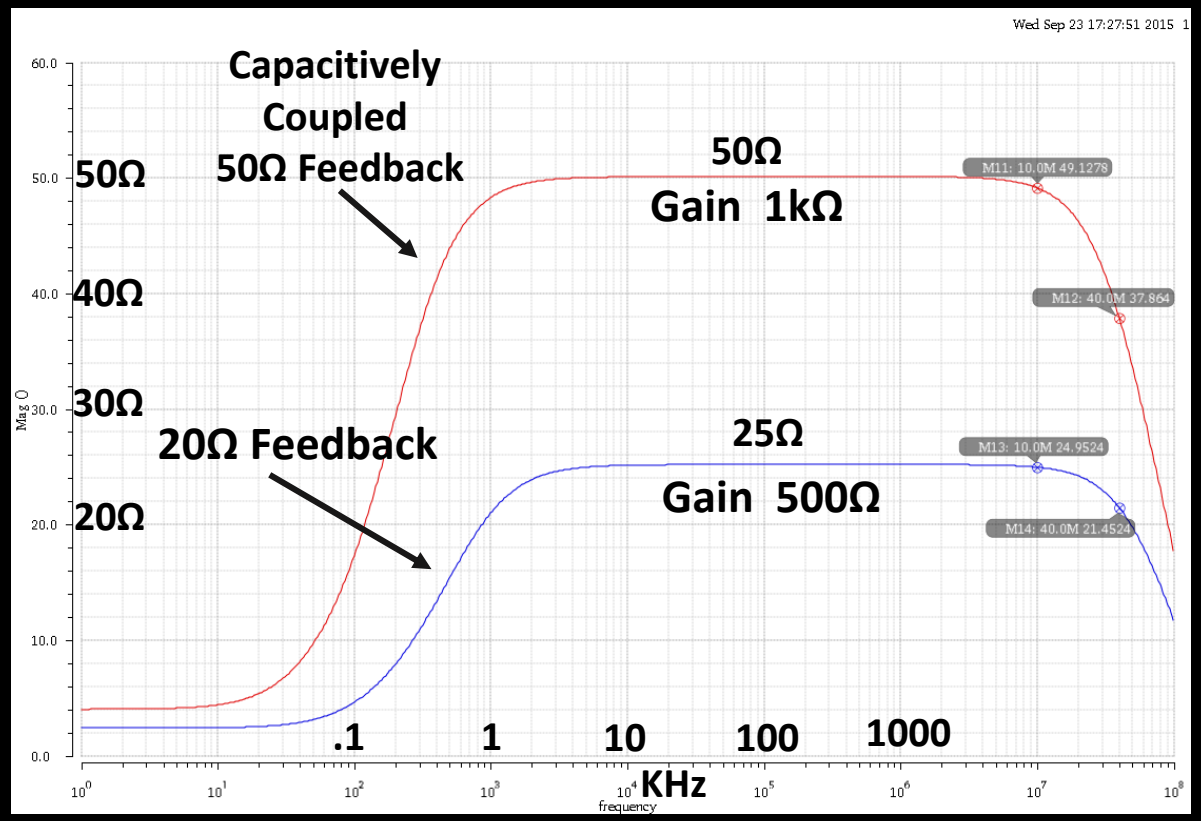
Bipolar Preamp Implementation

Preamp configured for 25 and 50Ω input impedance





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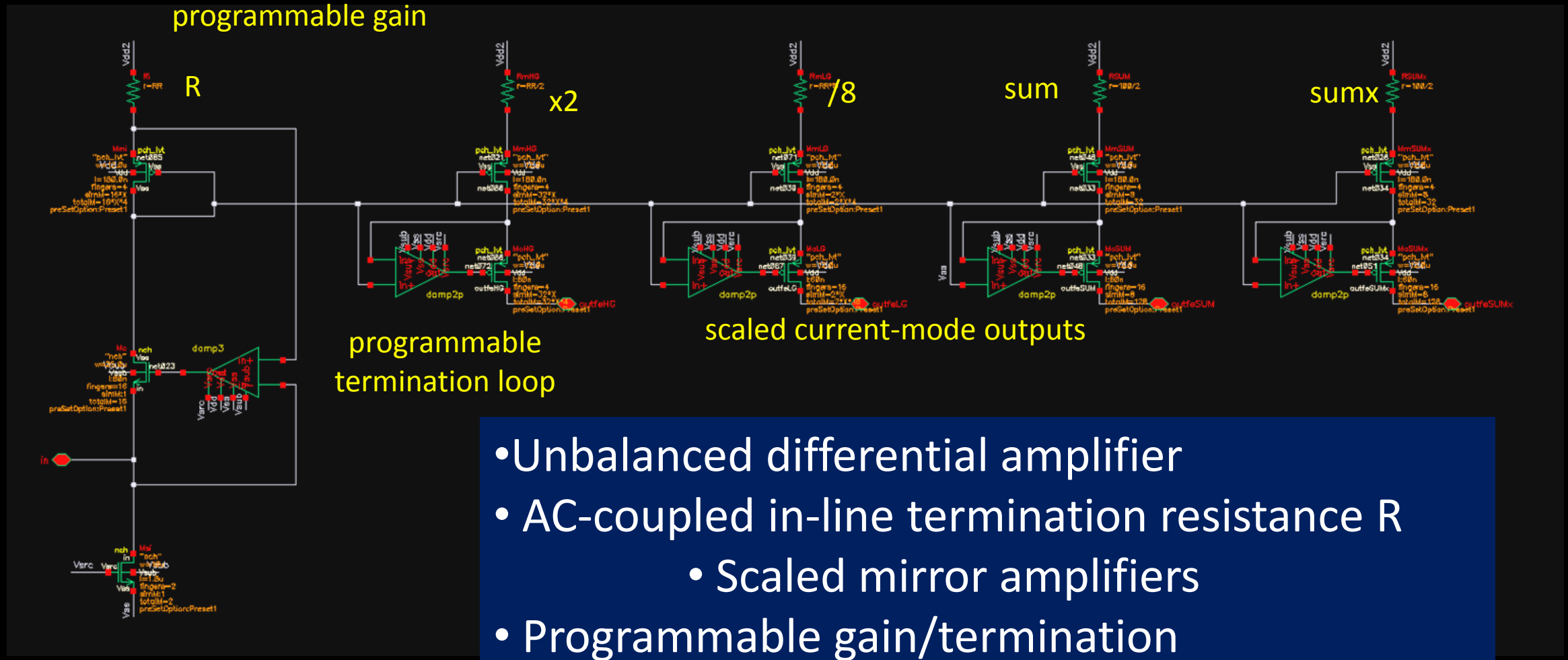
CMOS 65nm Front End Amplifier (SOC design)

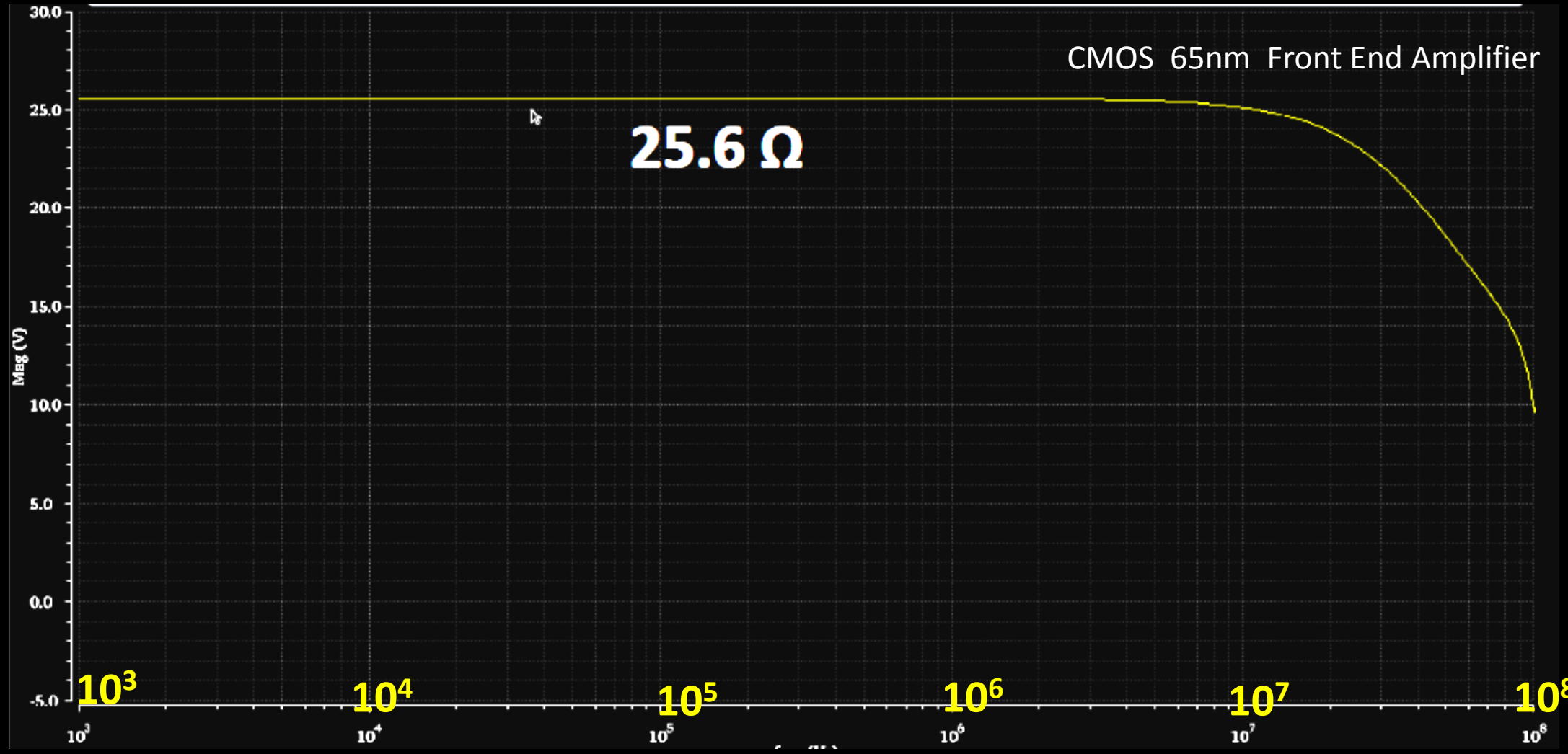
CMOS designs by Gianluigi De Geronimo, BNL



- Unbalanced differential amplifier
- AC-coupled in-line termination resistance R
  - Scaled mirror amplifiers
- Programmable gain/termination

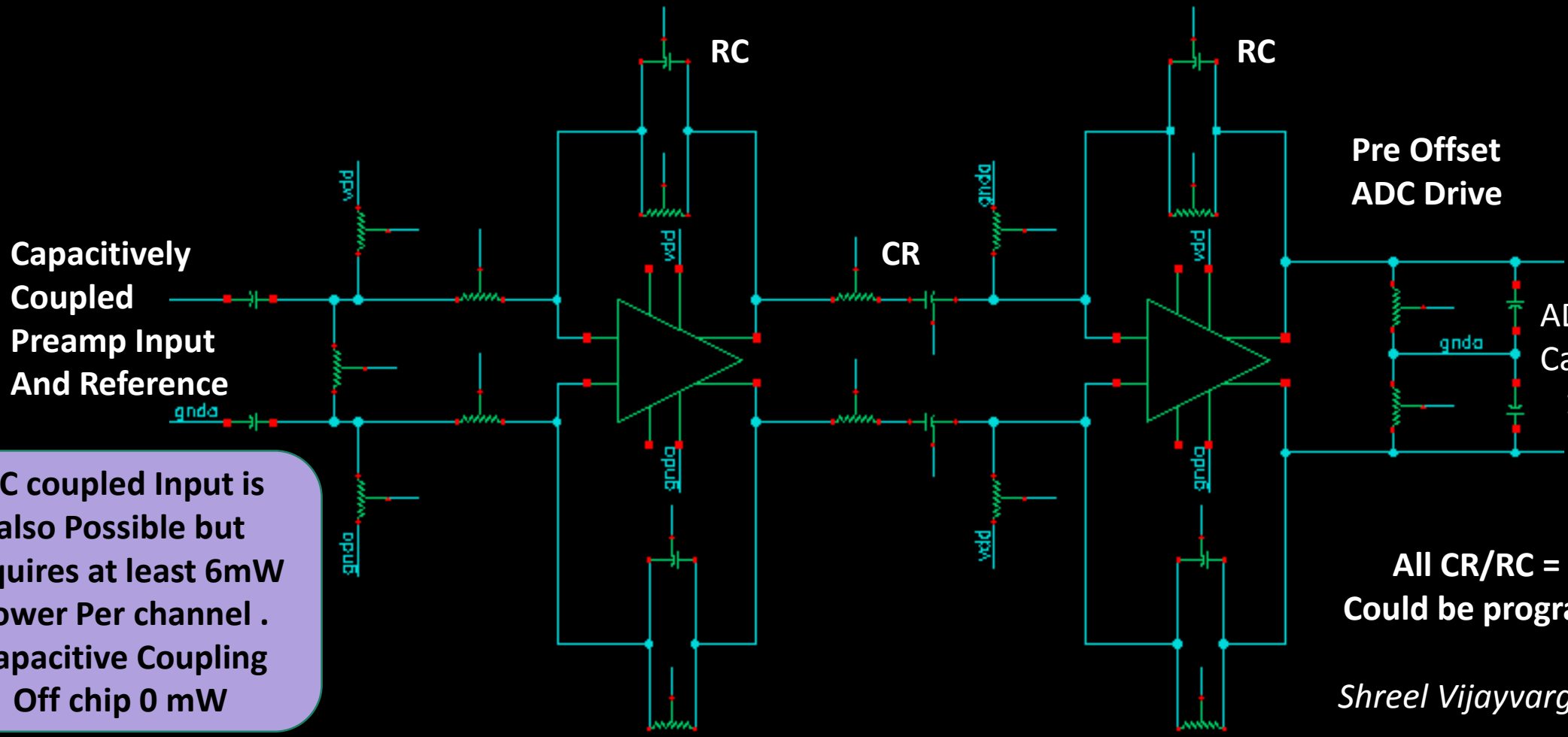
Termination Resistance Set to 25 vs Frequency

Results from Preliminary Design



Multiple ASIC solution: Shaper

Conventional Shaping with Opamps and differential ADC drivers



DC coupled Input is also Possible but requires at least 6mW Power Per channel . Capacitive Coupling Off chip 0 mW

All CR/RC = 15ns
Could be programmable

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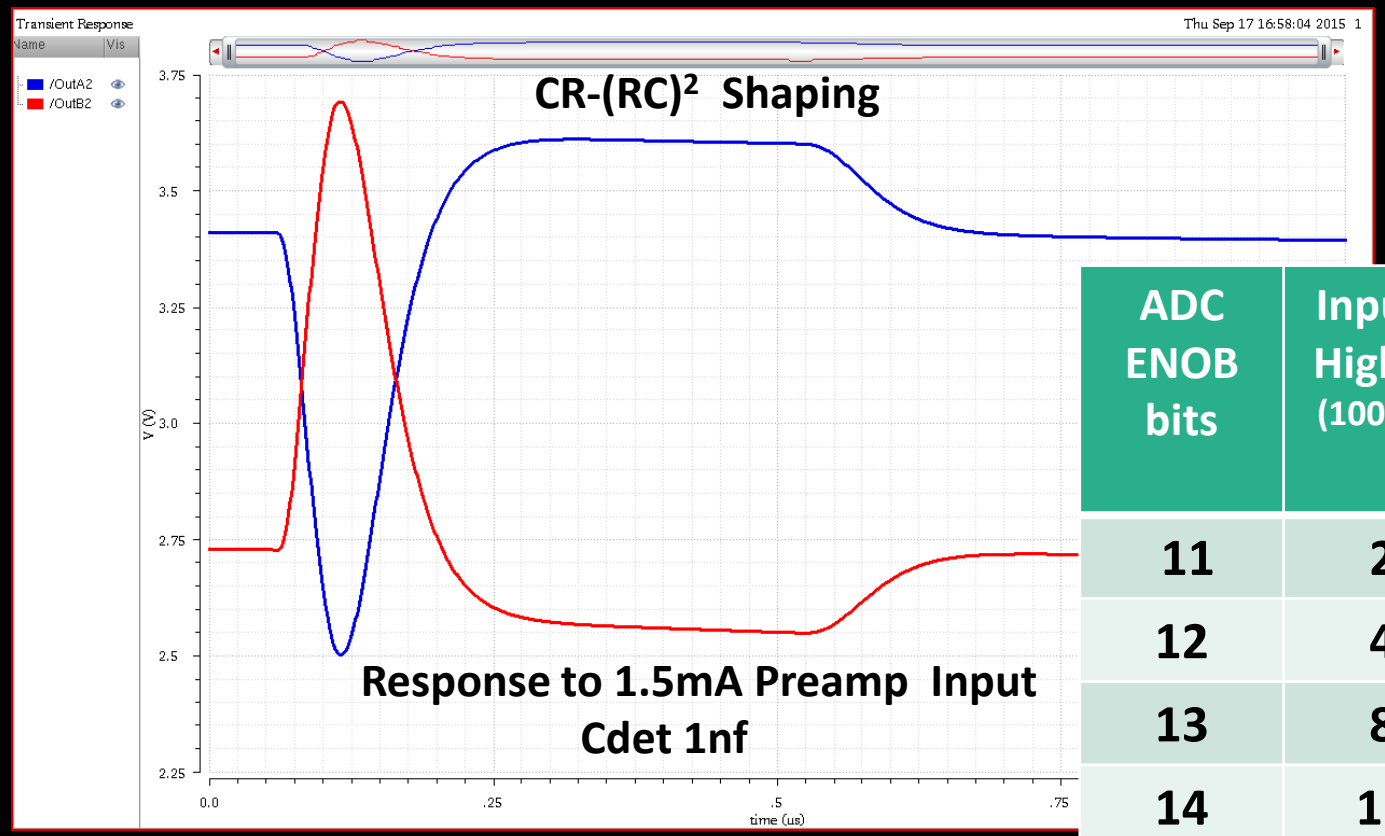
Shaper Optimization depends on ADC design

Differential Output to ADC 10pF on each output

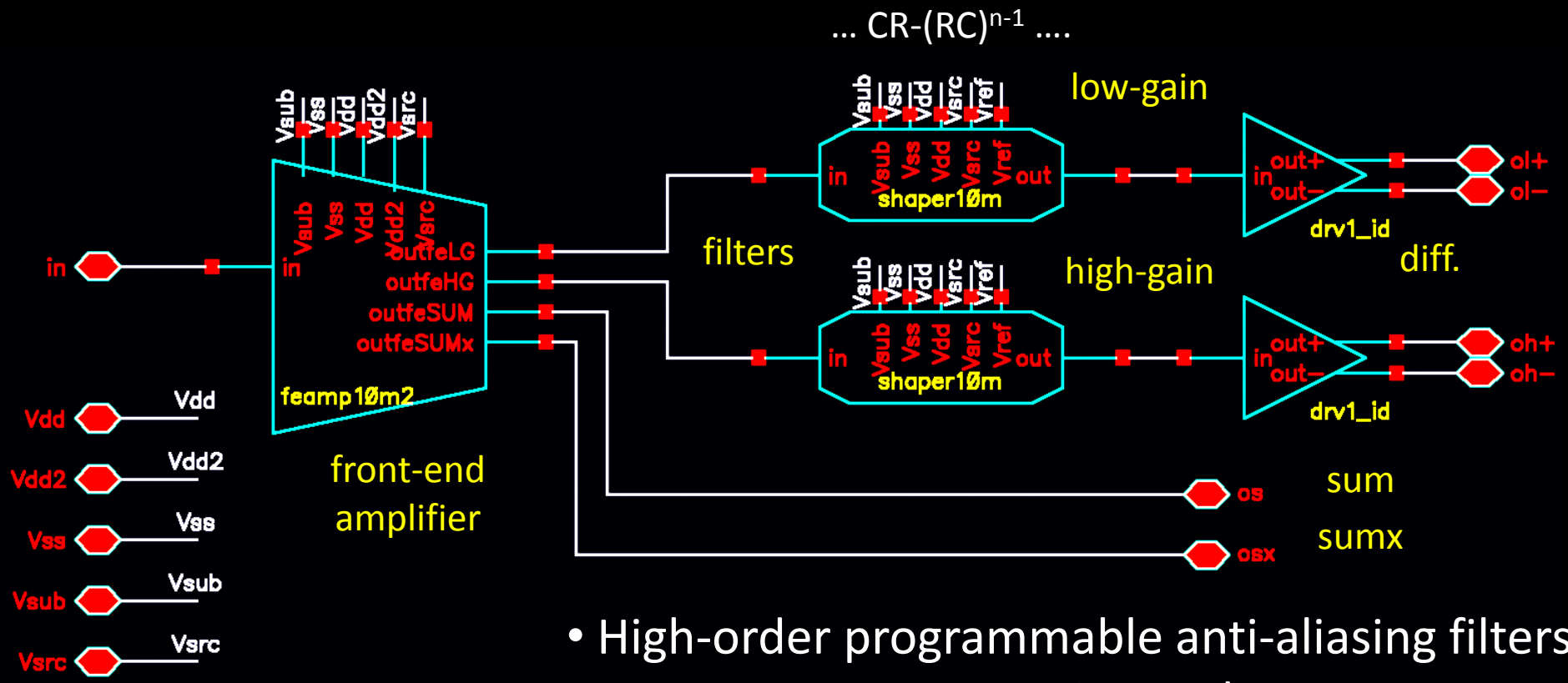


Optimization Requirements:

- 100nA ENI full chain Readout
- 10mA FS range
- Integral Non Linearity < .1%
- 10pF ADC inputs Settling to least count in 25ns (40MSPS)
- Max Signal output differential 2.2V

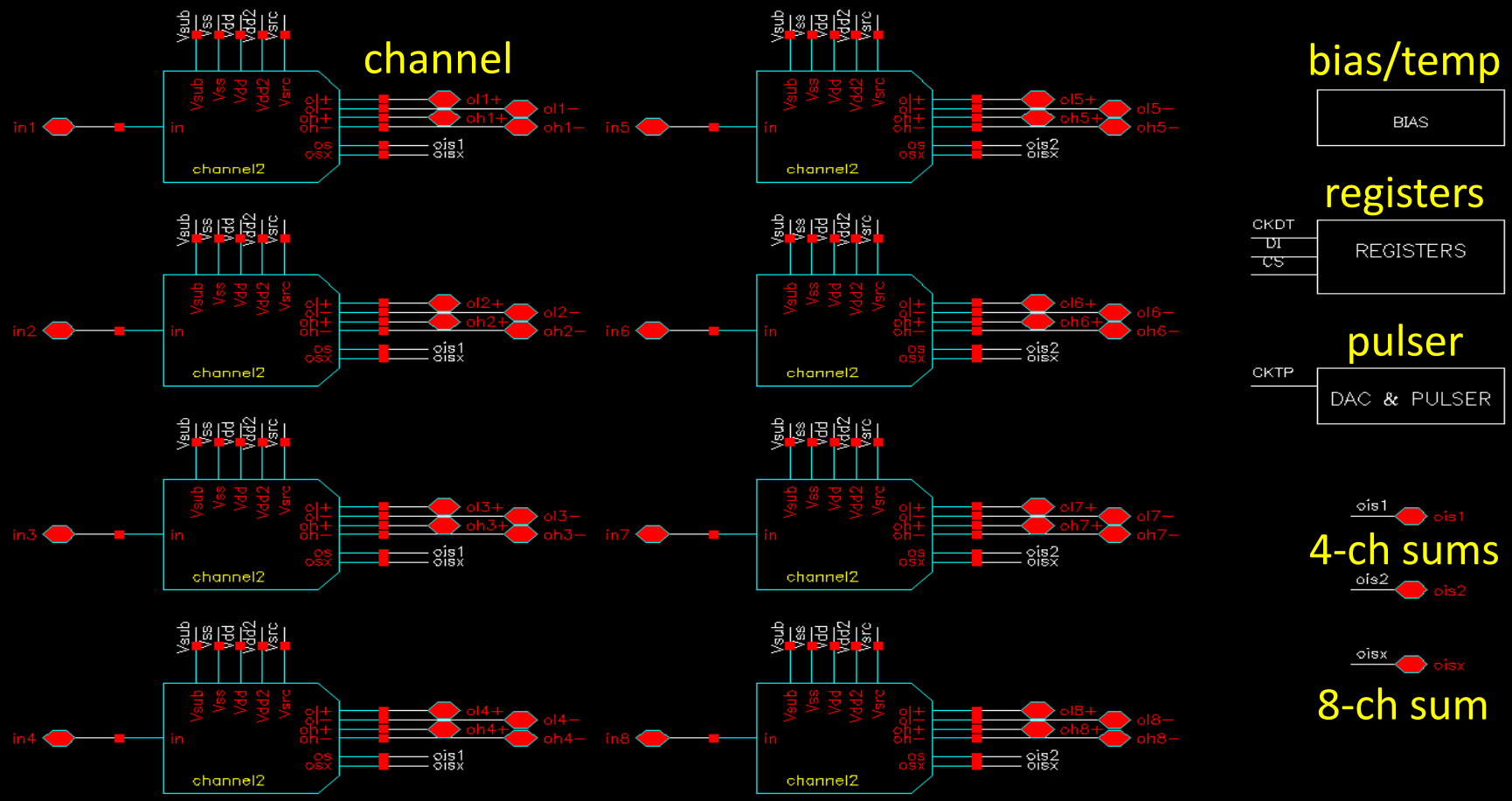
ADC ENOB bits	Input FSR High Gain (100nA/cnt) uA	# stages 10mA FS	Power for High Gain Low Noise (bipolar) Stage AND 9mA DN Preamp
11	200	3-4	Req. extra Gain Stage
12	400	3	100 mW
13	800	2	120 mW
14	1600	2	140 mW

CMOS 65nm Prototype Channel Design



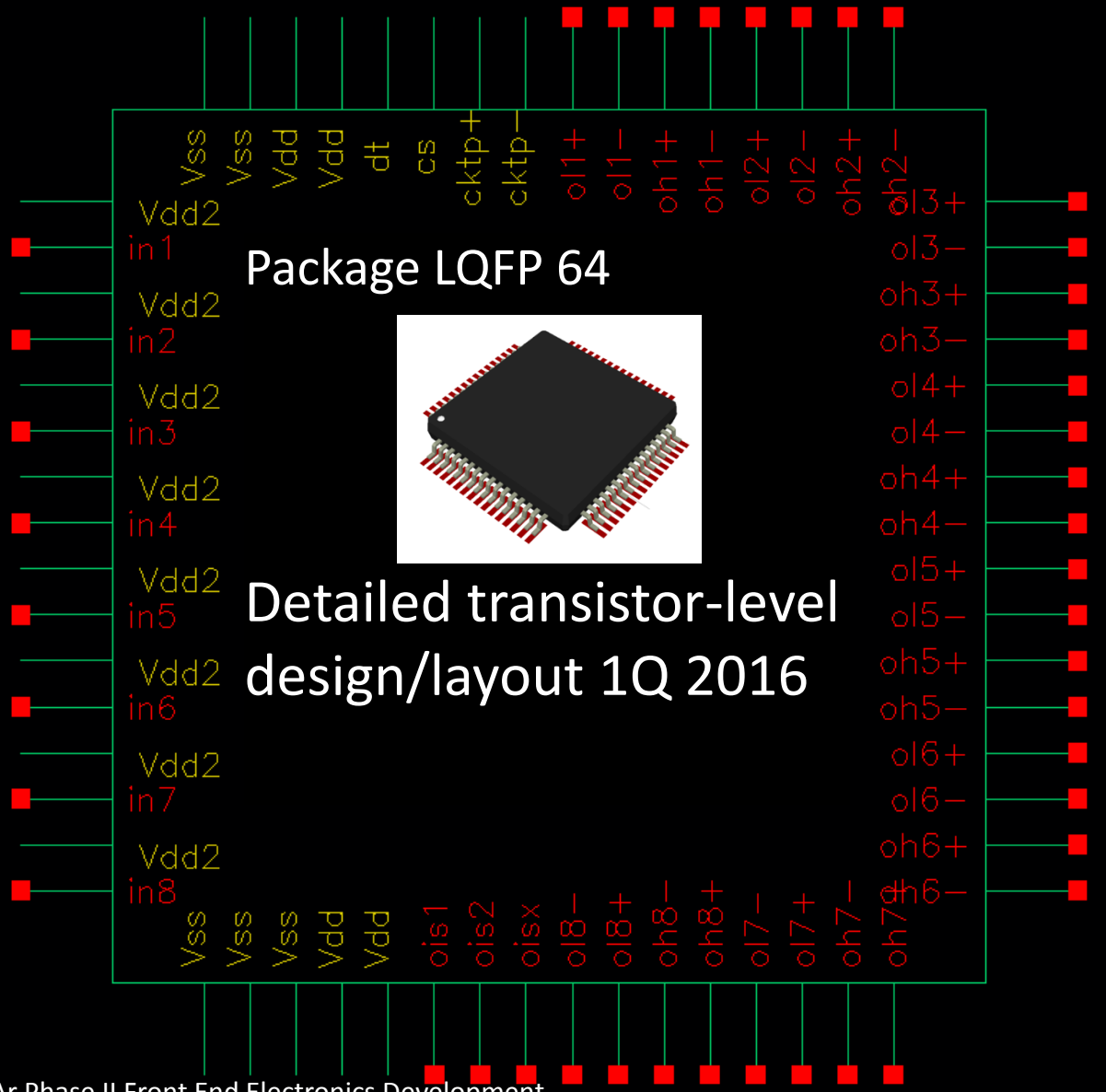
- High-order programmable anti-aliasing filters
- Current-output summing nodes
- Differential outputs

CMOS 65nm 8 Channel Prototype Chip Blocks



Top Level

CMOS Prototype for qualification of Process for System on a chip (SOC) Design



Digital Filtering Alternative

Multi-ASIC solution

Using the same preamp and a Single Ended to differential ADC driver with one 'RC' pole the shaping could be arbitrarily customized off detector using digital filters after conversion to perform the remaining CR-RC shaping.

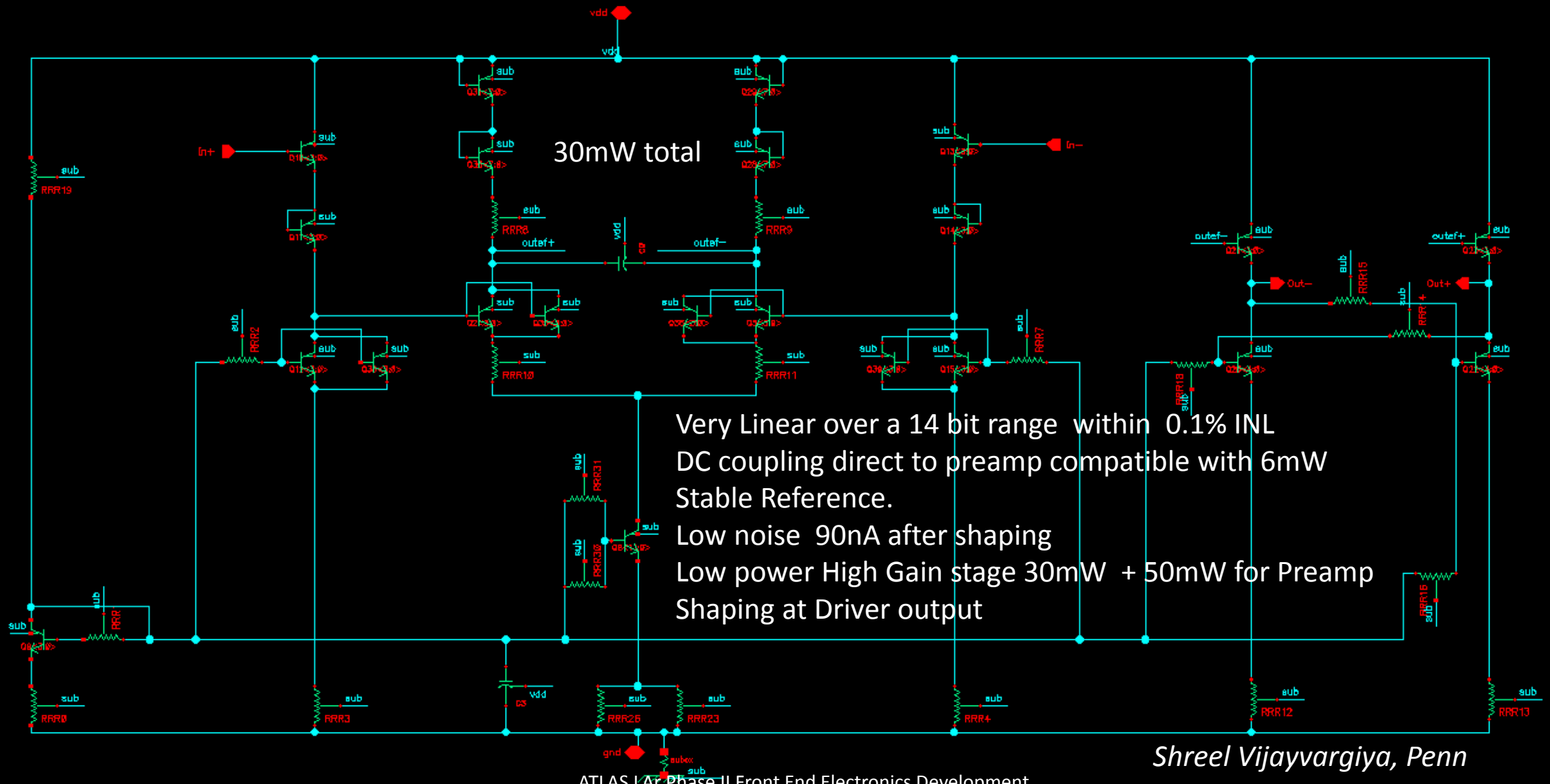
Unknowns:

- Required number of ADC bits to achieve the same effective noise level as the digitized fully shaped analog signal.

  → In the analog shaping a factor of 5 in amplitude is lost to the CR shaping

- Sample Rate due to the strong differentiation of the CR shaping and the radiation contamination of the HL-LHC environment a higher digitizing rate of ~ 80Mbps would be required.

Bipolar Single Ended to Differential Converter



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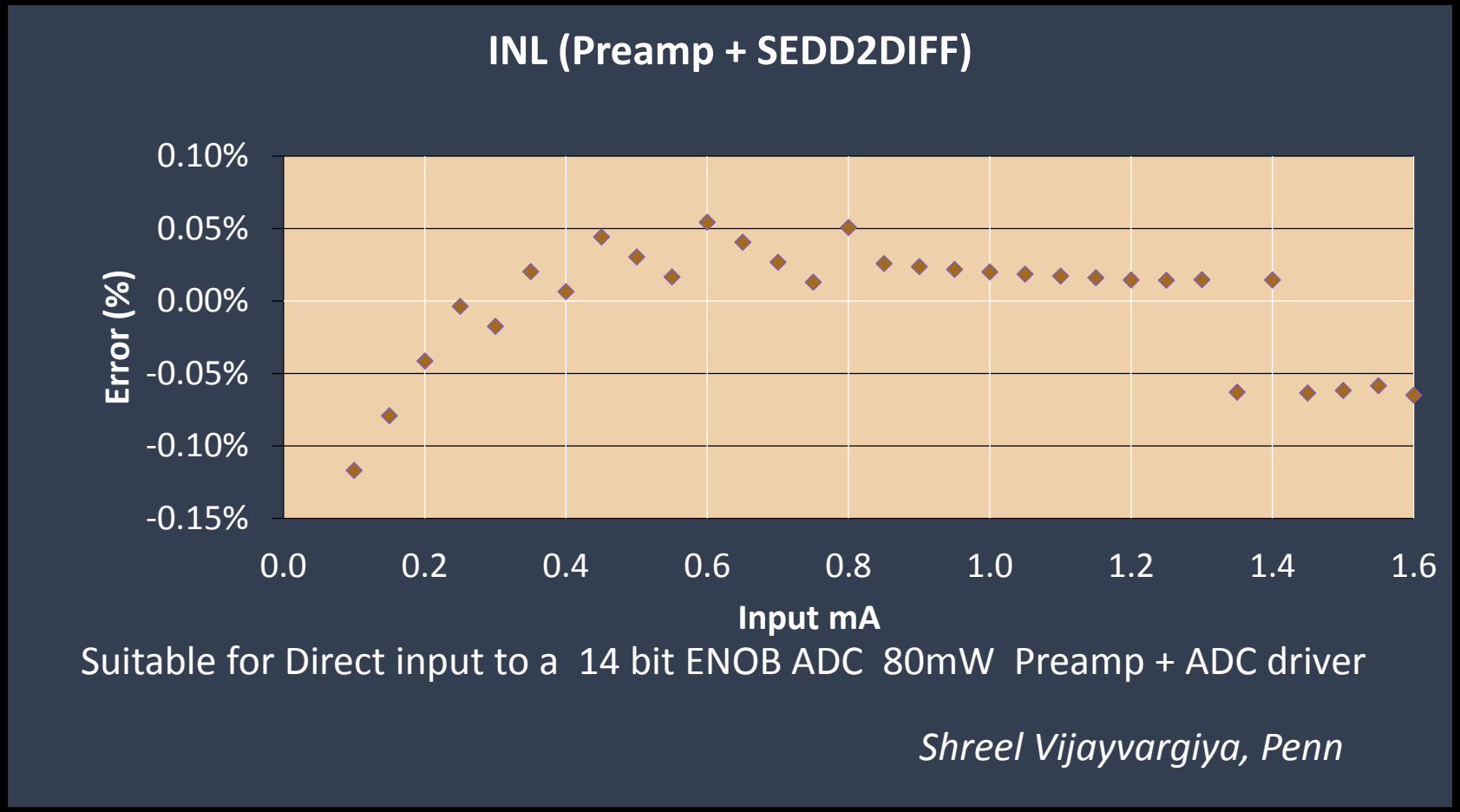
Linearity



Suitable for Direct input to a 14 bit ENOB ADC 80mW Preamp + ADC driver

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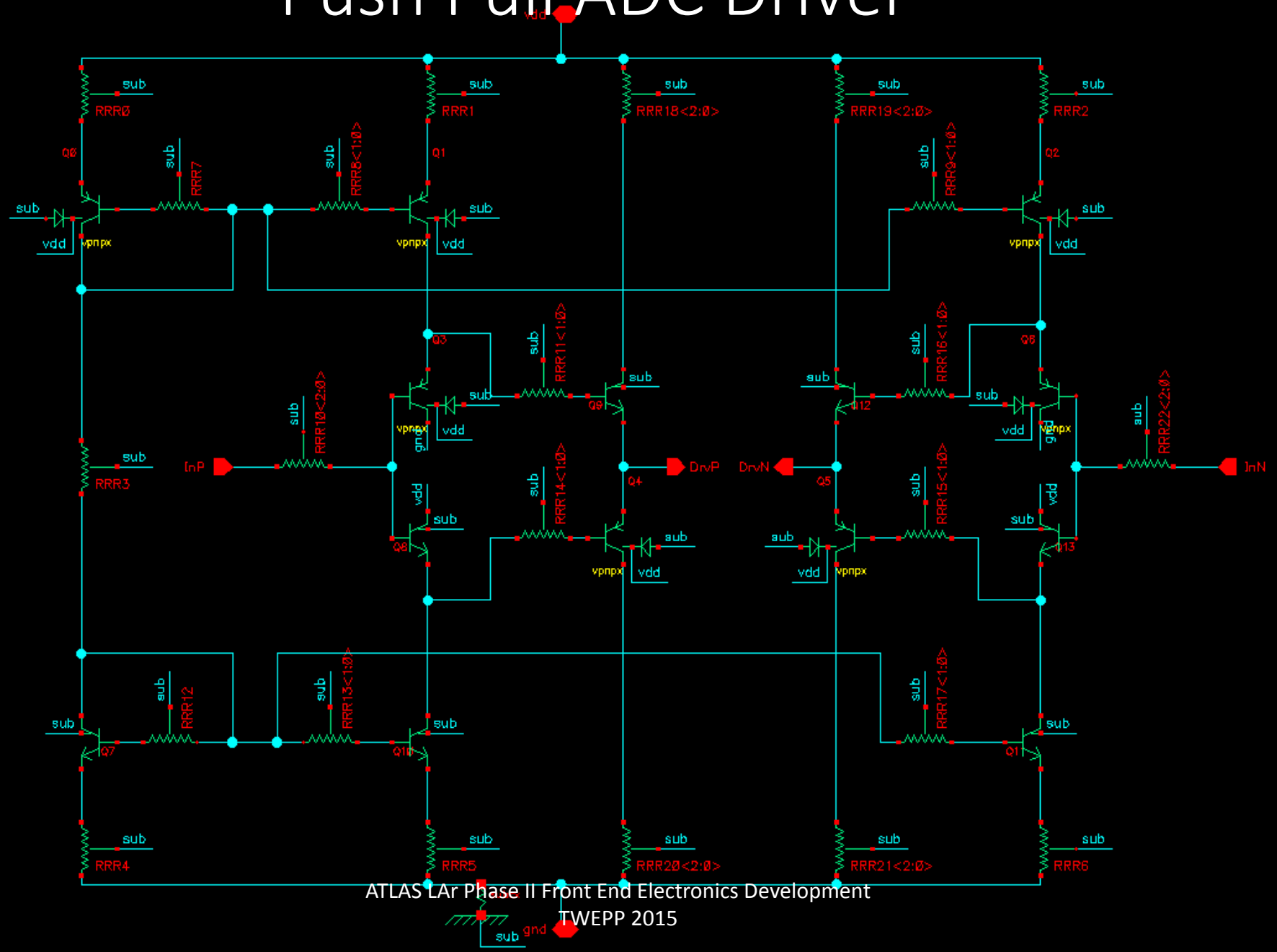
Summary

- Several Approaches for the ATLAS LAr Phase II Front End electronics are underway.
- Finalized Analog Specifications being formulated in parallel will help determine final tradeoffs in power, linearity and number of gain scales.
- A new approach using 65nm CMOS is competitive with current bipolar approach and may provide a significant savings in parts count and power on the 128 channel FEB.
- Digital Filtering of a minimally shaped signal may offer the opportunity to optimize signal shaping long after the integrated circuit designs have been committed. Much more study need to be done on the analog and ADC requirements for such a filter.

Backup

Push Pull ADC Driver



Differential OTA schematic with Push Pull Driver