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Development of ATLAS Liquid Argon Calorimeter Read-out Electronics for the HL-LHC

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The high-luminosity phase of the Large Hadron Collider will provide a 5-7 times greater instantaneous and total luminosities than assumed in the original design of the ATLAS Liquid Argon Calorimeters and their read-out system. An improved trigger system with higher acceptance rate and longer latency and a better radiation tolerance require an upgrade of the read-out electronics. Concepts for the future read-out of the 183.000 calorimeter channels at 40-80 MHz and 16 bit dynamic range, and the development of radiation tolerant, low noise, low power and high-bandwidth electronic components will be presented.

Summary

The High-Luminosity LHC (HL-LHC) is requiring operation of the LHC and associated detectors at luminosities of up to $(5-7.5) \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, with the goal of accumulating an integrated luminosity of 3000 fb⁻¹. To be able to retain interesting physics events even at rather low transverse energy scales for single objects, increased trigger rates are foreseen for the ATLAS detector. At the Level-0 and Level-1 selection stage acceptance rates of 1MHz and 400kHz are planned, combined with longer latencies in order to read out the necessary data from all detector channels. Under these conditions, the current read-out of the ATLAS Liquid Argon (LAr) Calorimeters does not provide sufficient buffering and bandwidth capabilities. Furthermore, the expected total on-detector radiation doses of 10^{13} neq/cm^2 (NIEL) and 0.3 kGy (TID) are beyond the qualification range of the current front-end electronics. For these reasons a complete replacement of the LAr front-end and back-end read-out system is foreseen.

The new electronics must capture the triangular detector pulses of about 600 ns length with signal currents per channel of up to 10 mA and a dynamic range in excess of 16 bit. The noise should be kept below 100 nA and the power per front-end channel should not exceed 50 mW. With the available ASIC technologies different concepts of the read-out design will be possible.

In 180 nm SiGe technology (IBM 7WL) and choosing unipolar shaping, two gain stages can cover the desired dynamic range. An ADC matching this pre-amplifier and shaper will need to provide 14 bit digitization range. Such a design is shown to meet the noise requirements and achieve an integral non-linearity below 0.1%. Moreover, in simulations of the complete read-out chain using the unipolar shaping approach signal pile-up is introducing a controllable baseline shift, and an additional digital CR shaping stage does not introduce a degradation of the energy resolution.

Alternatively, a development of pre-amplifier and shaper as well as SAR ADCs is performed in 65 nm CMOS technology. Due to the lower voltage range, a 4-gain design of the analog part is studied with programmable peaking time to optimize the noise level in presence of signal pile-up. The 64 nm ADC is laid out in SAR architecture and is completed with an active SEE detection mechanism by feeding the signals into two ADCs in parallel and comparing their output. In this way, the signal-to-noise ratio can be further improved in presence of radiation. Results for a 80 MHz 12-bit prototype design show ENOB values above 10.8 bits after 10 kGy irradiation, and similar performance is reached for a 14-bit layout.

In this contribution, results from simulation of the performance of the ATLAS LAr Calorimeter read-out system for the different options, as well as from the design studies and first test of the ASIC components will be presented.

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