



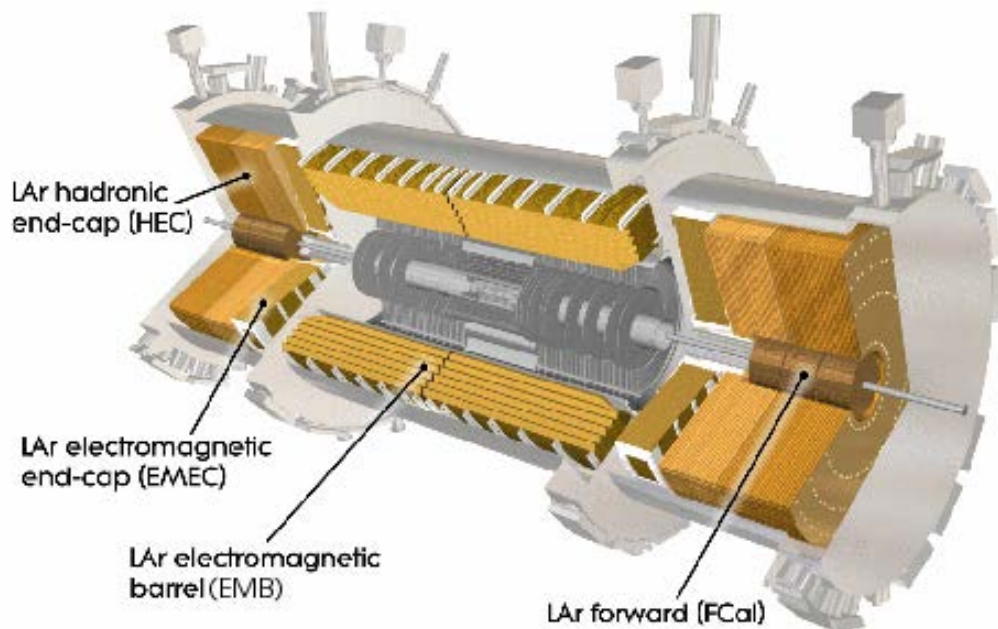
Performance of the Demonstrator System for the Phase-I Upgrade of the Trigger Readout Electronics of the ATLAS Liquid Argon Calorimeters

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on behalf of the ATLAS Liquid Argon Calorimeter Group***

Outline

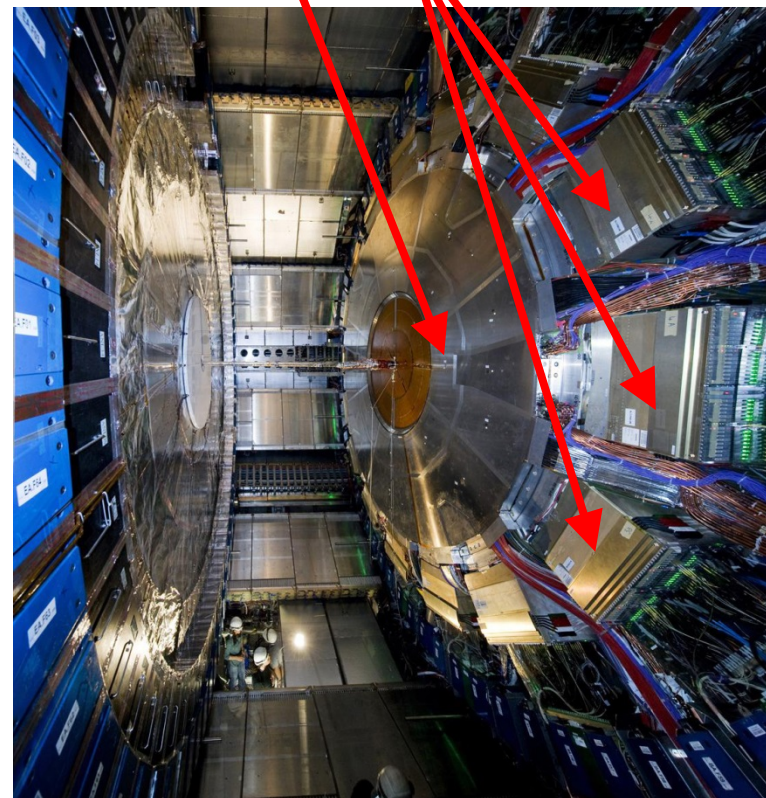
- ***LHC and ATLAS Liquid Argon calorimeter***
 - *ATLAS LAr calorimeter*
 - *LHC schedule*
- ***LAr calorimeter Trigger Demonstrator***
 - *Motivation*
 - *Readout Electronics and components*
 - *Installation*
 - *Results*
- ***Summary***

ATLAS LAr calorimeter



- LAr calorimeter : 182k channels
- Front End : 1600 Front End Boards
- Back End : 200 Readout Out Driver boards

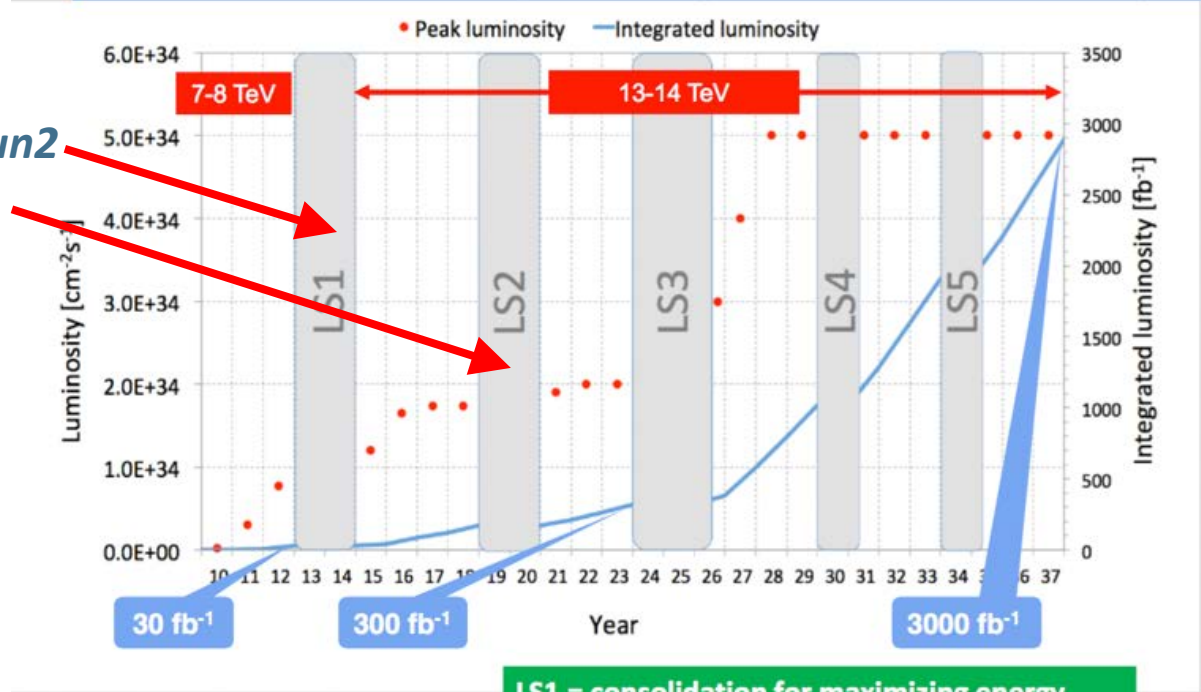
Front End Crates
Calorimeter



Between Electromagnetic barrel and end-cap

LHC schedule

LHC roadmap: Integrated luminosity



Demonstrator LS1/Phase0->Run2
 Electronics LS2/Phase1->Run3

LS1 = consolidation for maximizing energy reach of the LHC (8 to 14 TeV)
 LS2 = LIU for beam intensity upgrade
 LS3 = HL-LHC for luminosity upgrade

CERN
 Status of LHC and HL-LHC
 EPS-HEP 2015 conference
 Frédéric Bordry
 27th July 2015

→ Luminosity increase

Number of interactions per bunch crossing doubled.....

→ Pile up effect

Triggering electromagnetic objects suffer from huge multi-jets background

Upgrade and demonstrator motivation

- **Current electron and photon (EM) trigger selections alone**

Would be 270 kHz under Run 3 (after LS2) luminosity and pileup conditions

- **Reducing the single EM trigger rate to the desired bandwidth of 20 kHz**

Would require a significant increase of transverse energy thresholds

- **Need to introduce a new concept of EM trigger**

New EM trigger system will be installed in parallel of the current system but in *principle* we should not use the old one (for smooth startup after LS2)

- **Demonstrator motivation**

Install the new concept covering a small area of the detector : June 2014

-> One Front End Crate over 32 is equipped with the new electronics for the demonstrator

-> Part of the calorimeter covered by the demonstrator : $1.767 < \phi < 2.160$, $0 < \eta < 1.4$

Do not disturb the current system

Learn from this new system (pulse shapes, timing...)

Super cells

- **Current concept : Trigger Tower**

E_T sum in an area of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$

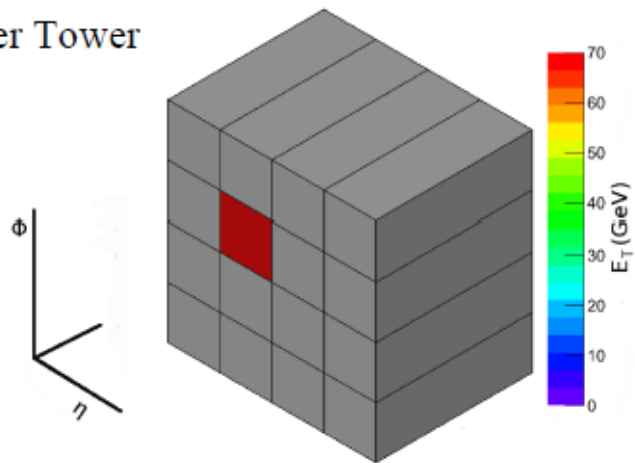
- **New concept : Super Cell**

Finer segmentation : area down to $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$

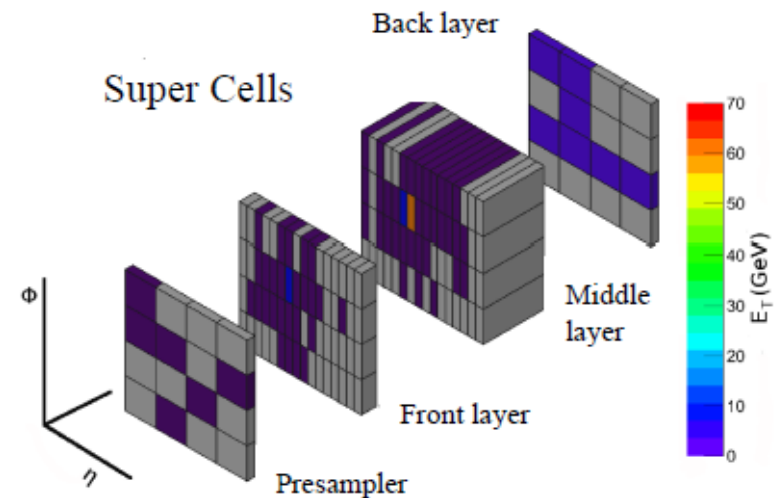
Granularity depends on the detector layers

- **Typically Trigger Tower consists of 60 Super Cells**

Trigger Tower



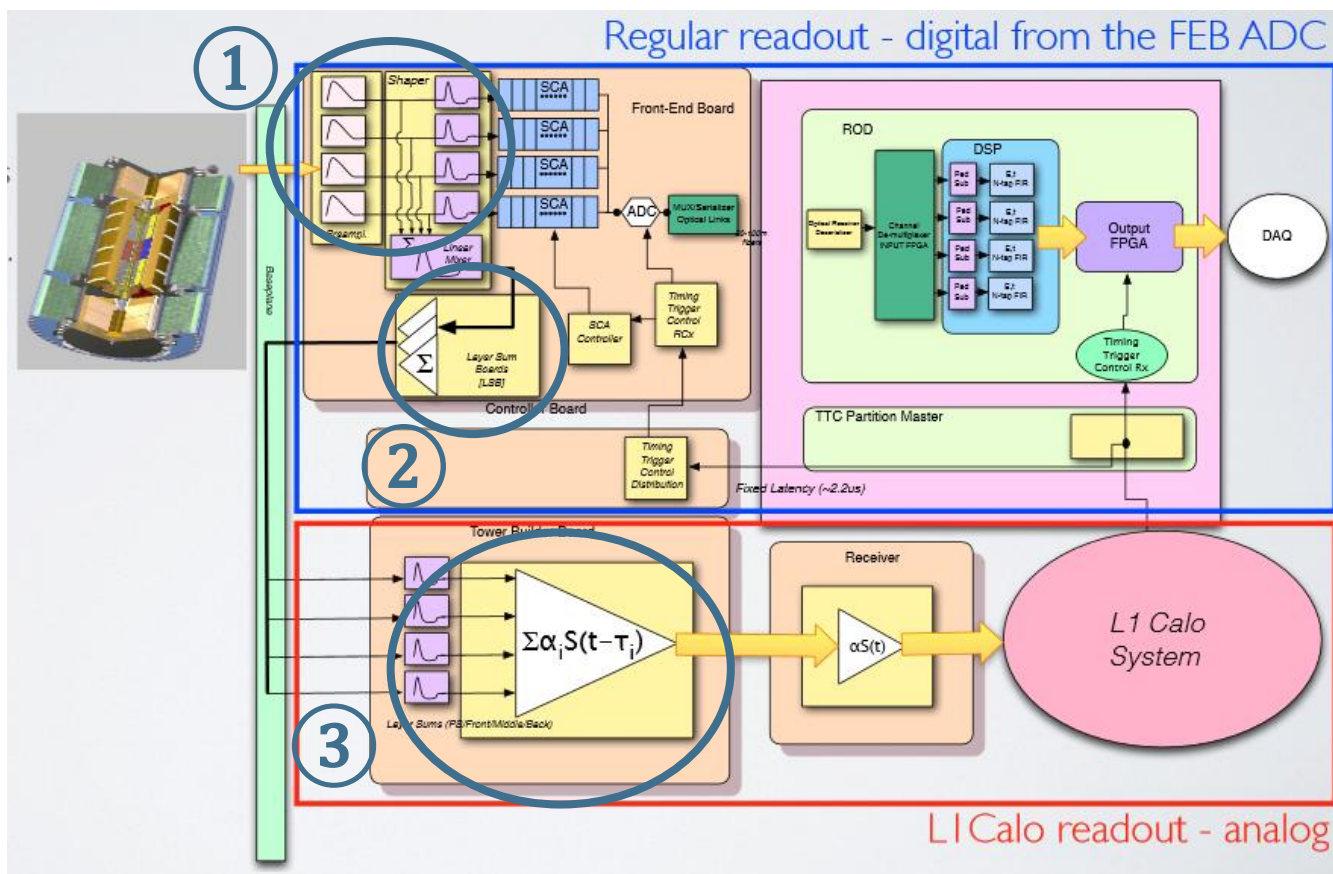
*70 GeV electron shower
seen into only one Trigger Tower*



*70 GeV electron shower
seen into multiple Super Cells*

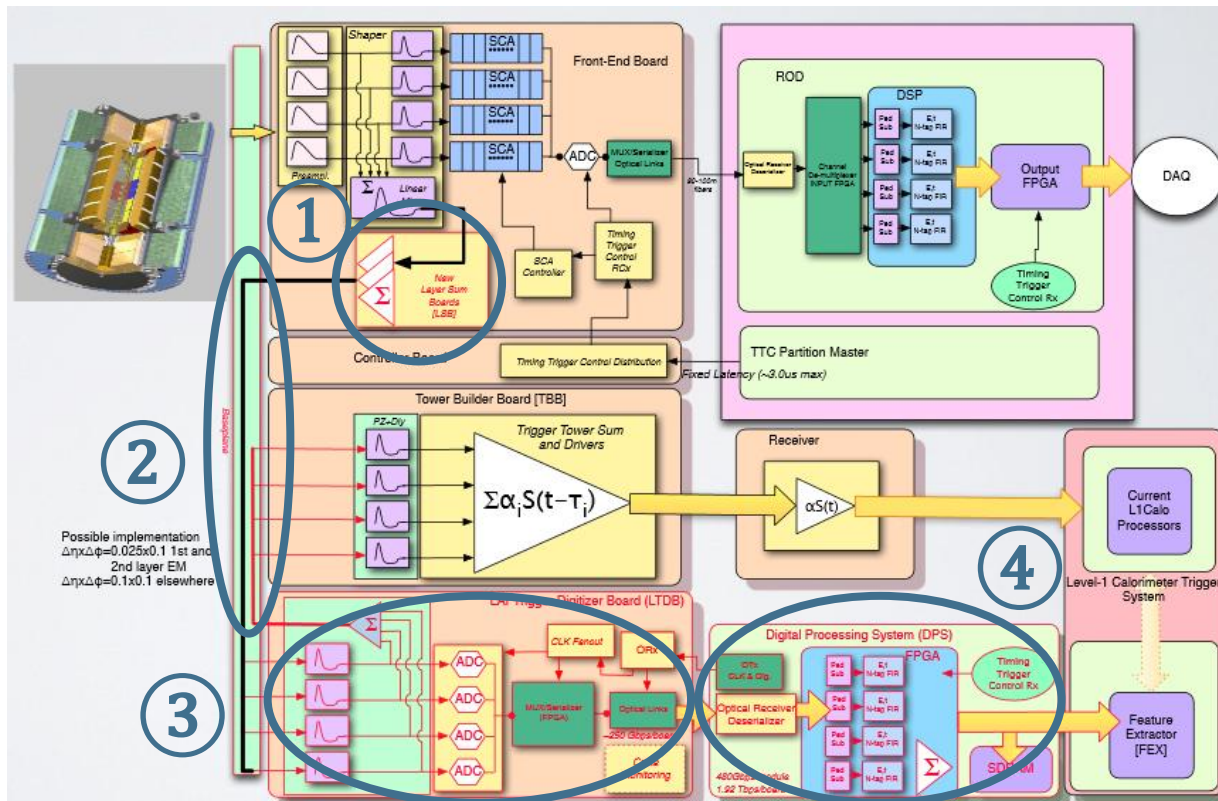
Trigger architecture – Current system (analog)

- ① -> Cell signals are amplified and shaped
- ② -> Summed by *Layer Sum Board (LSB)* and sent to *Tower Builder Board (TBB)*
- ③ -> Trigger Tower Builder sums analog signals from LSB



Trigger architecture – Upgrade system (digital)

- ① -> New LSB : forms *Super Cell*
- ② -> New backplane : transmits SC to LTDB and sums to *Tower Builder Board*



- ③ -> *LAr Trigger Digital Board (LTDB)* : digitizes SC at 40MHz, generates analog sums
- ④ -> *LAr Digital Processing Board (LDPB)* : reconstructs E_T for L1A Calo system

Upgrade, Demonstrator: LSB, Backplane

- **Layer Sum Board (LSB)**

Forms finer granularity Super Cell and drives the signals to LTDB

Energy quantization down to 64 MeV to 250 MeV instead of 1 GeV

- **Backplane**

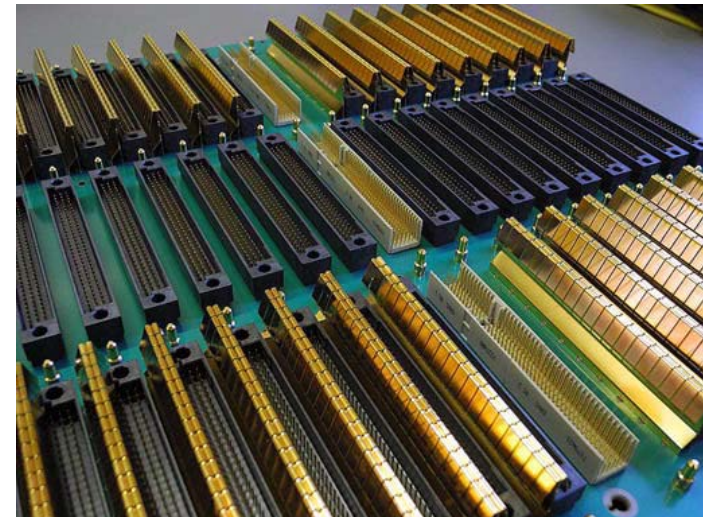
5 possible configurations (EM Barrel, 2xEM End Cap, H End Cap, Fcal)

Transmits new sums to Trigger Tower Builder

Transmits new Super Cells signals to LTDB

For demonstrator -> EM Barrel

-> **Demonstrator : 2 backplanes changed**

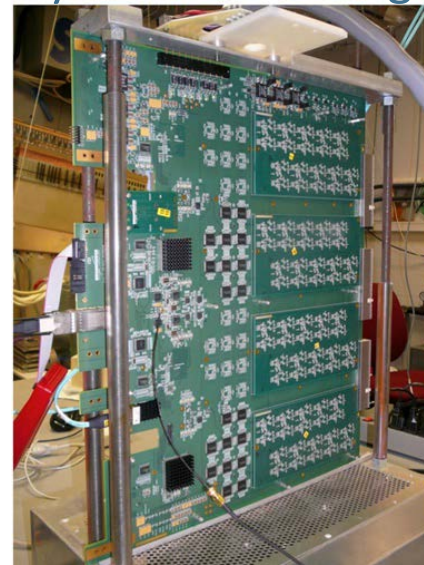


EM barrel backplane

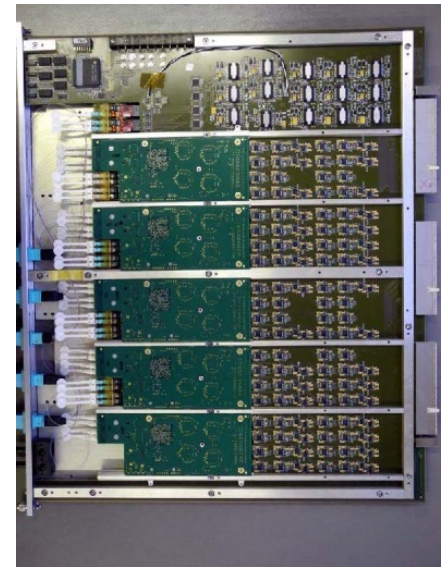
Demonstrator : LTDB

- *Handles up to 320 Super Cell signals*
284 Super Cells in EM Barrel, 312 in EM End Cap
- *Super Cells signals are digitized with 12bits ADC@ 40MHz*
ADC COTS : TI ADS5272
- *Multiplexing of 8 Super Cells on one 4.8Gbps optical link*
8B10B encoding, K code sent every Bunch Crossing
FPGA (XILINX/ALTERA)
40 transmitter optical links
Output : ~ 200Gbps/LTDB

-> *Demonstrator : 2 LTDB installed*



Digital on mother board



Analog on mother board

LTDB boards (490x410mm)

Demonstrator LDPB : ABBA

- **ATCA board : 3 ALTERA FPGA StratixIV**
- **Receives up to 320 Super Cell signals (SC) from one LTDB**
40 optical receiver links @ 4.8Gbps
- **Stores Super Cells into circular buffer**
Latency up to 2.5us
- **Waits for TTC trigger to readout Super Cells**
L1A, Trigger Type
- **Readout through 10GbE Ethernet network**
Readout with ATCA fabric interface
IPBus requests

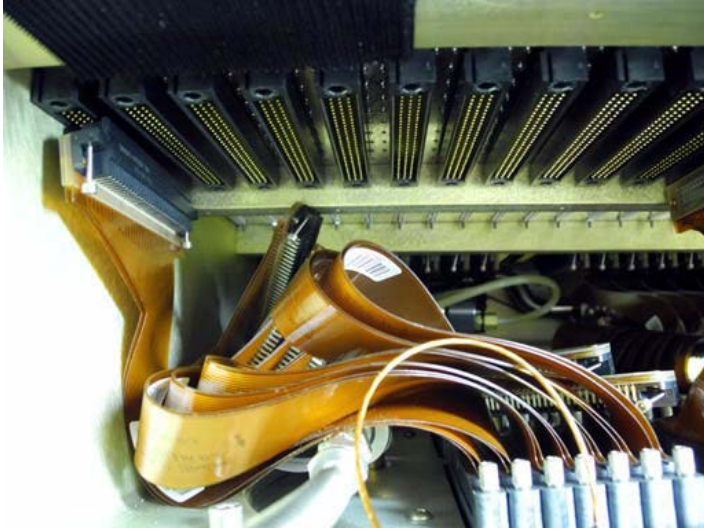
-> **Demonstrator : 2 ABBA installed**



ABBA board
280x320mm, 16 layers

Used like an oscilloscope triggered by TTC

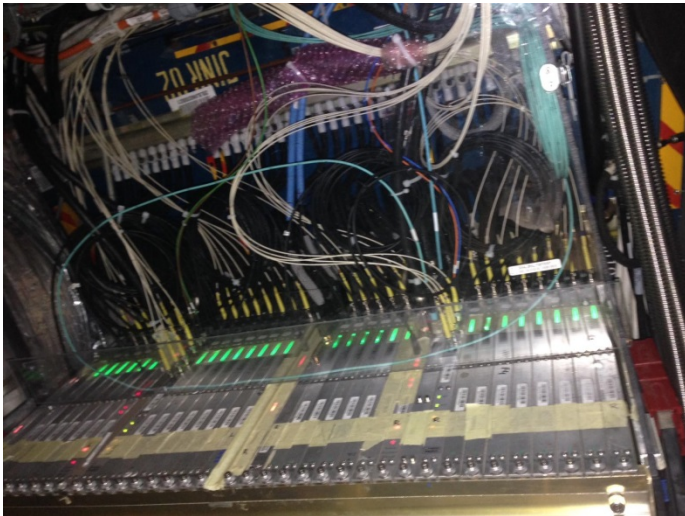
Installation – LTDB in UX15 (EM barrel I06 crate)



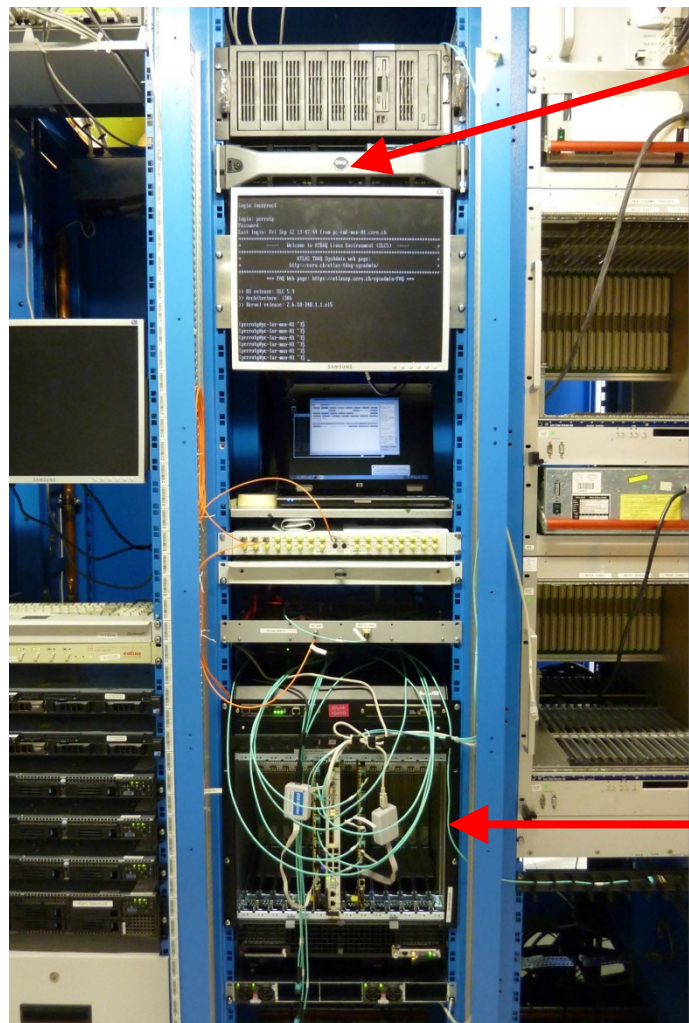
Uncabling old backplane



Plugging warm cables into new backplane



Installation – LDPB in ATLAS counting room (USA15)



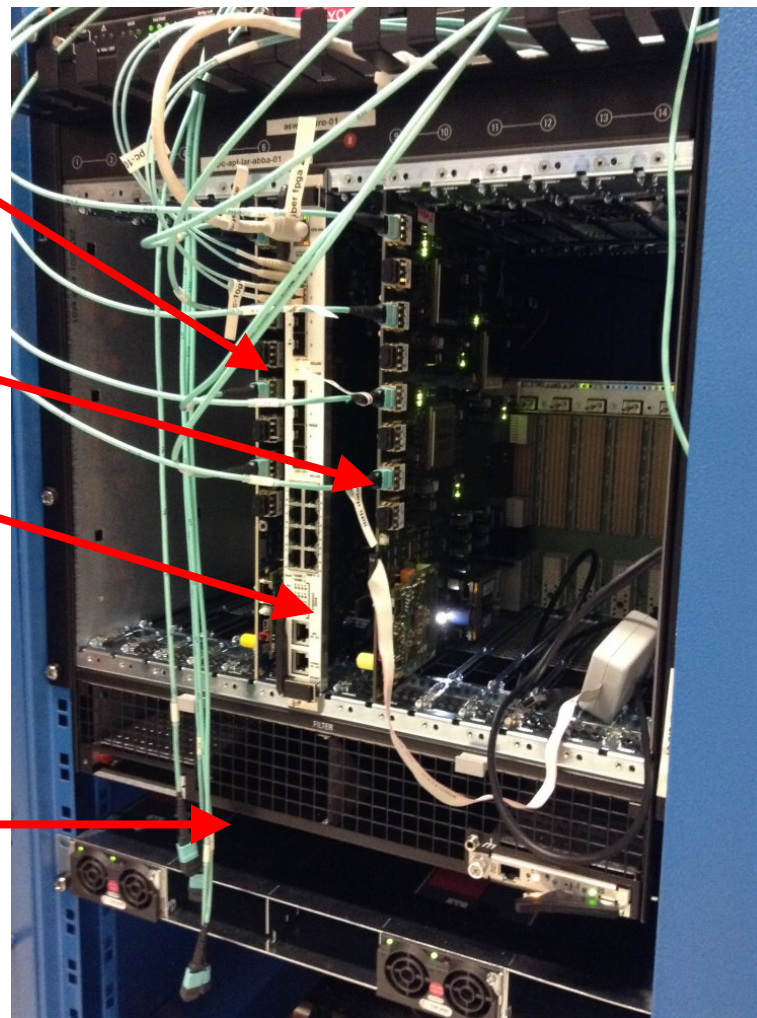
Readout PC
10GbE

ABBA board n°1
(BNL LTDB)

ABBA board n°2
(LAL/CEA LTDB)

Switch 10GbE

ATCA crate



FPGA firmware / Software

- **FPGA firmware :**

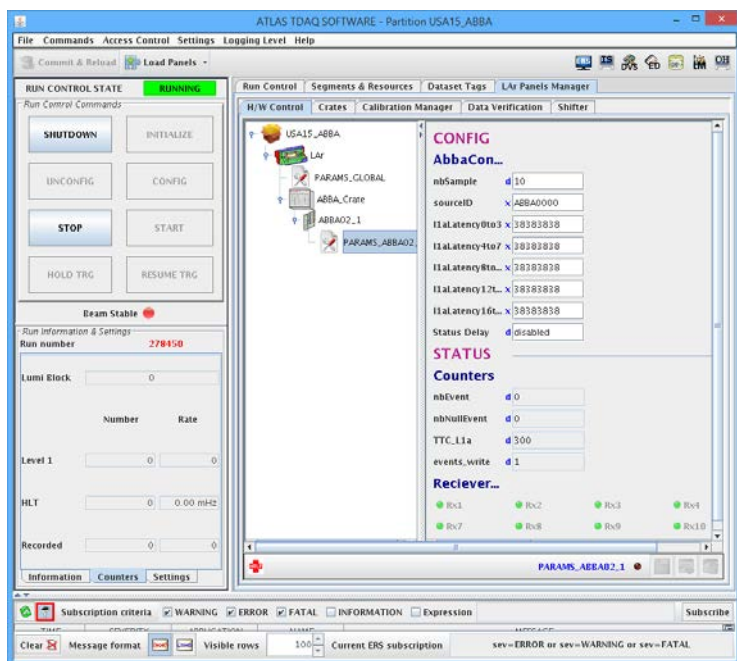
Git repository

JIRA (tasks tracking system)

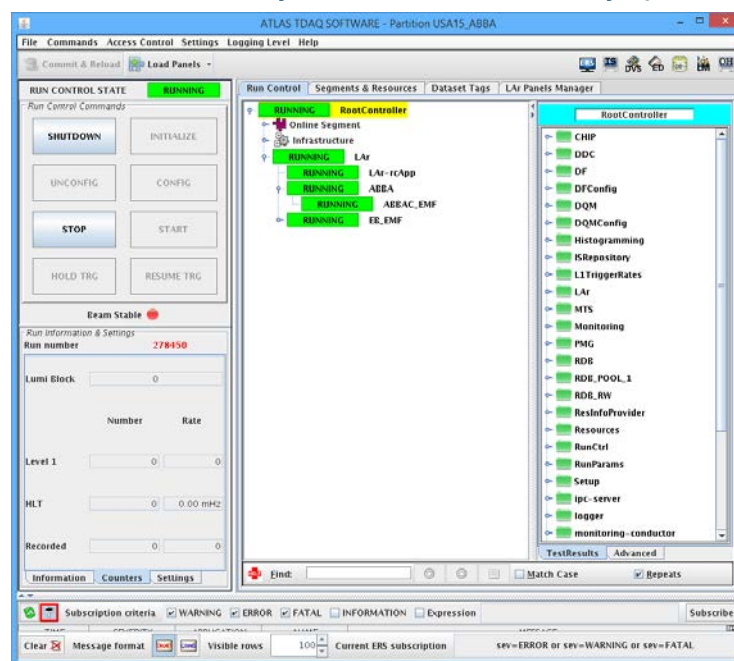
- **Acquisition software : Trigger and Data AcQuisition system (TDAQ)**

Several PCs are used to configure and readout the ABBA boards using TDAQ

Data are retrieved from the ABBA boards in an asynchronous way (IPBus)



TDAQ configuration

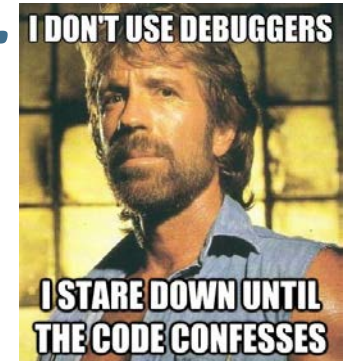


TDAQ data readout

Debugging / Acquisition / Analysis /

Hardware+Firmware+Software debugging

-> A lot of (long) work



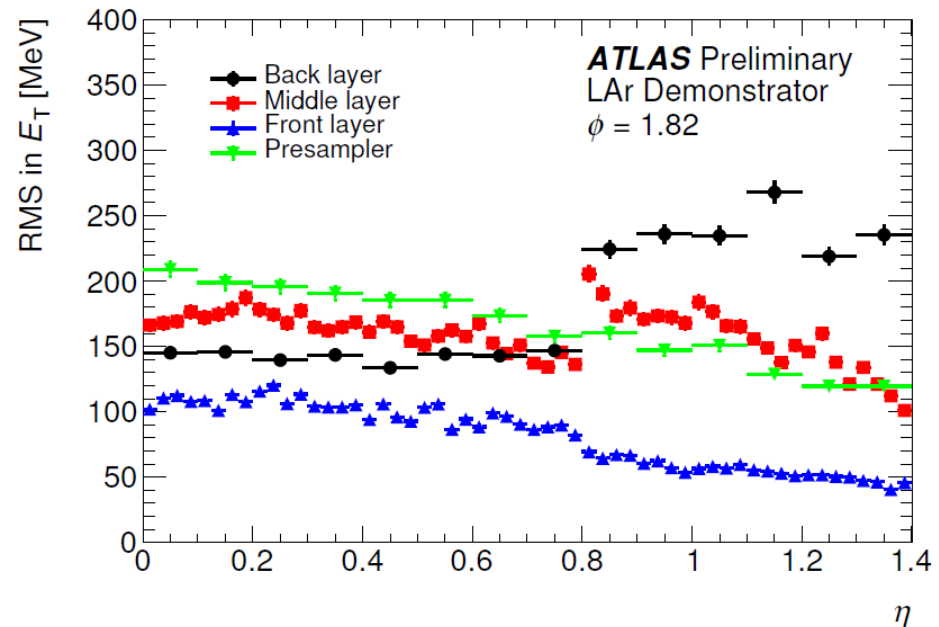
www.phdcomics.com

Results : Noise

- Noise = RMS of ADC pedestal
- Readout through the complete DAQ chain
FEB -> LTDB -> ABBA -> TDAQ software
- Results

Stable for Front Layer in η

The jump seen at $\eta=0.8$ reflects the change of absorber thickness, electrodes and calibration resistors



Results : Linearity

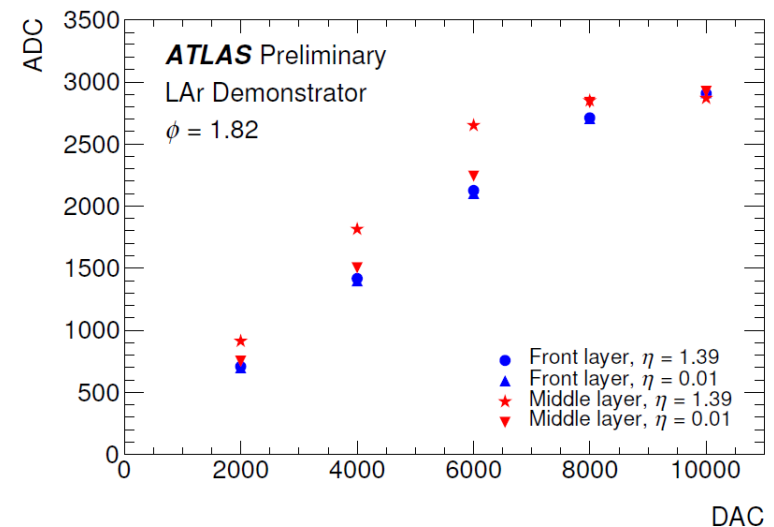
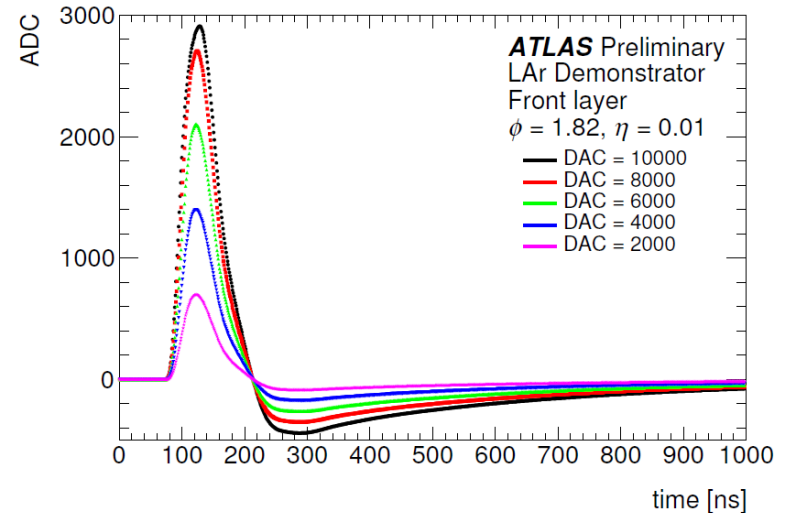
- **Pulse sent through Calibration board**
Scan the DAC values
- **Readout through the complete DAQ chain**
FEB -> LTDB -> ABBA -> TDAQ soft
- **Results**

Linearity=f(DAC)

Saturation of analog part ~ 10000

Expected behavior from LSB

-> *an η -dependent quantization is discussed to not saturate the ADC*



Summary

- ***A part of the new Trigger scheme (Demonstrator) has been installed***

Both Front End and Back end electronics have been validated

-> One Front End Crate (1/32) is equipped for the demonstrator

Readout through TDAQ software

- ***Measures have been done with this new Trigger chain***

Does not affect the current system : no additional noise

Does not disturb the current readout system : works in parallel

Pulses shapes have been checked with Calibration runs

- ***Plans***

Tests are still on going to capture real p-p collisions

-> Need to adjust trigger selection through TTC

-> TTYPE for our specific calorimeter region

Data will be used to adjust Filter algorithm coefficients