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Performance of the Demonstrator System for the Phase-I Trigger Readout Electronics Upgrade of the ATLAS Liquid-Argon Calorimeters

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For the Phase-I luminosity upgrade of the LHC, a higher granularity trigger readout of the ATLAS LAr Calorimeters is foreseen in order to enhance the trigger feature extraction and background rejection. The new readout system digitizes the detector signals, grouped into 34000 so-called Super Cells, with 12 bit precision at 40 MHz and transfers the data on optical links to the digital processing system, which extracts the Super Cell energies. A demonstrator version of the complete system has now been installed and operated on the ATLAS detector. Results from the commissioning and performance measurements will be reported.

Summary

The Large Hadron Collider is foreseen to be upgraded during the shut-down period of 2018/19 to deliver about 3 times the instantaneous design luminosity. Since the ATLAS trigger system will not allow an increase of the trigger rate an improvement of the trigger system is required in order to avoid raising the transverse momentum thresholds for physics objects. The ATLAS LAr Calorimeter read-out will therefore be modified and trigger signals with a higher spatial granularity will be provided to the trigger. New trigger signals will be arranged in 34000 Super Cells which achieves a 5-10 times better granularity than the current trigger towers. Information from different calorimeter layers and a finer segmentation in pseudorapidity will allow better feature extraction and background suppression. The efficiency for electrons, photons, tau leptons in the low transverse momentum range can be kept at the current values, while background from hadronic jets is suppressed, keeping the trigger rates in the required range.

The Super-Cell read-out is composed of custom developed 12-bit SAR ADCs in 130nm CMOS technology to be installed on-detector in a radiation environment and digitizes the detector pulses at 40MHz. The data will be transmitted to the back-end using a custom serializer and optical converter applying 5.44Gb/s optical links. These components are installed on 124 LAr Trigger Driver Boards (LTDB) each handling up to 320 Super-Cell channels. Two prototype versions of the LTDB using commercial TI ADS5272 ADCs are already installed on the ATLAS detector in a demonstrator system. This system is operated in parallel to regular ATLAS data taking in the LHC Run-2.

The back-end system will receive data at a total rate of 25Tb/s. LAr Digital Processing Boards (LTDBs) equipped with 4 Arria-10 FPGAs are foreseen to perform digital signal processing for precise energy reconstruction, pile-up suppression and identification of the correct bunch crossing time. Each of the 32 LTDBs handles about 1100 Super-Cells on average. Currently, two prototype LTDBs implementing Stratix V FPGAs are part of the demonstrator system.

The demonstrator set-up is completed and one Front-End Crate (FEC) covering a region of $\Delta\eta \times \Delta\phi = 1.4 \times 0.4$ of one LAr half-barrel is equipped with prototype components. The demonstrator system provides the full functionality of the future LAr Phase-I trigger system. It is composed of a new FEC baseplane, new Layer Sum Boards (LSB) mounted on the existing Front-End Boards (FEB), prototype LTDBs, additional signal fibers, and prototype LDPBs.

The talk will give an overview of the Phase-I Upgrade of the ATLAS LAr Calorimeter readout and of the custom developed hardware. Performance results from the prototype boards in the demonstrator system will

be reported. First measurements of noise per channel, correlated noise and system linearity will be presented. Furthermore, using the detector calibration system, the dynamic range of the system is explored and saturation effects in analog and digital part are analysed and compared with simulations.

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