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FATALIC: A dedicated Front-End ASIC for the Atlas TileCal Upgrade

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A front-end ASIC (FATALIC) has been developed to fulfil the requirements of the Phase 2 upgrade of the ATLAS Tile Calorimeter. This electronics performs the complete processing of the signal delivered by each PM tube. The first stage is a current conveyor which splits the 17bit dynamic range of the input signal into three ranges. Each channel is followed by a shaper and a dedicated pipeline 12bit ADC operating at 40MHz. The chip is developed using a 130nm CMOS technology.
Measurements show a linearity better than 0.5% for low energy particles, and an ENC limited to 10 fC.

Summary

FATALIC, standing for Front-end ATlAs tiLe Integrated Circuit, is a front-end ASIC developed to fulfil the requirements of the Tile Calorimeter (TileCal) of the ATLAS experiment which has to be upgraded to comply with the High Luminosity programme planned for LHC around 2024. This upgrade is mainly motivated by the ageing of the components, a better radiation tolerance, an improvement of the reliability correlated with a simplification of the system and an increase of the precision on a wider dynamic range. It is why the integration of the front-end electronics into an ASIC has to be considered.
FATALIC has been designed to perform the complete processing of the signal delivered by each PM-Tube. This signal exhibits a large dynamic range up to 1200 pC for the highest expected energy particles. The current of the PMT flows to the input stage of FATALIC based on a current-conveyor which splits the high dynamic range at these outputs into three ranges (high, medium and low-gain channels). Each channel is followed by an integrator which performs a current-to-voltage conversion and a shaping with a 25-ns peaking time. Lastly, a 12-bit pipeline ADC operating at 40 MHz performs the digitization of each gain-channel. The data of two gain-channels are delivered on a single 12-bit bus: the data of the medium gain-channel is always transmitted on the first 40 MHz clock edge, whereas on second clock edge the data of the low-gain or of the high-gain channel are delivered. The selection of the relevant output data is digitally performed inside the chip depending of the saturation from the most sensitive channel.

The FATALIC chip has been developed with a full differential architecture using the IBM 130nm CMOS technology, taking advantage of its mixed-signal properties. For test purposes, each of the 40 prototype circuits has been packaged in a TQFP64 package and wired on a new front-end board, named “all-in-one”. First results of the measurements show a linearity better than 0.5% for the low energy particles (up to 14 pC), and of about 1% for the upper part of the dynamic range (up to 1200 pC). The noise requirement is fulfilled with an intrinsic noise of the electronics measured through the digitization path, expressed in terms of equivalent input charge, limited to 10 fC rms at pedestal. The power consumption of the complete “all-in-one”board is limited to 200 mW.

A test beam campaign will start on October 2015 to fully evaluate the performance of the upgraded read-out electronics based on the FATALIC ASIC and the performance of two others options proposed by the collaboration.

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