A radiation tolerant Data link board for the ATLAS Tile Cal upgrade

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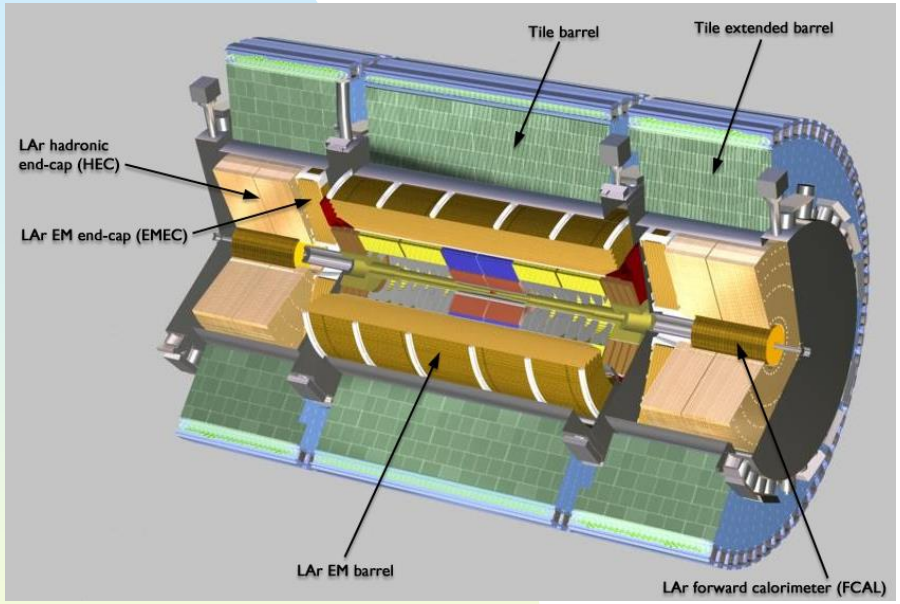
On behalf of the ATLAS Tile Calorimeter System

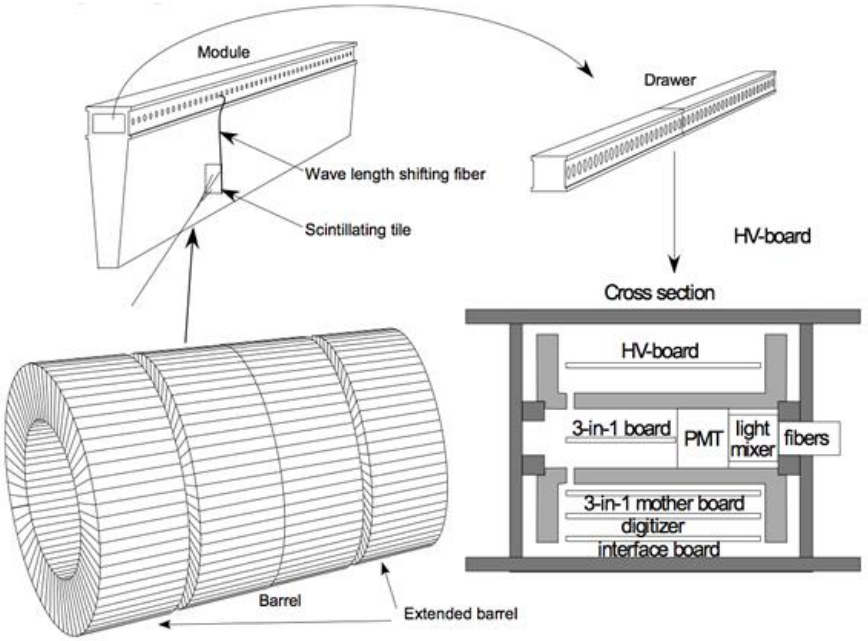
Outline

ATLAS TileCal
Upgrade aims
Overview of the Phase II upgrade
The Data link board
The Upgrade Demonstrator

ATLAS TileCal



256 wedge shape modules around LAr



On-detector electronics in extractable drawers

Phase-II Upgrade Aims

The Phase-II ATLAS upgrade will probably take place from 2023 to 2025

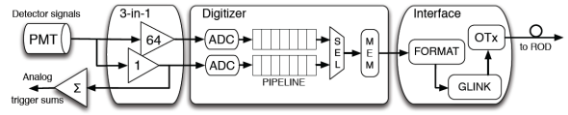
- End of life for present system
- Components obsolete – State-of-the-art components require new hardware solutions
- Increased luminosity → Need more efficient trigger algorithms →
- Make all information available to the trigger and with minimum latency
    - Transfer all data to control room
    - Fully digital trigger using tower sums derived from DAQ data
    - Adapt to Level 0/1 scheme
- Increase reliability – Redundancy and radiation tolerant solutions
- Smaller modules – to reduce consequences of failures
- MiniDrawers – Smaller drawers easier to maintain (replace) in radiation environment
- Flexibility - Programmable logic

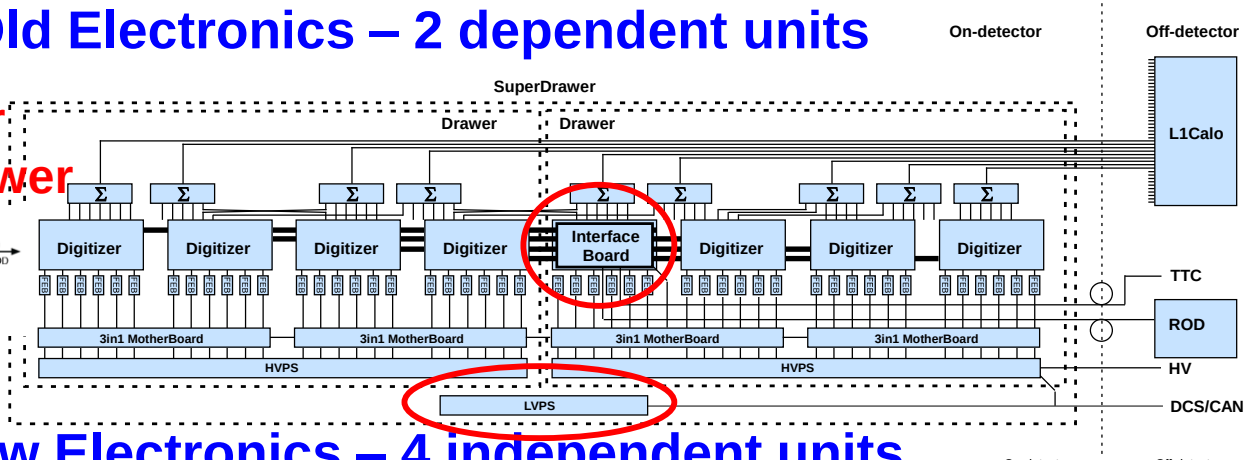
All on- and off-detector electronics will be replaced - only the PMTs remain

Overview of the Phase-II upgrade

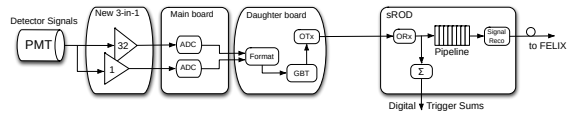
Old Electronics – 2 dependent units

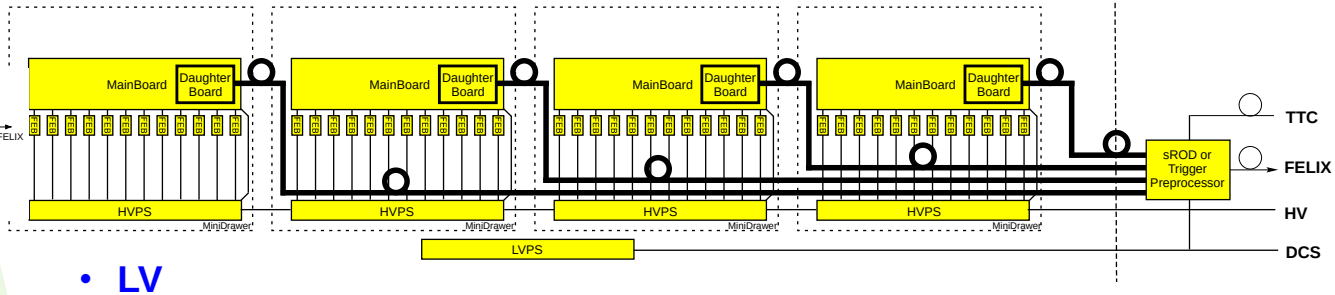
SPOFs for entire drawer





New Electronics – 4 independent units

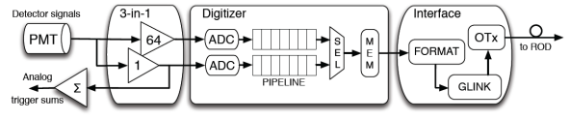


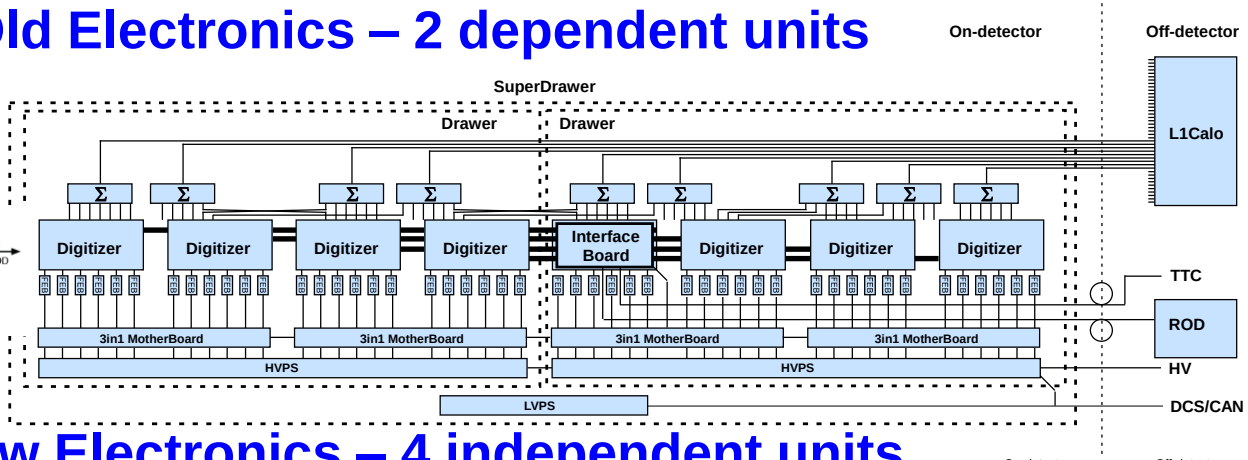


- LV
  - New Front-End Boards – 3 versions
  - Main Boards – adapted to each FEB type
  - Daughter Boards - FPGA radiation tolerance
  - New links
  - New redundant 3 stage LVPS (200V→10V→5,-5,3.3,1.2,1V)
- HV
  - New HVPS - 2 versions
  - Active Dividers
- New pre-processors

Overview of the Phase-II upgrade

Old Electronics – 2 dependent units





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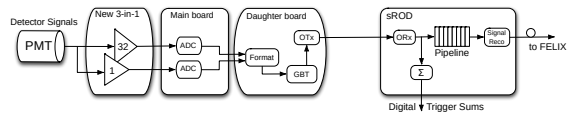
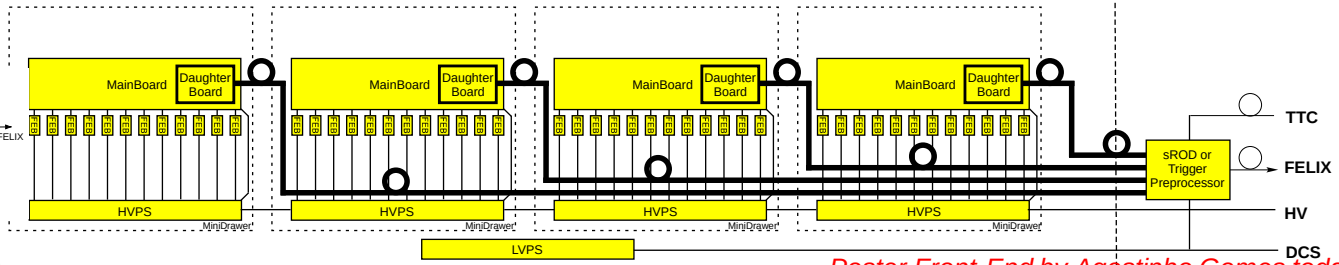
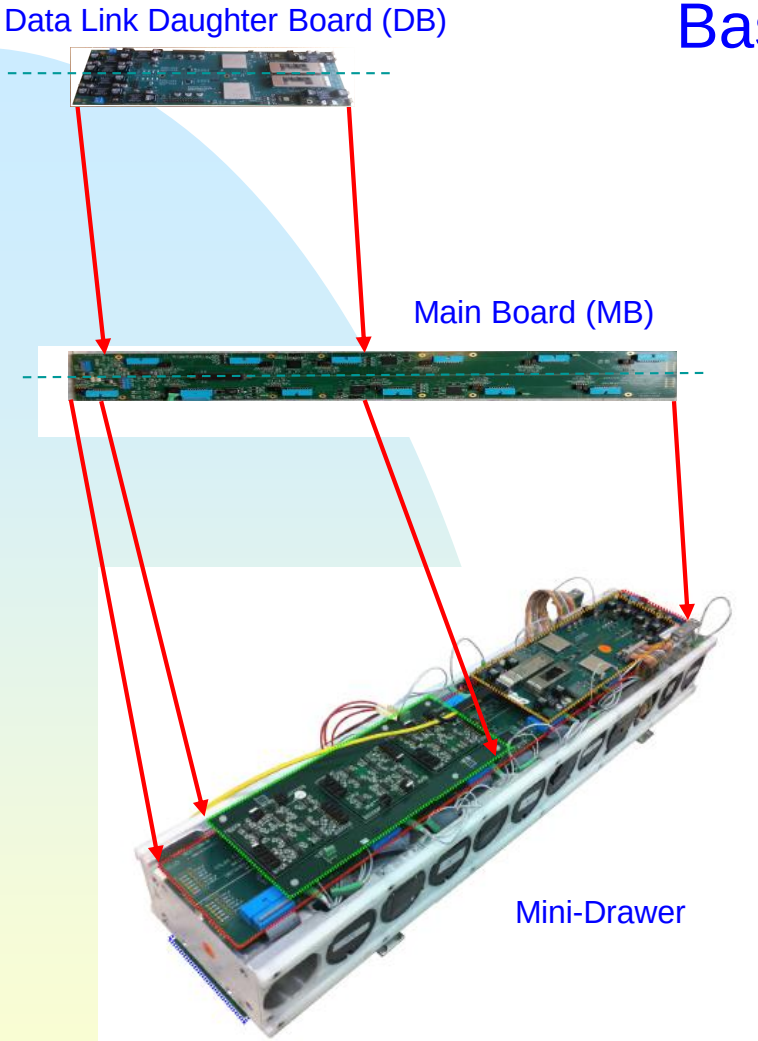




- **LV**
  - **New Front-End Boards – 3 versions** *Poster Front-End by Agostinho Gomes today*
  - **Main Boards – adapted to each FEB type** *Poster QIE12 by Gary Drake today*
  - **Daughter Boards - FPGA radiation tolerance** *Oral FATALIC by Laurent Royer Thursday*
  - **New links**
  - **New redundant 3 stage LVPS (200V→10V→5,-5,3.3,1.2,1V)**
- **HV**
  - **New HVPS - 2 versions** *Poster HVPS by Francois Vazeille Wednesday*
  - **Active Dividers**
- **New pre-processors** *Poster sROD by Fernando Carrio today*

The Data Link Board

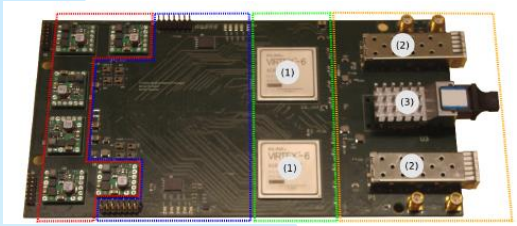
Basic redundancy



- All on-detector boards divide symmetrically around the center line
- The two halves are largely independent
- All calorimeter cells are independently read out by right side and left side electronics
- Even if one side of a board fails the affected cells will still be read out by opposite side

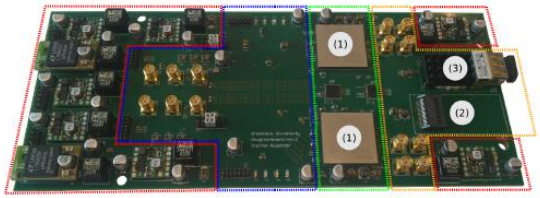
Link Board history

Version 1



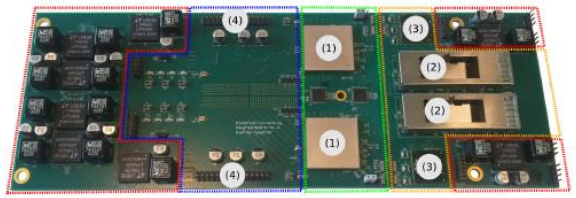
2 Virtex 6 + 2 SFP + 1 PPOD

Version 2



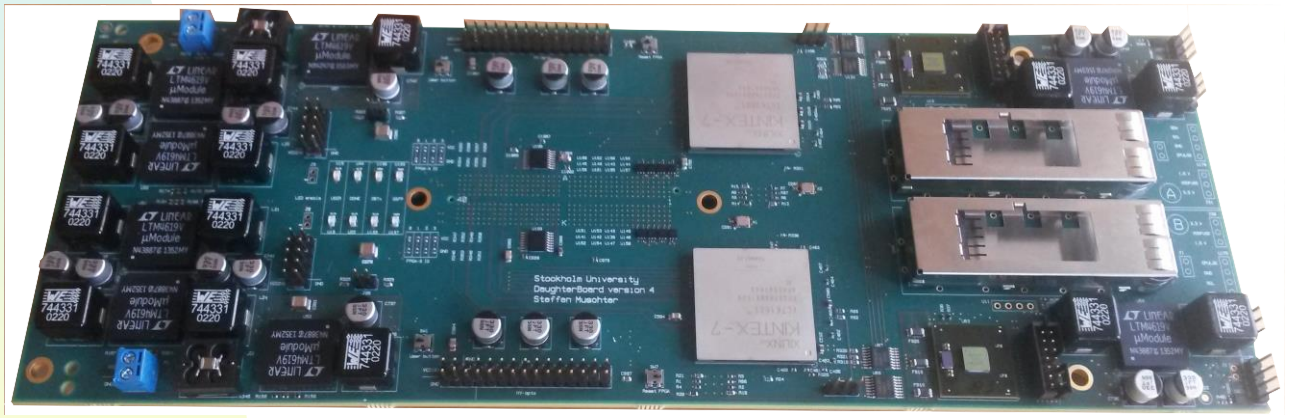
2 Kintex-7 + QSFP+ + 1 PPOD

Version 3



2 Kintex 7 + 2 QSFP+ + 2 GBTx

Version 4

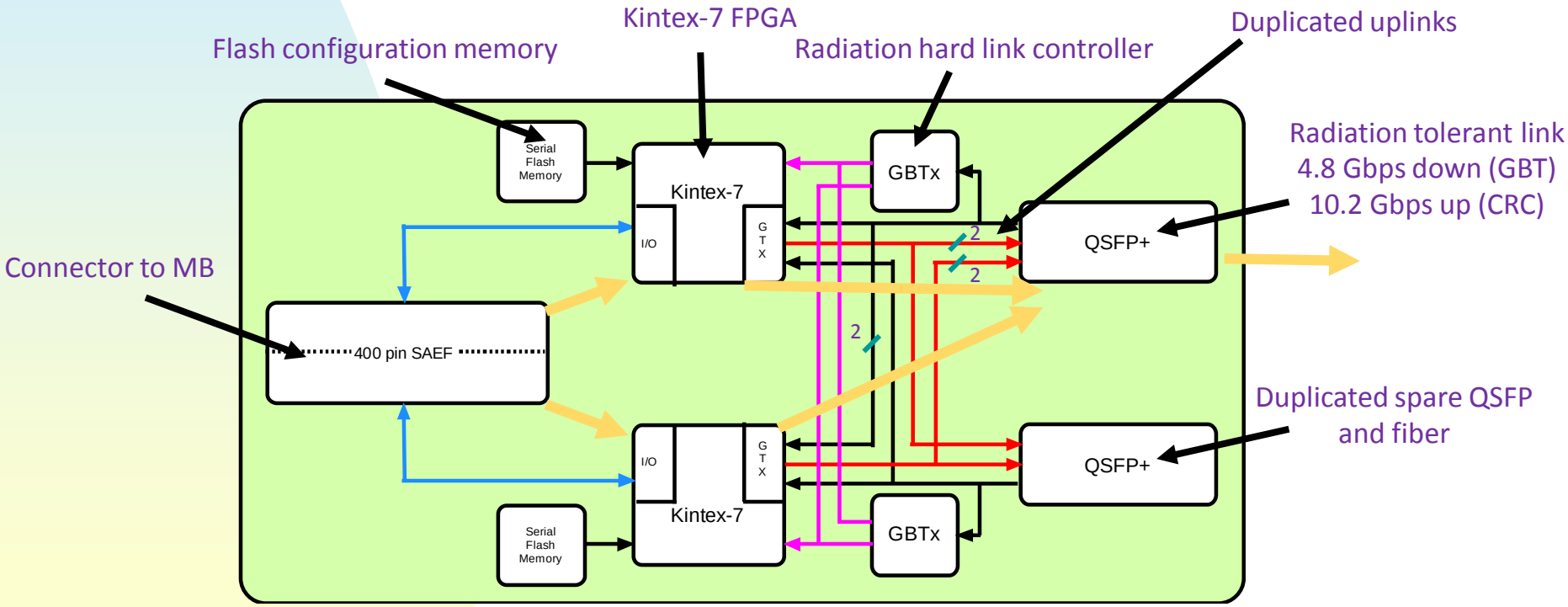


Same as v3, but modified to be able to serve main boards for different FE options

Daughter Board and links

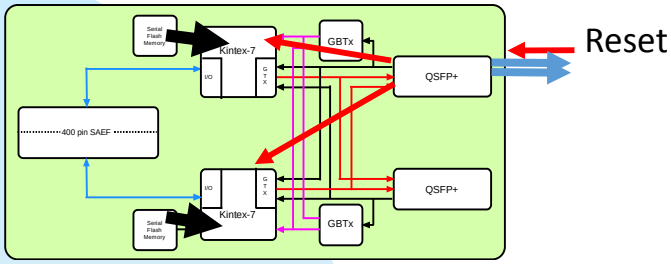
Clock, trigger and Control via GBT protocol
System clocks and FPGA configuration via radiation tolerant GBTx chips
4 times redundant high speed transmission (8 if board symmetry is included)
2 independent QSFP+ to be switched manually in USA-15 patch panel

QSFP+ modulator based radiation tolerant link:
BER around 10^{-18}
4x10 Gbps



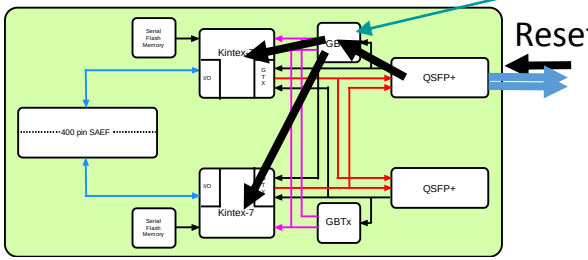
Error mitigation strategies

DB configure from flash after reset

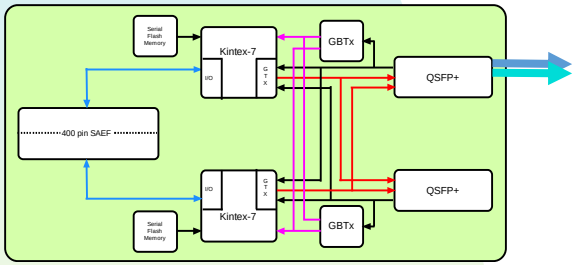


Remote Configuration via GBTx

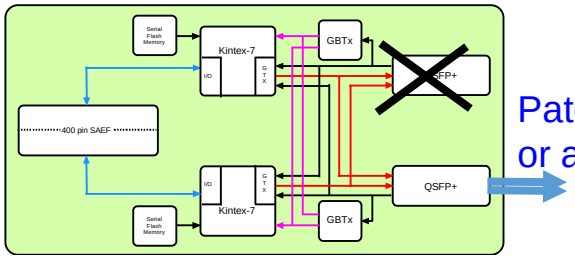
Rely on the radiation hardness of GBTx



Use link redundancy + CRC for transient Link failures

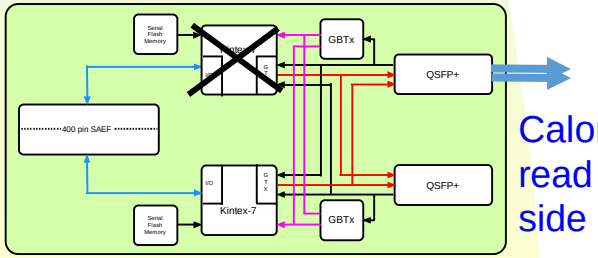


Switch QSFP after permanent link failure



Patch panel reconnect or automatic switch

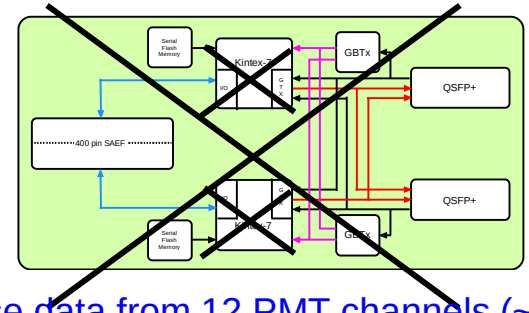
FPGA failure



Calorimeter cell only read out from one side

Precision loss but no loss of data

Loss of both FPGAs or both links



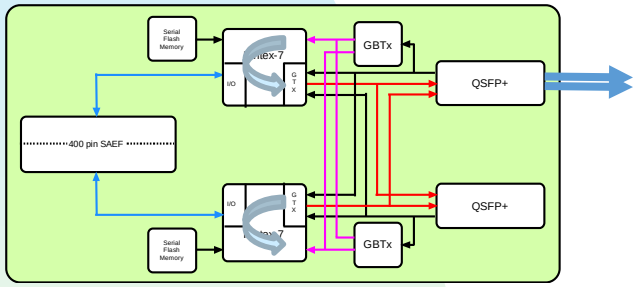
We lose data from 12 PMT channels (~0.1 %)

FPGA error mitigation

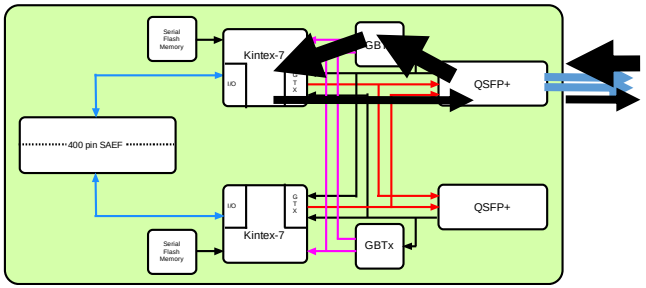
Use Triple Redundancy mode

TMR + fast recovery -> greatly reduced failure rate

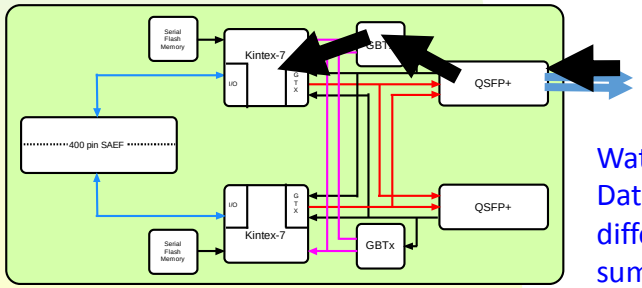
Scrubbing of configuration memory



Partial re-configuration

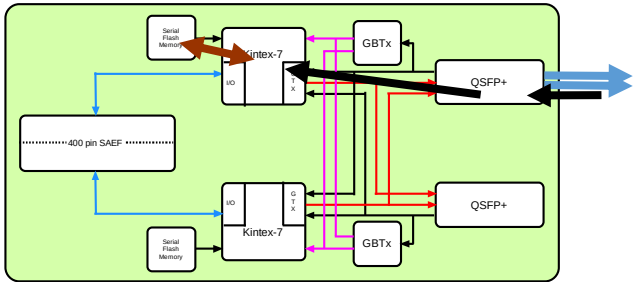


Watch dog activated full re-configuration

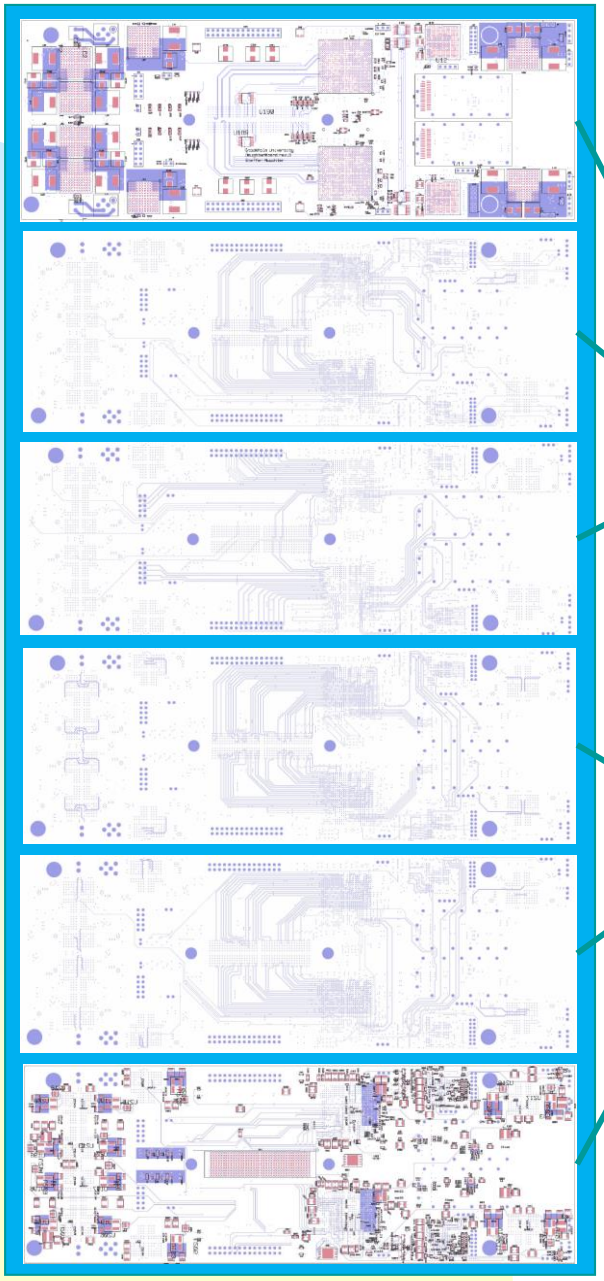


Watch dog function: Data corruption or differences in check sums calculated on ADC data and data delivered off detector

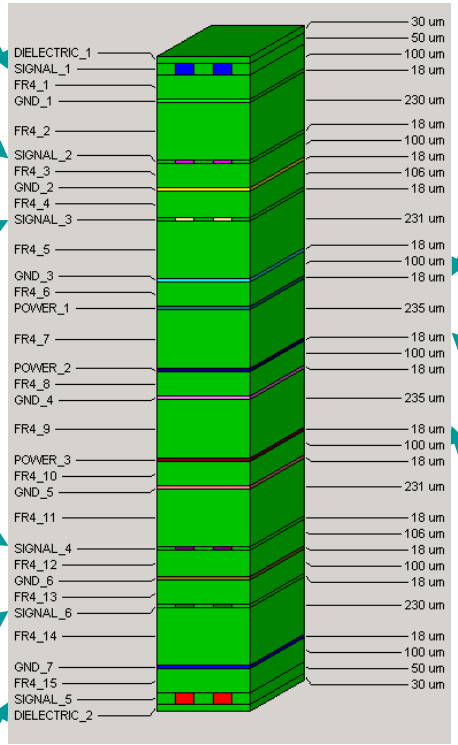
Continuous supervision and rewrite of Flash memory

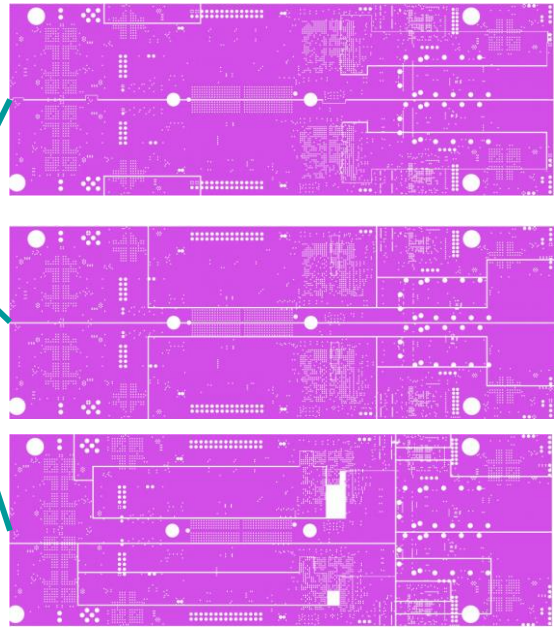


PCB



16 layer PCB
All signal layers adjacent to ground planes on both sides
High speed signals in middle layers





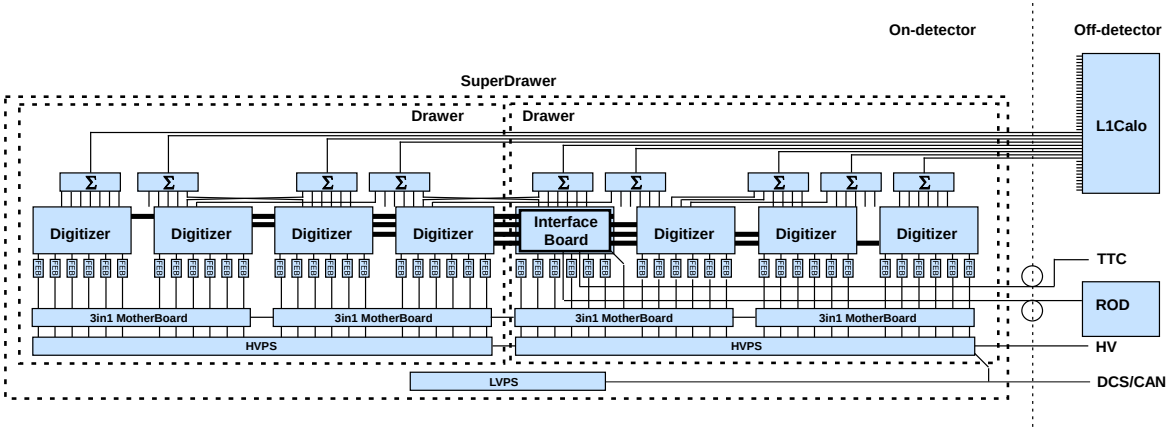
POL DC-DC converters eliminate problems with power drop
Power filtered to reduce noise especially for TCX supply
Much effort to allocate related signals to proper banks

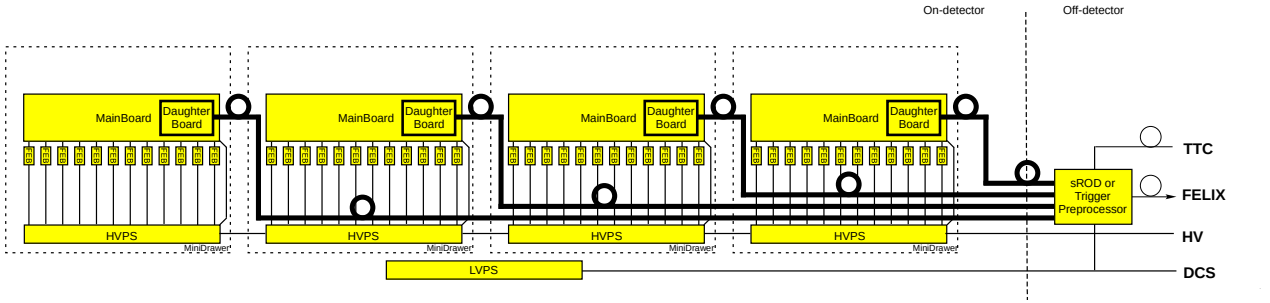
TileCal Phase-II Demonstrator

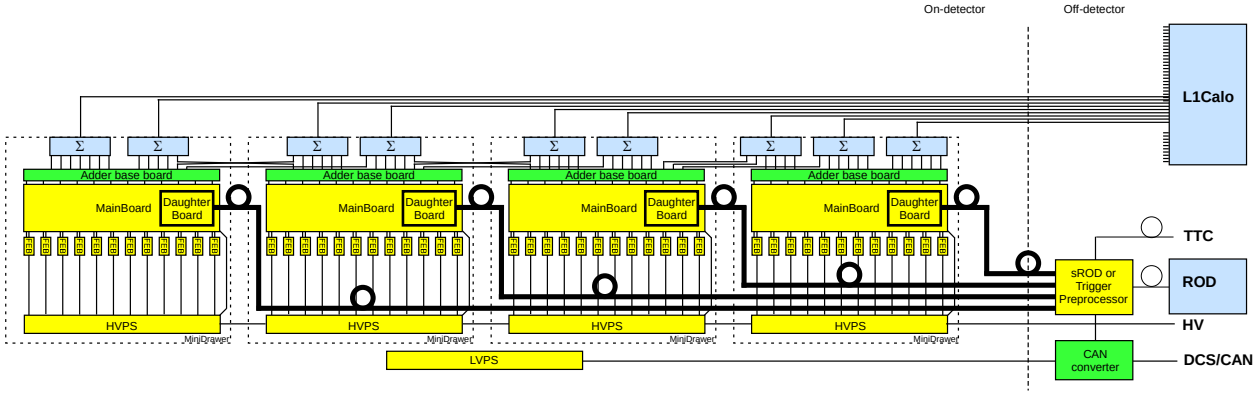
Old electronics

New electronics

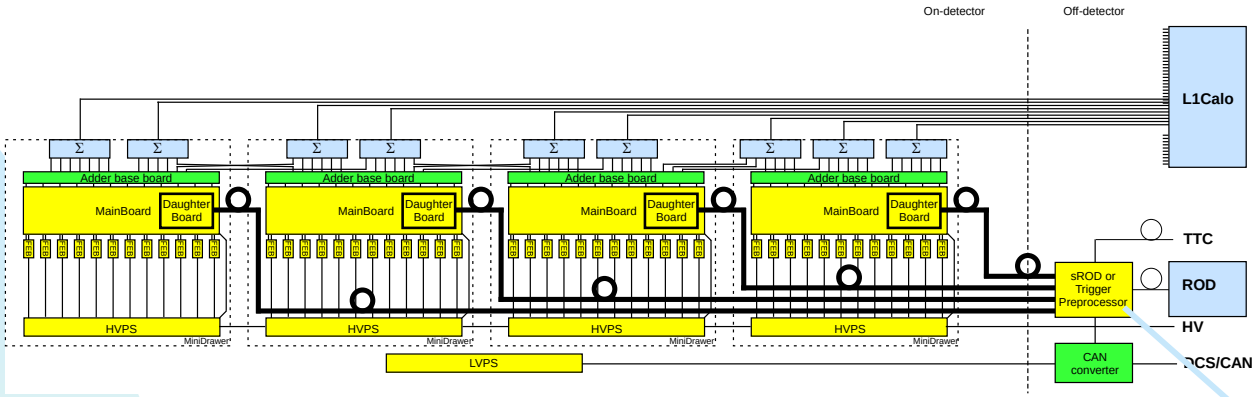
Hybrid electronics to be deployed as a demonstrator of upgrade electronics inside TileCal during Phase 0 (LS1)
Must be compatible with present electronics
Aimed to test phase-II electronics under sharp conditions







Use of Demonstrator data



A number of demonstrator units (with v3 DBs).
used in test benches and in upcoming test beam studies
will be upgraded with v4 DBs (depending on GBTx availability)

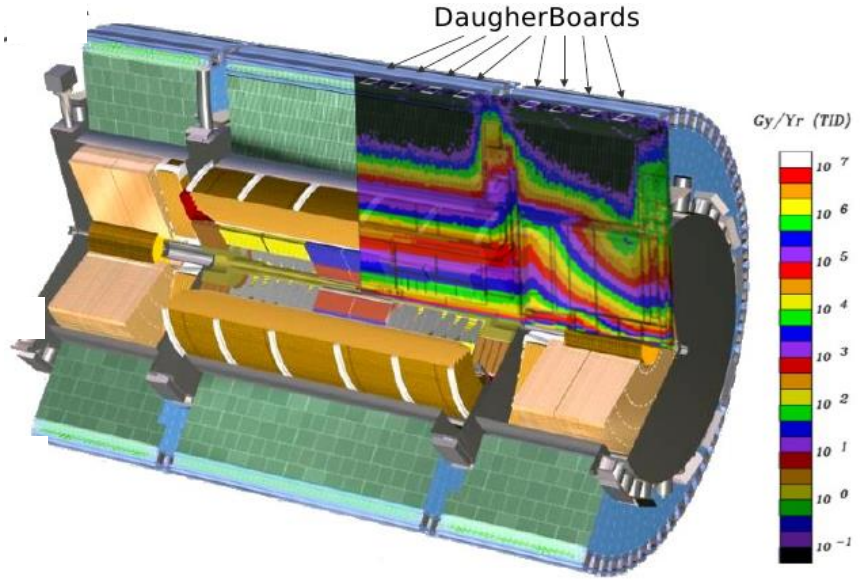
DAQ and DCS software developed
Equivalence to present system have been demonstrated

Data from the demonstrator can be used for:
Study of L0 and L1 trigger algorithms
Study of L0-trigger architectures
Study of ROD architectures (Preprocessor {=sROD} and FELIX {ROD switch})
Study of DCS architectures
etc.

This will require sharing data with LAr and L1Calo demonstrators

Radiation levels

TID: < .2 Gy/year
<10^{10} p/cm^2/year



- Experience shows that permanent FPGA errors are scarce, SEU are the ones to worry about
- 3 single bit SEU errors per day expected and one double bit error per three days (tile level is about 1/10 of that of LAr)
- A preliminary radiation test at MGH in Boston gave an estimated 10 SEU:s per day.
- There are basically four different types of SEU induced errors that will influence operation differently
  - Errors in TMR protected part of configuration memory
  - Errors in not protected part of configuration memory
  - Errors in TMR or CRC protected FPGA fabric
  - Errors in not TMR or CRC protected FPGA fabric
- New radiation studies are planned with v4

SEU error mitigation

Single bit SEU errors are mitigated by scrubbing which removes the error in ~30ms. Here TMR helps

but if two SEUs in the two of the three TMR modules happen within 30 ms TMR does not protect

The probability for this is

2000 FPGAs in system

$$\frac{rate^2 \cdot t_{coinc} \cdot n_{FPGA} \cdot year}{n_{\mathrm{mod}/FPGA}} \varepsilon = \frac{3^2 \cdot 0.03 \cdot 2000 \cdot 365 \cdot 2}{24 \cdot 3600 \cdot 3} \varepsilon = \frac{3.65 \cdot 10^4}{2 \cdot 0.4 \cdot 3 \cdot 10^3} \varepsilon \approx 14 \cdot \varepsilon$$

Size of ECC config mem

<< 1, the fraction of TMR protected circuits times the fraction of errors in this area that affect function

Double bit errors in TMR protected areas take longer to fix, in the worst case full reconfiguration, about 10s

$$\frac{rate^2 \cdot t_{coinc} \cdot n_{FPGA} \cdot year}{n_{\mathrm{mod}/FPGA}} \varepsilon_1 = \frac{10 \cdot 2000 \cdot 365}{3^2 \cdot 24 \cdot 3600} \varepsilon_1 = \frac{3.65 \cdot 10^6}{1.08 \cdot 0.36 \cdot 10^5} \varepsilon_1 \approx 10^2 \varepsilon_1$$

- CRC protects the output part including transceivers and links, reduced in the same way as TMR protection.
- A small part of the system can not be protected by TMR or CRC. Does not benefit from coincidence reduction but the area can be made very small.

$$rate \cdot n_{FPGA} \cdot year \cdot \varepsilon_2 = 10 \cdot 2000 \cdot 365 \cdot \varepsilon_2 \approx .73 \cdot 10^7 \varepsilon_2$$

<<< 1, the fraction of not TMR protected circuits times the fraction of errors in this area that affect function

- Errors in the FPGA fabric in TMR or CRC protected areas are protected as in the configuration memory.
- Those outside this area can not be detected, but can be minimized and will only remain for one clock cycle

The effect of the errors on detector operation depend on their duration

Conclusions

One of the largest concerns has been to achieve sufficient reliability
which we have reached by spending band width by duplication (4 or 8 times)
A reasonable strategy considering the cost.

The estimated rate of SEU errors in TMR or CRC protected parts is small
Double bit errors more problem but OK
However, the small part that cannot be covered by TMR or CRC is a concern and must be minimized

Due to the board redundancy the calorimeter cell will still be read out even if errors block a FPGA path
Transient errors in both FPGAs very unlikely, unless both are hit with same particle

4 generations of link daughter boards have been designed to study evolving design criteria.
Even though the last design has included all concern raised so far, extensive tests will still be made

There is still work to do!

Acknowledgements

The Stockholm group has been sole responsible for the hardware design.
Actually, it formed the basis for the main designer Steffen Muschter's thesis

The firmware, however, involved more groups such as Stockholm, Valencia, Chicago and CERN

The software development was mainly done by CERN, Chicago and Stockholm.

Testing in the TileCal test facility at CERN and later at the test beam involves and will continue to involve the entire TileCal upgrade community