POWER DISTRIBUTION FOR THE ATLAS LAR TRIGGER DIGITIZER BOARD

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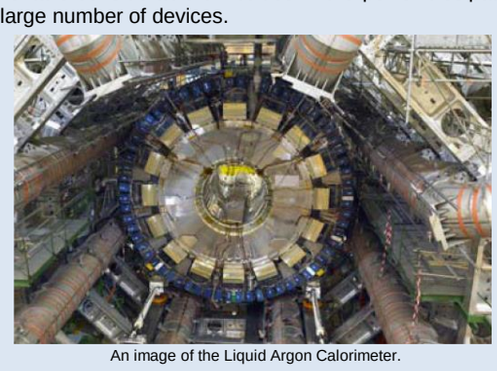
ON BEHALF OF THE ATLAS LIQUID ARGON CALORIMETER GROUP

The research activity for the design of the power distribution section of the ATLAS LAr Trigger Digitizer Board board (LTDB) will be presented. Many aspects concerning the radiation hardness and the ability to operate Point-of-load converters even in presence of high magnetic fields will be covered. Devices designed by CERN have been used and their capability for implementation on the ATLAS LTDB has been exploited with the aim to have a power distribution section with the required performances.

1. Introduction

A Liquid-argon Trigger Digitizer Board (LTDB) is being developed for the Phase-I trigger upgrade of the ATLAS Liquid Argon Calorimeters.
Several ASICs such as GBTx, optical transmitter/receivers, level translators and custom designed ADCs, as well as multiple ARTIC FPGAs from Xilinx are mounted on the board to assure the functionalities of the LTDB. These devices require several different supply voltages and a well-specified power-up sequence. Furthermore, different analog circuits are also present on the LTDB.
The full functionality of the board requires considerable resources in terms of power distribution. For this reason a relative large area of the board is reserved to it. Moreover the LTDB has to operate in a hostile environment. Each component has to be tested for radiation and magnetic field tolerance, and special design techniques have to be applied. The most important aspects are basically those related to the reliability of the devices over time.
Supply circuits are particularly affected by hostile environment. For example, high magnetic fields can lead to malfunctions, failures and degradation of the performances of some switching power supplies. It was therefore considered useful to study these aspects carefully with the aim of being able to design power systems that can work reliably on the ATLAS detector.
We propose the use of Point of Load (PoL) developed by CERN and denoted as FEASTMP (see datasheet and [1 - 3]). This device is able to assure optimal performance in the presence of both high magnetic fields and high level of radiations. The digital components on the LTDB require voltages between 1V and 4V and up to 10W of power each. The considered PoL provides a maximum output current (4 A) and maximum deliverable power of 10W. Only for the digital part of the LTDB board 23 FEASTMPs are therefore needed. This entails considerable difficulties in the power dissipation of this large number of devices.



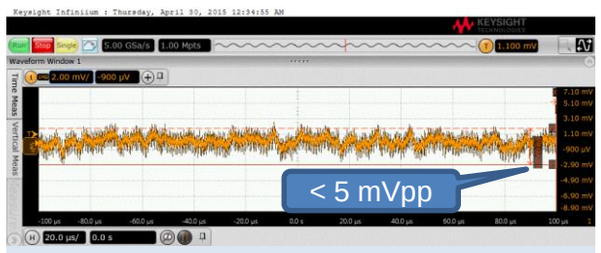
An image of the Liquid Argon Calorimeter.

In what concern the analog part of the LTDB, LDOs have been proposed but this aspect will be not covered here.
Furthermore, the LTDB needs, for some on-board devices, a supply voltage with a low level of residual ripple (less than 10 mV) which is being verified experimentally. It must be considered that the ripple may be affected by the value of the input voltage, by the value of the output voltage and, finally, by the output current.
Some preliminary tests confirm that the FEASTM can comply with these important requirements.

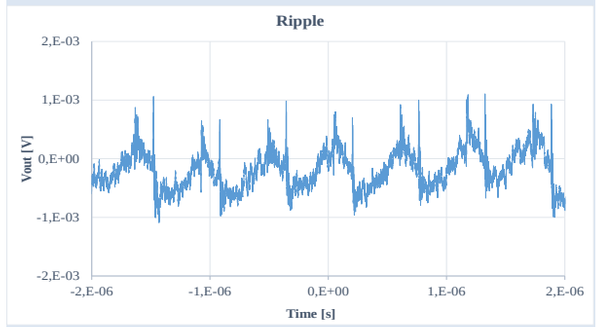
The FEASTMP @ 2.5 V output voltage (see datasheet fro dimensions)

2. FEASTMP PoL Features

- ***2.1 Ripple***: Output behavior in terms of noise is an interesting key point. Actually, the noise can be evaluated by means of the ripple in the output signal. It is important to remember that the ripple is the unwanted residual periodic variation of the output of a device which has been derived from an alternating current source. The value of the output ripple is very important in many situations. In the LTDB a ripple less than 10 mVpp is required. The ripple of the system depends also on the magnetic field strength. For the LTDB board in its environment the value will be ~ 0.6 T. In the experimental validation it is sufficient to test the device under conditions stronger than the standard. Some example of ripple measurement are reported in the following figures. Data without magnetic field are reported for different input voltage. Measurements have been obtained with conditions equal to the ones indicated by the manufacturer.
  In the present case the PoL is a DC-DC converter and it is supplied by a DC voltage source, as it will be in the final application. The ripple tends to increase along with the magnetic field but not in a significant way.
  The experimental results are perfectly in compliance with the values given by the manufacturer (see the following figures).



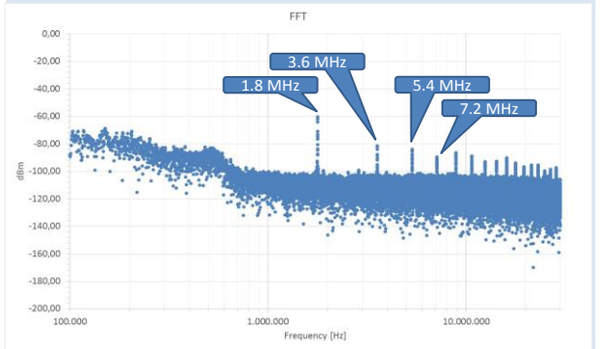
Scope configuration: Sampling Mode Real Time, Sampling rate Automatic: 20 GSa/s, Averaging: off, Interpolation: Auto, Vertical Scale: 2.00 mV/div, Coupling: AC, Bandwidth Limit: 20 MHz, Horizontal Scale: 1 µs/div.
Bandwidth limit set to 20 MHz is used in order to be in compliance with the indication of the device datasheet.



Output Ripple (Vin = 7 V, Iout = 1.67 A, Magnetic Field = 0 T).

It is important to verify the performance of this device with different input voltage because the main converter used in ATLAS – LAr (LAr Calorimeter) is designed with many different output voltages. The evaluation of the maximum output voltage ripple is very important and shown in the above figure.

- ***2.2 Noise***: Noise is also important in the considered applications. The spectrum highlights the main frequency which is used by the converter (about 1.8 MHz) and the multiple frequency as expected."



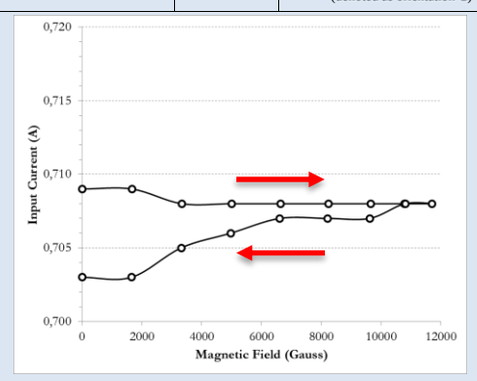
Spectrum of the FEASTMP PoL.

- ***2.3 Voltage levels***: The usableoutput voltages of the actual Main Converters (MC) are: 11V, 7V, 6V, 4V.
  - The FEASTMP PoL device, up to now, operates only with positive input voltages even if an inverting version, denoted as FEASTMN, will be available in the future.
  - The input voltage of 4 V is not suitable to be used as input for FEASTMP supply. FEASTMP are, in fact, designed for an input range 5 – 12 V.

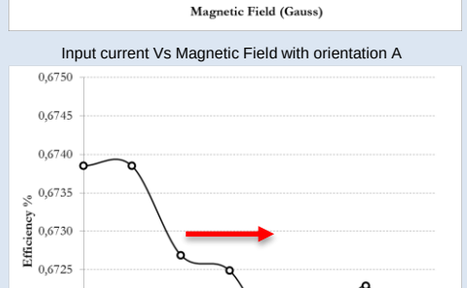
- ***2.4 Radiation Tolerance***: TID up to >200Mrad(Si), displacement damage up to $5x10^{14}n/cm^2$ (1MeV-equivalent), absence of significant SEEs up to >65MeVcm^2/mg (only short SETs smaller than 20% of the nominal Vout are observed). See ref. [1 – 3] for details.

- ***2.5 Magnetic field tolerance***: in excess of 40,000 Gauss. Experimental tests were conducted with magnetic field values typical for installed LTDB board.
  Here are reported, for example, the results obtained with Vin = 12 V, Vout = 1.8 V and Iout = 3.2 A and magnetic Field test conditions as in following Table, according to the rising and falling of the magnetic field as indicated by arrows.

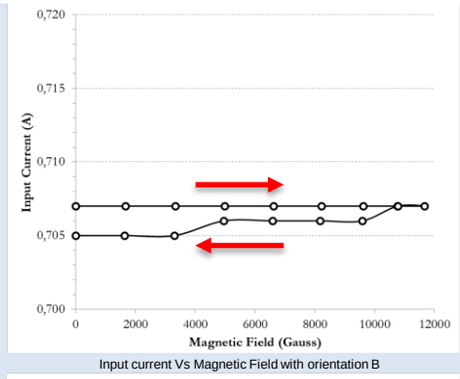
Device	*Symbol*	*Description*
	+	Perpendicular entering in the plane (denoted as orientation A)
	←	Horizontal from right to left (denoted as orientation B)
	↓	Horizontal top down (denoted as orientation C)



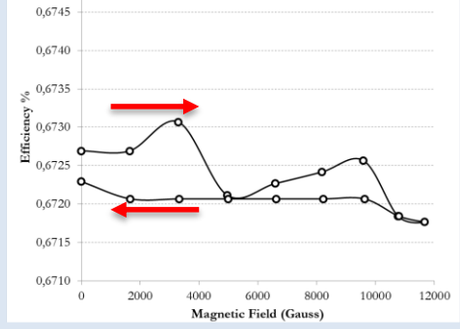
Input current Vs Magnetic Field with orientation A



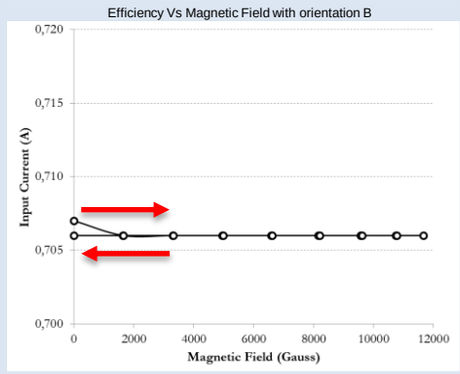
Efficiency Vs Magnetic Field with orientation A



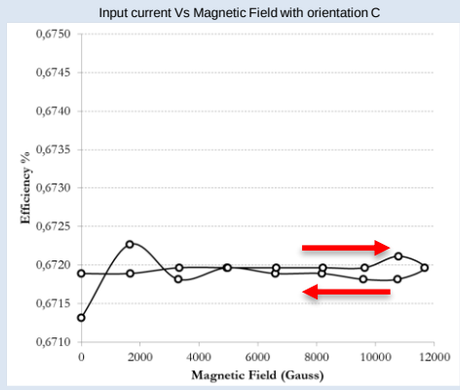
Input current Vs Magnetic Field with orientation B



Efficiency Vs Magnetic Field with orientation B



Input current Vs Magnetic Field with orientation C

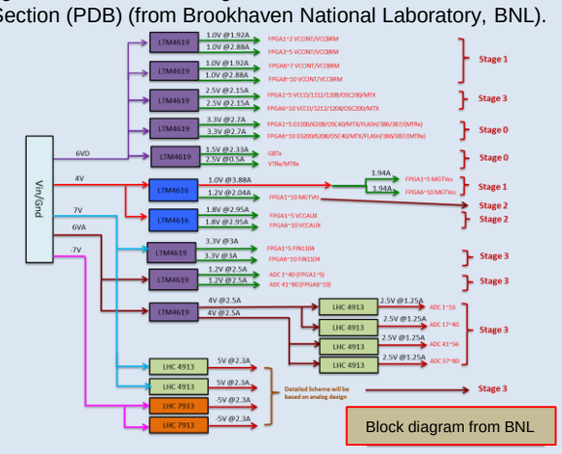


Efficiency Vs Magnetic Field with orientation C

- ***2.6 Conclusions***: The device developed by a research group of CERN is definitively able to well operate in environment with very high magnetic field as shown by the tests reported in this paper and by the features given by the manufacturer. Moreover, the device highlights a good performance in term of both output ripple and noise: both spectrum and output ripple are in compliance with the required specifications.

3. PDB for LTDB

TO ue this PoL for the LTDB supply distribution. The following figure show the block diagram of the LTDB Power Distribution Section (PDB) (from Brookhaven National Laboratory, BNL).



Block diagram from BNL

The design of the PDB of the LTDB has been planned in 3 steps over a time line of 1-2 year(s):

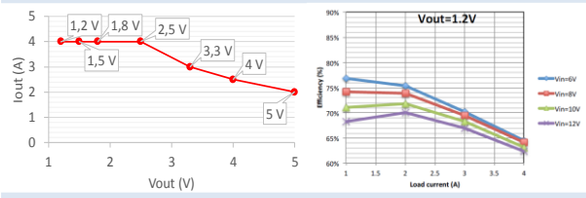
- ***Step 0 (by BNL):*** LTDB with on-board Power Distribution with devices from Linear Technology (digital part) and ST (analog part)
  + : LTM4616 (10 mV pp ripple), LTM4619 (20 mV pp ripple)
  -: LHC4913, LHC7913
- ***Step 1 (by Milan)***: a custom Power Distribution Board ("PDB") which can be mounted on the LTDB
  - LTDB and PDB development/test can proceed independently ..... Almost !
  - Performance tests on the PDB as a system are possible
  - Different PoL devices can be tested (if the interconnections between the two boards are not changed)

- ***Step 2 (by Milan)***: Power Distribution Section as a part of the LTDB
  - PDB layout "integrated" into the LTDB (to reduce the problems concerning the area)
  - Interesting for final LTDB production
  - The design is based on FEAST2 ASICs and re-design
  - Untested ASICs (expected yield ~ 95%) already purchased.
  - CERN is looking into the possibility of delivering full tested devices for future purchases.

4. The Step 1

The Step 1 consist in the design and manufacture of the PDB board. Many issues: mechanical, electrical *etc*…

Max current delivered by FEASTMP and its efficiency:



→ Many FEASTMP are necessary and Cold Plate is required

Power dissipation:

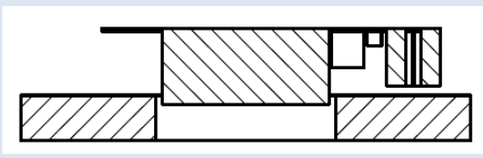
Output voltage	Efficiency (worst case)	Max Iout	Power dissipation
1.2 V	62 %	4 A	2.95 W
1.5 V	67 %	4 A	2.95 W
1.8 V	70 %	4 A	3.10 W
2.5 V	76 %	4 A	3.16 W
3.3 V	82 %	3 A	2.17 W
5.0 V	88 %	2 A	1.36 W

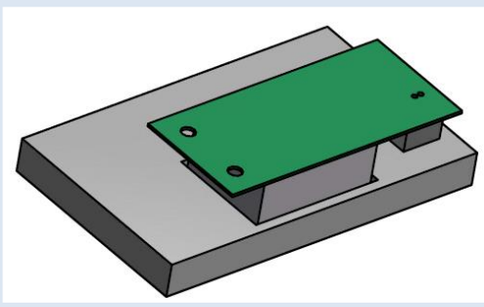
→ Many FEASTMP are necessary and Cold Plate is required

Number of FEASTMP utilized:

Items	FEASTMP output voltage
5	FEASTMP @ 1.0 V
3	FEASTMP @ 1.2 V
1	FEASTMP @ 1.5 V
2	FEASTMP @ 1.8 V
3	FEASTMP @ 2.5 V
2	FEASTMP @ 3.3 V
4	FEASTMP @ 4.0 V
20	Devices

PCB Design difficulties
→ many openings are necessary





Reduced available area
- Max: 410.55 x 53-74 mm (shaped, 0.026 m^2).
- There is no room to house the linear devices (LDO) on the PDB.
- Therefore the analog voltages will be obtained with the LDO devices mounted on the LTDB.

STEP 1 is focused on understanding the FEASTMP behavior in our specific application, the LDO behavior is not a concern because they have been widely used before.

5. Conclusions

- The design of the PDB has been addressed and the layout is now complete.
- Table of connections between LTDB and PDB as been defined (with BNL).
- Final PCB is reported in the following figure.
- PCB is in production;
- Tests expected in Nov/Dec 2015;
- If test successful the PDB will be inserted and tested as part of the LTDB by Brookhaven National Laboratory (BNL).

6. References

[1] Michelis, S.; Faccio, F.; Jarron, P.; Kayal, M., "Air core inductors study for DC/DC power supply in harsh radiation environment," in Circuits and Systems and TAISA Conference, 2008. NEWCAS-TAISA 2008. 2008 Joint 6th International IEEE Northeast Workshop on, pp.105-108, 22-25 June 2008.
[2] Michelis, S.; Allongue, B.; Blanchot, G.; Buso, S.; Faccio, F.; Fuentes, C.; Marchioro, A.; Orlandi, S.; Saggini, S.; Spiazzi, G.; Kayal, M., "An 8W-2MHz buck converter with adaptive dead time tolerant to radiation and high magnetic field," in ESSCIRC, 2010 Proceedings of the, pp.438-441, 14-16 Sept. 2010.
[3] Faccio, F.; Blanchot, G.; Fuentes, C.; Michelis, S.; Orlandi, S.; Saggini, S.; Troyano, I., "FEAST2: A Radiation and Magnetic Field Tolerant Point-of-Load Buck DC/DC Converter," in Radiation Effects Data Workshop (REDW), 2014 IEEE, pp.1-7, 14-18 July 2014.