KLauS
a low power
SiPM charge readout ASIC

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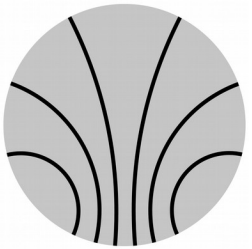


Overview

- Electronics for ILD scintillator-based calorimetry
- KLauS Prototype ASICs
  - Front-end development
  - ADC development
- Summary & further plans

Readout electronics for ILD scintillator based calorimetry

Charge measurement of Silicon Photomultiplier signals

Fully integrated: Front-end & Digitization

Low noise charge measurements

→ SiPM gain calibration

Large dynamic range

→ Large number of Silicon photomultiplier pixels

Time measurement & Autotriggering capability

Low Power consumption

Several million channels in calorimetry systems

25uW / channel with power pulsing (< 1% duty cycle)

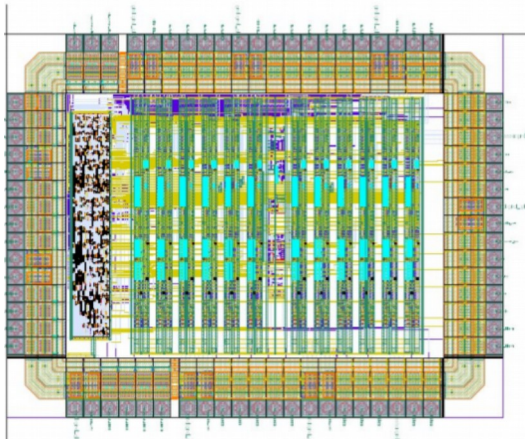
KLauS development history

2010

'KLauS2' : AMS 350nm Technology
12ch analog front-end

2011-2012

Detailed characterization of KLauS2

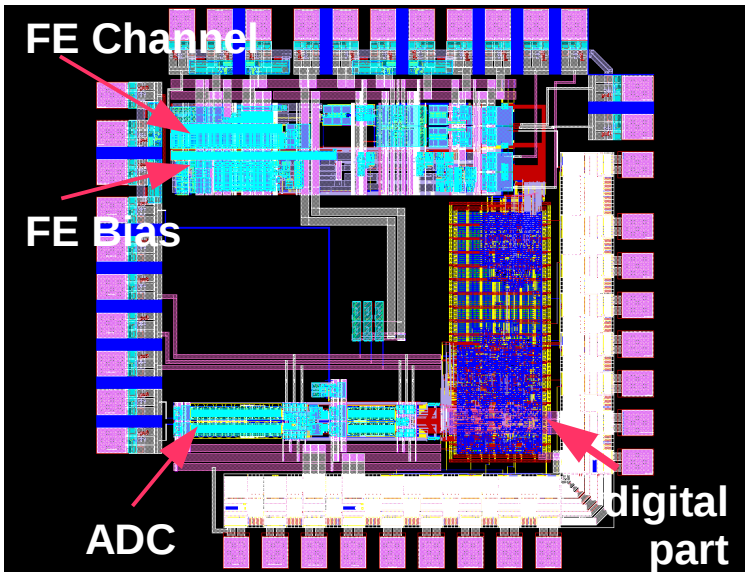


[KLauS2.0 – analog only]

March/15 & May/15

'KLauS3.0a/b' : UMC 180nm
→ New front-end
KLauS2 input stage & shaper topology
→ SAR ADC

Main goal for front-end redesign:
Optimizations for very low gain SiPMs
Low noise
Keep large dynamic range



[KLauS3.0 – Front-end & ADC]

Current prototypes

March / 15

- Front-end
  - Critical blocks implemented
- ADC channel

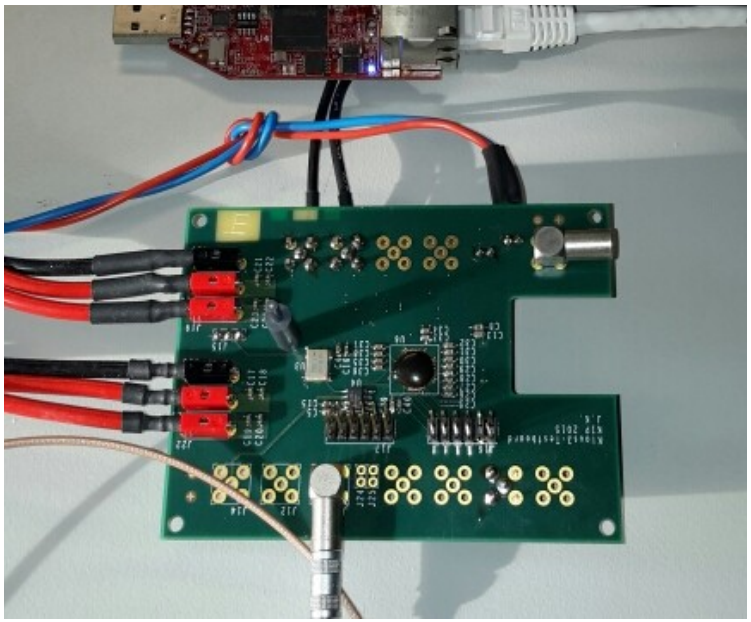
Received in July

- Being tested now

May / 15

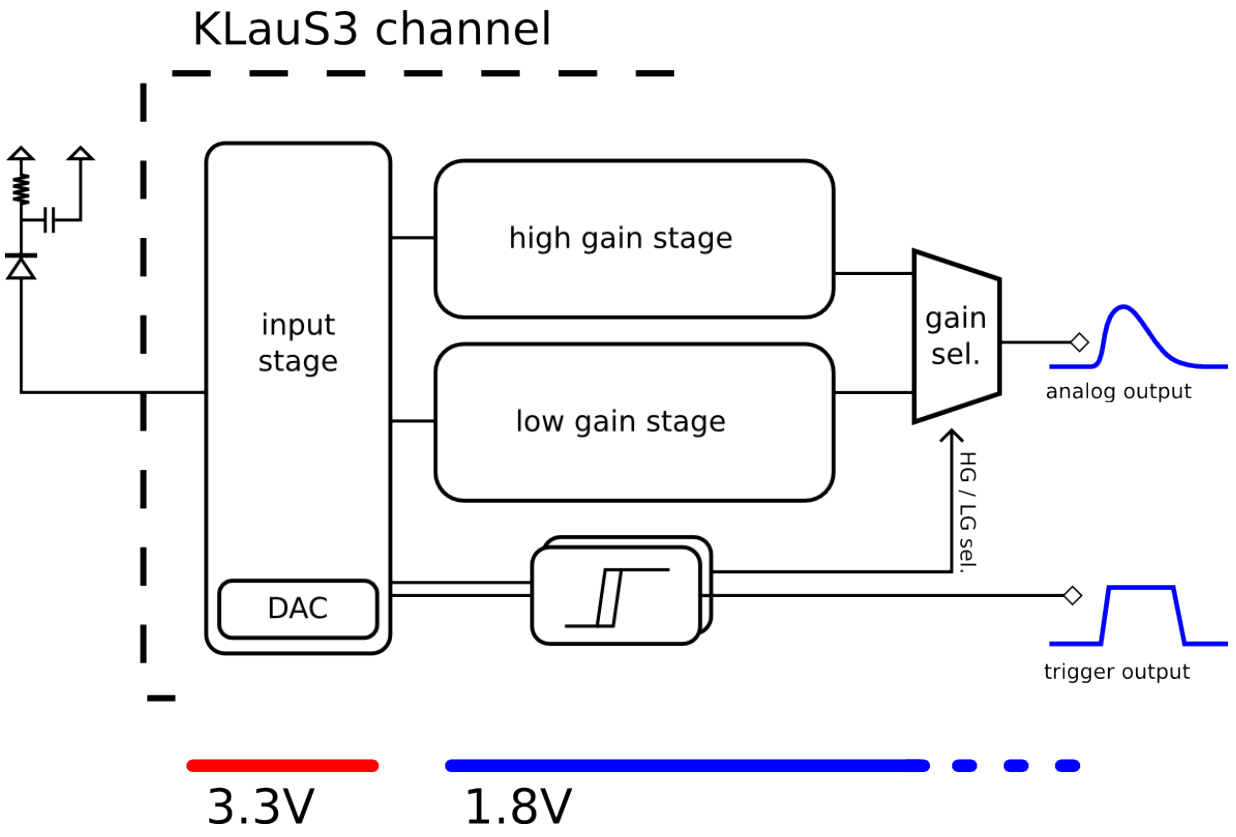
- Front-end
  - Most remaining Front-end blocks
  - Filter optimizations
- ADC
  - bug fix in control logic

Expected back mid-october



[KLauS3.0 test setup]

Front-end: Blocks



[Channel front- end blocks]

Input stage:
- Low input impedance
- SiPM bias voltage DAC

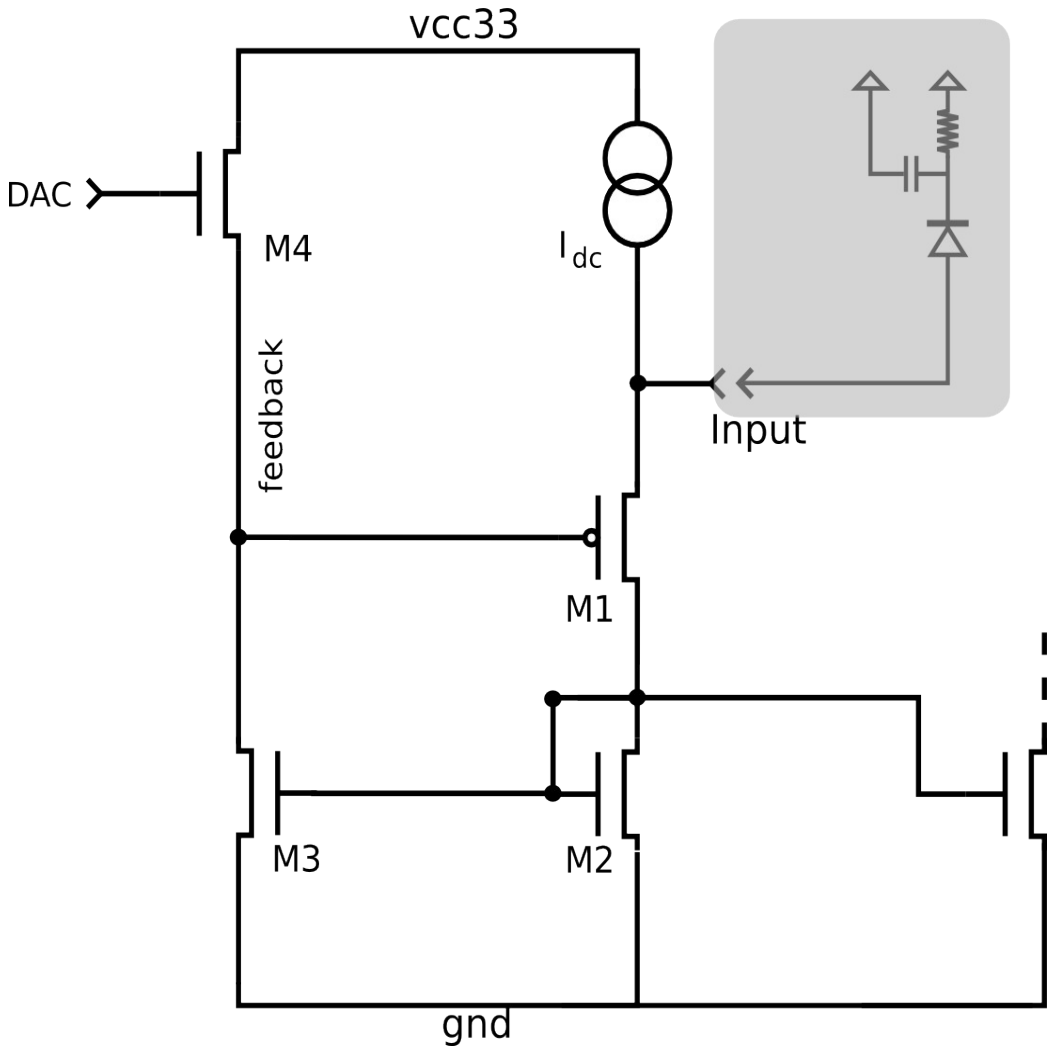
High gain stage:
- Single pixel spectra
- O(10ths of pixels)

Low gain stage:
- Full SiPM dynamic range

2 Trigger branches:
- Event trigger
- HG/LG selection

Minimize power consumption
- Power gating
- Dual supply scheme

Input stage topology



[simplified schematic]

Common gate & current feedback

$$R_{in}^{DC} = \frac{1}{g_{m1}} - \left(\frac{g_{m3}}{g_{m2}} \times \frac{1}{g_{m4}} \right)$$

Nominal input impedance ~50Ω

150uA bias current @ 3.3V

SiPM Bias voltage tuning

['DAC' → 'feedback' → input]

~ 2V tuning range

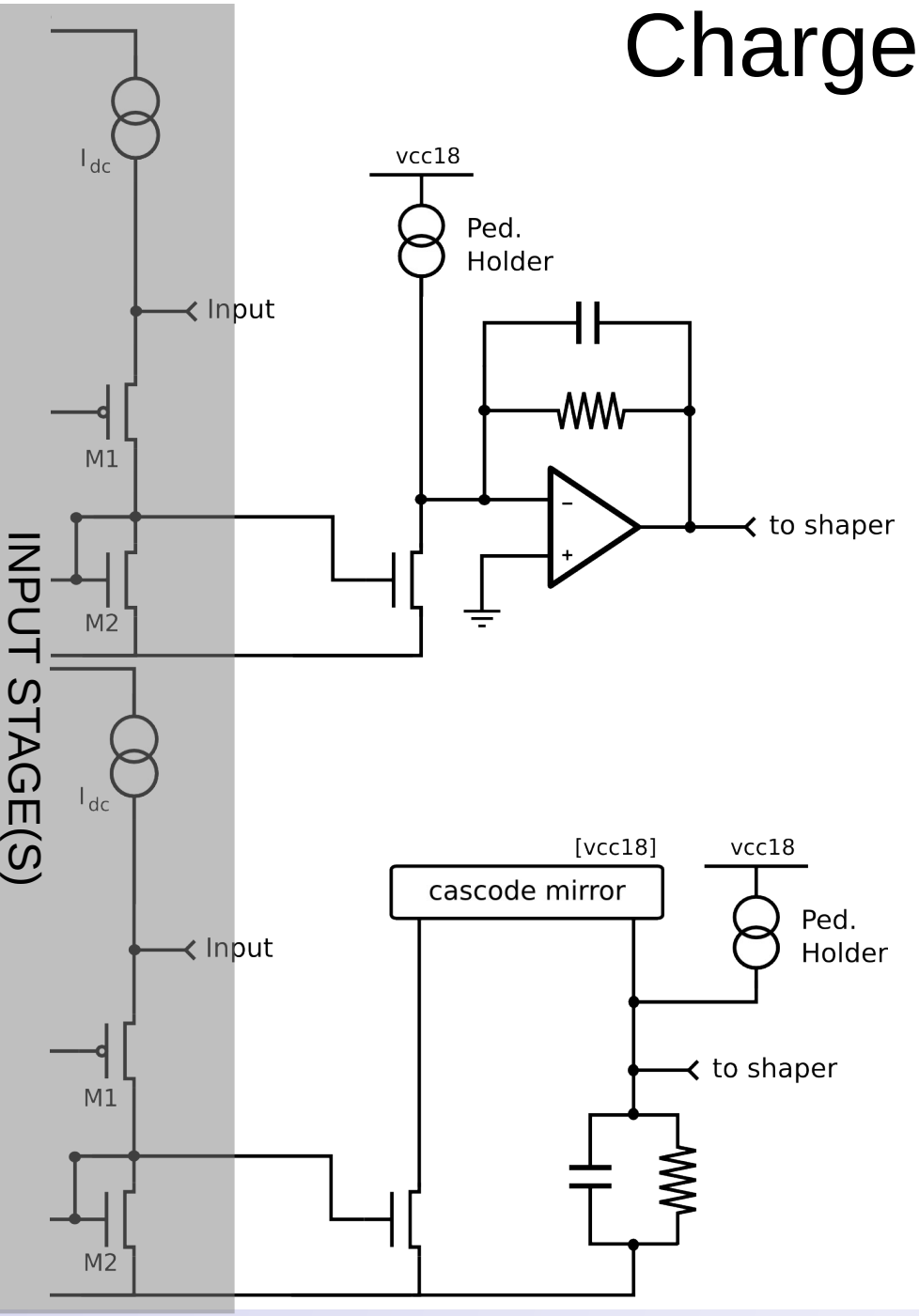
Low power 8bit DAC

2nA / LSB

Power gating compatible

Small DC input voltage change in low power mode

Charge integration



High gain stage: Active integration scheme

for small signals on single pixel level

Miller-opamp with 400MHz GBW

Low gain stage: Passive integration

for large signals

input stage mirror: regulated cascode

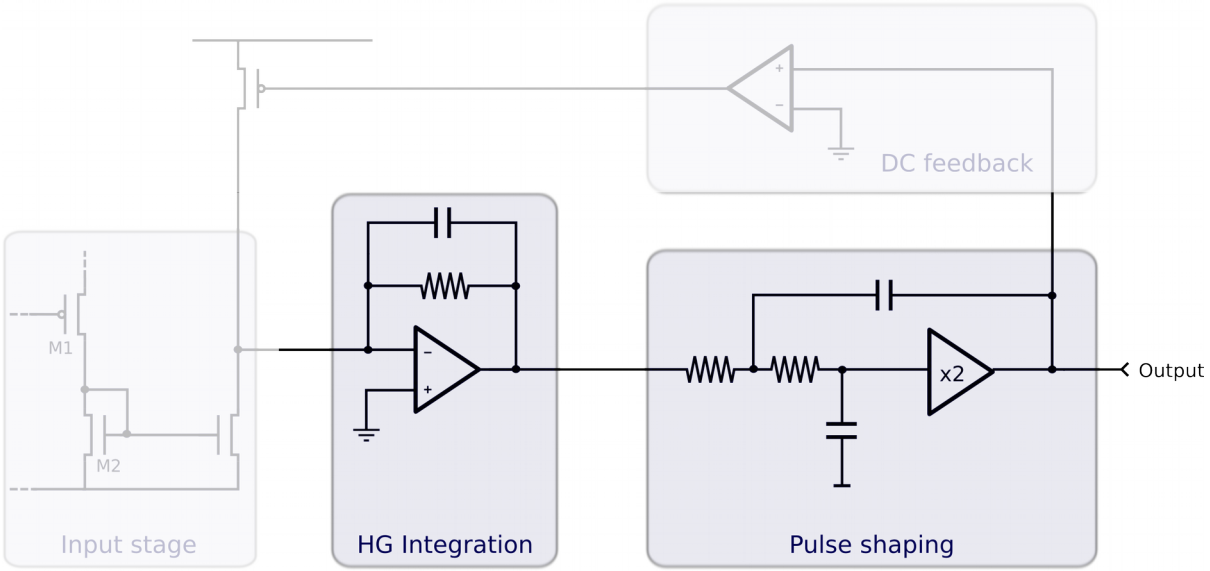
pmos integration mirror: low voltage cascodes

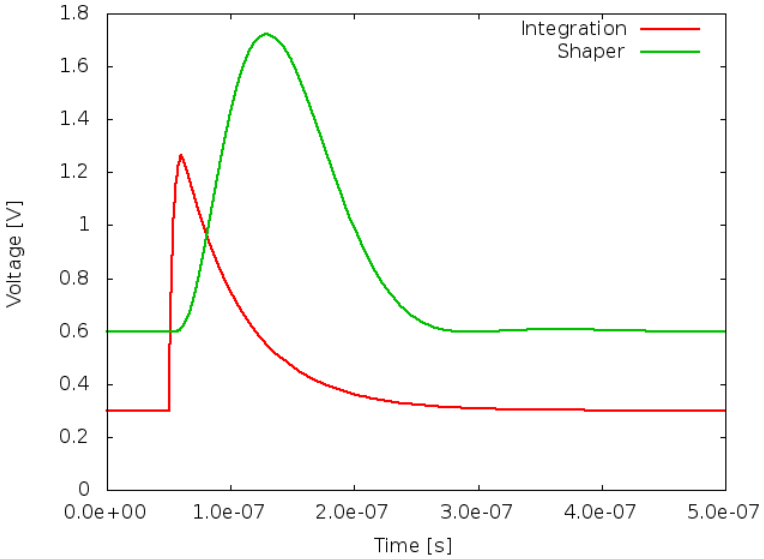
Pedestal stabilization

DC feedback of channel output

Using subthreshold Amplifiers

Shaper and channel pulse response





$$H(s) \propto \underbrace{\frac{1}{s \cdot \tau}}_{Integration} \cdot \underbrace{\frac{1}{(s \cdot \tau + 1)^2 + 1}}_{Shaper}$$

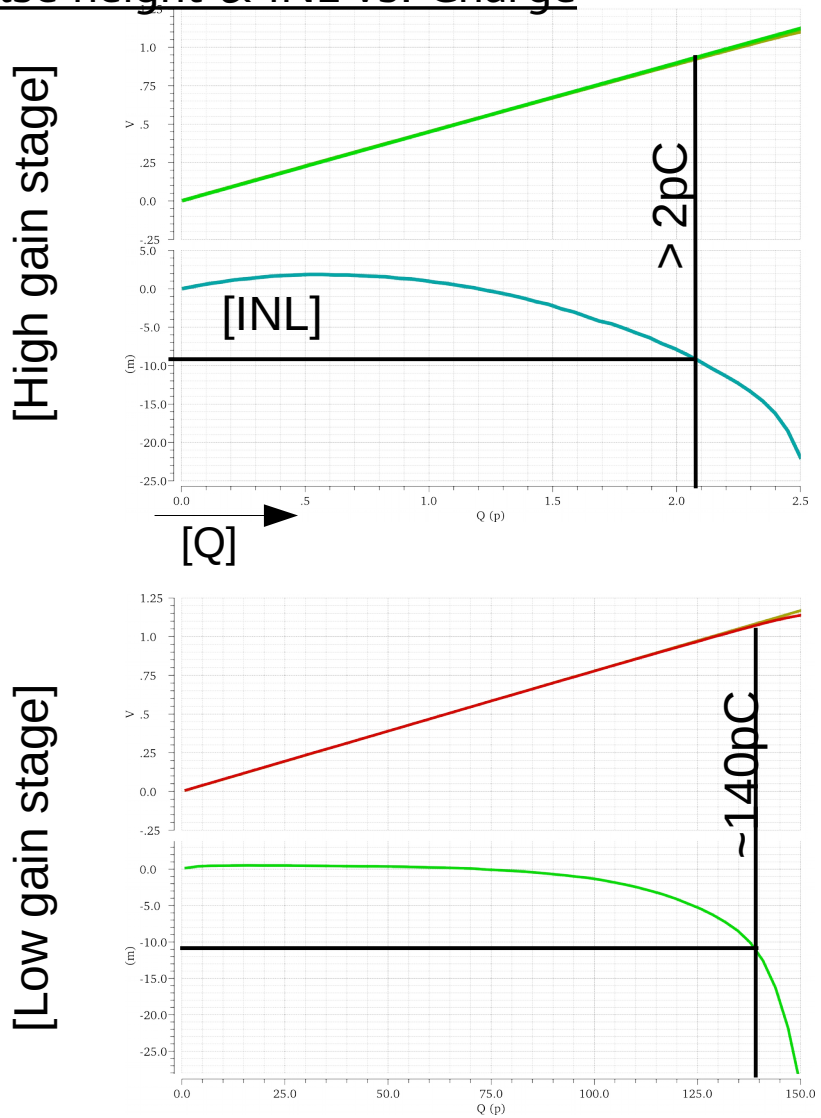
$$h(t) \propto e^{(-t/\tau)} \cdot \left(1 - \cos\left(\frac{t}{\tau}\right)\right)$$

Shaper: Sallen-Key topology
→ pair of complex poles

Same time constants for integration & shaper
→ Semi gaussian pulse, small undershoot

Simulations: Linearity & Noise

Pulse height & INL vs. Charge



High gain stage

Design goal:

Allow decent SNR for very low gain Sensors

[e.g. Hamamatsu 10µm series, Gain ~10^5]

Expected ENC < 3fC

→ Single pixel S/N > 5

Dynamic range ~ 2pC @ INL < 1% FSR

[≈ 135px for 10µm ; ≈34px for 25µm MPPC]

Low gain stage

Exploit SiPM dynamic range

~ 140pC @ INL < 1% FSR

Moderate SNR requirements

Equivalent noise charge ~ 50fC

Front-end measurements: SiPM bias voltage DAC

Measure DC voltage at SiPM input

2V tuning range acheived

2 ASICs: Little deviations in slope

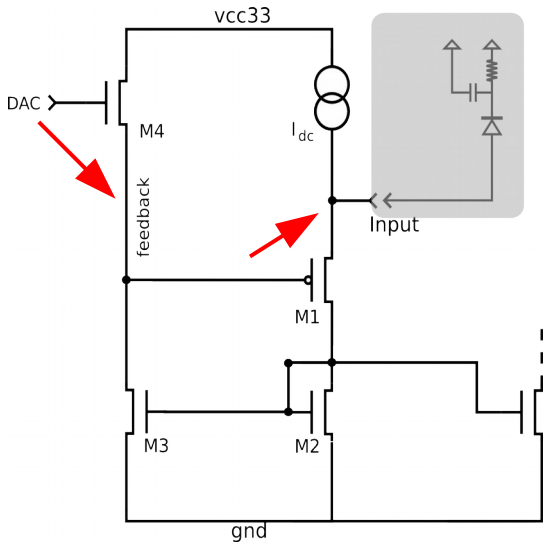
[external Vref + 1.5b trimming]

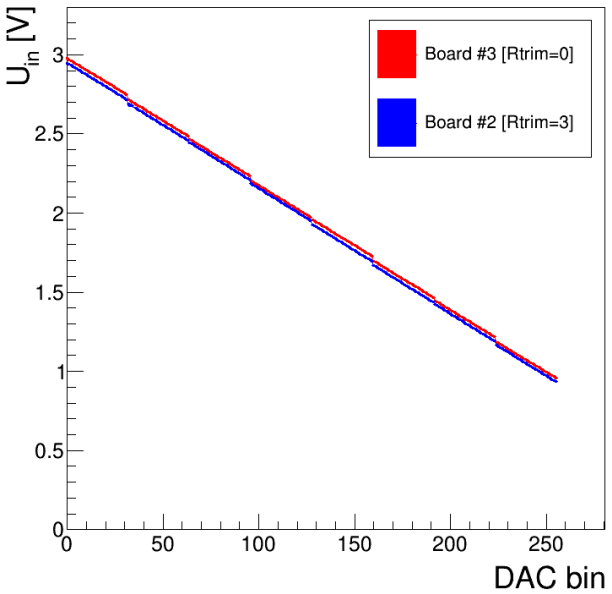
Analysis of Nonlinearity sources

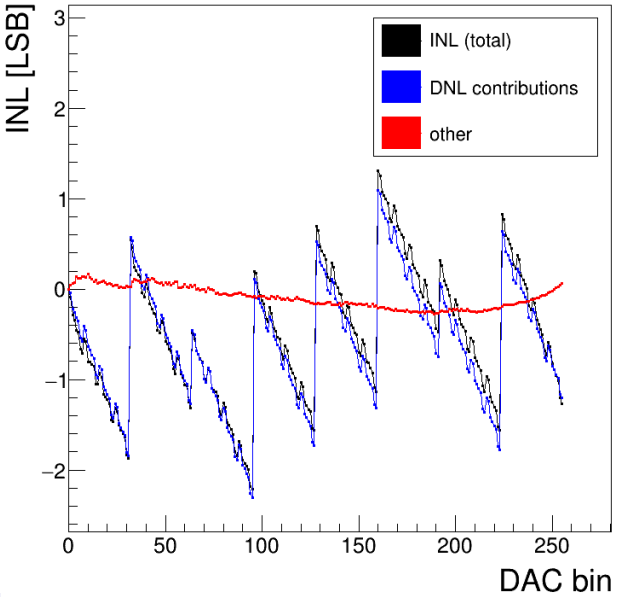
Main source is DNL (3 LSB)

[Layout update in next submission]

Other sources negligible & as expected



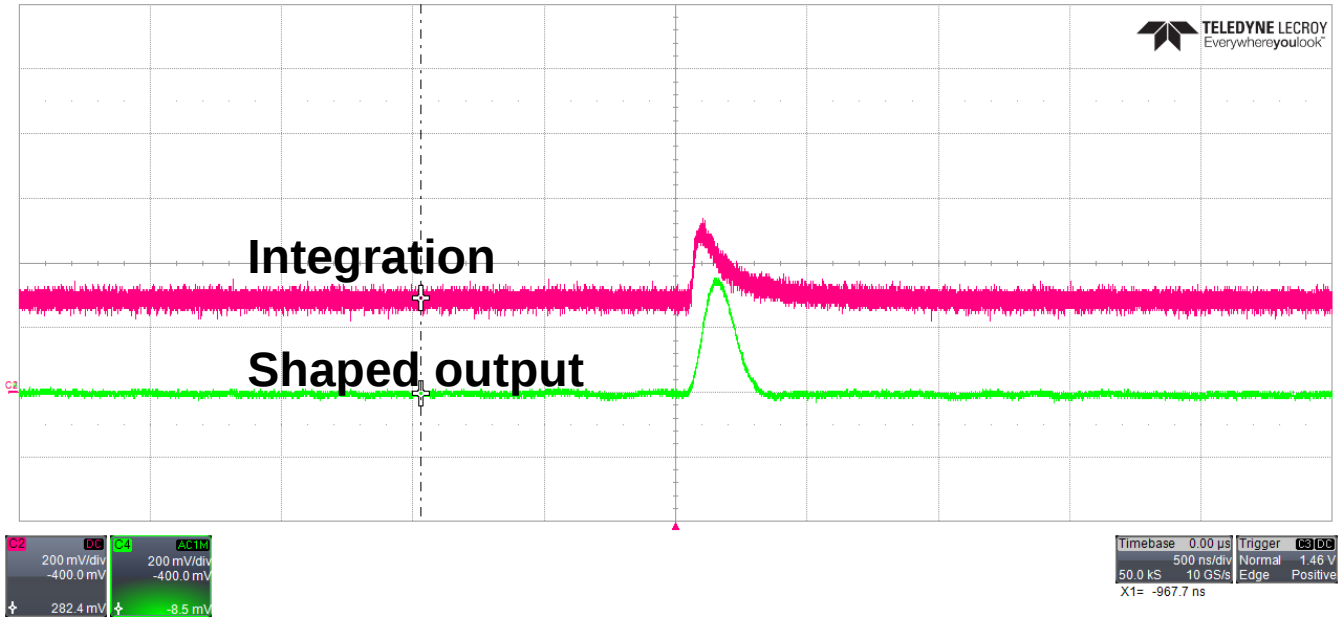


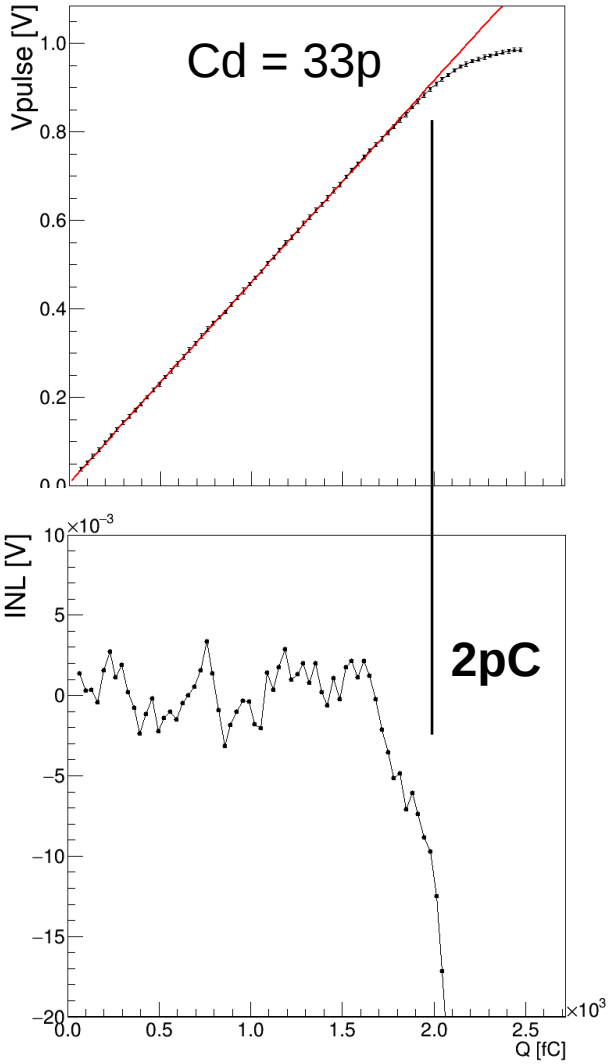


Front-end measurements: Charge injection

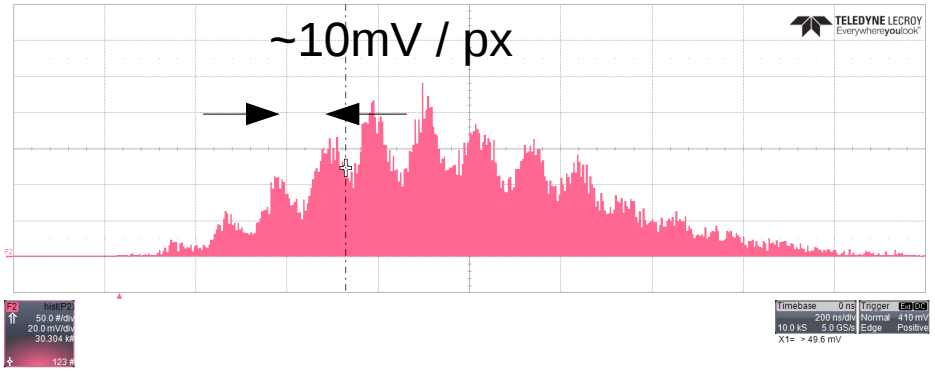
Test of high gain stage

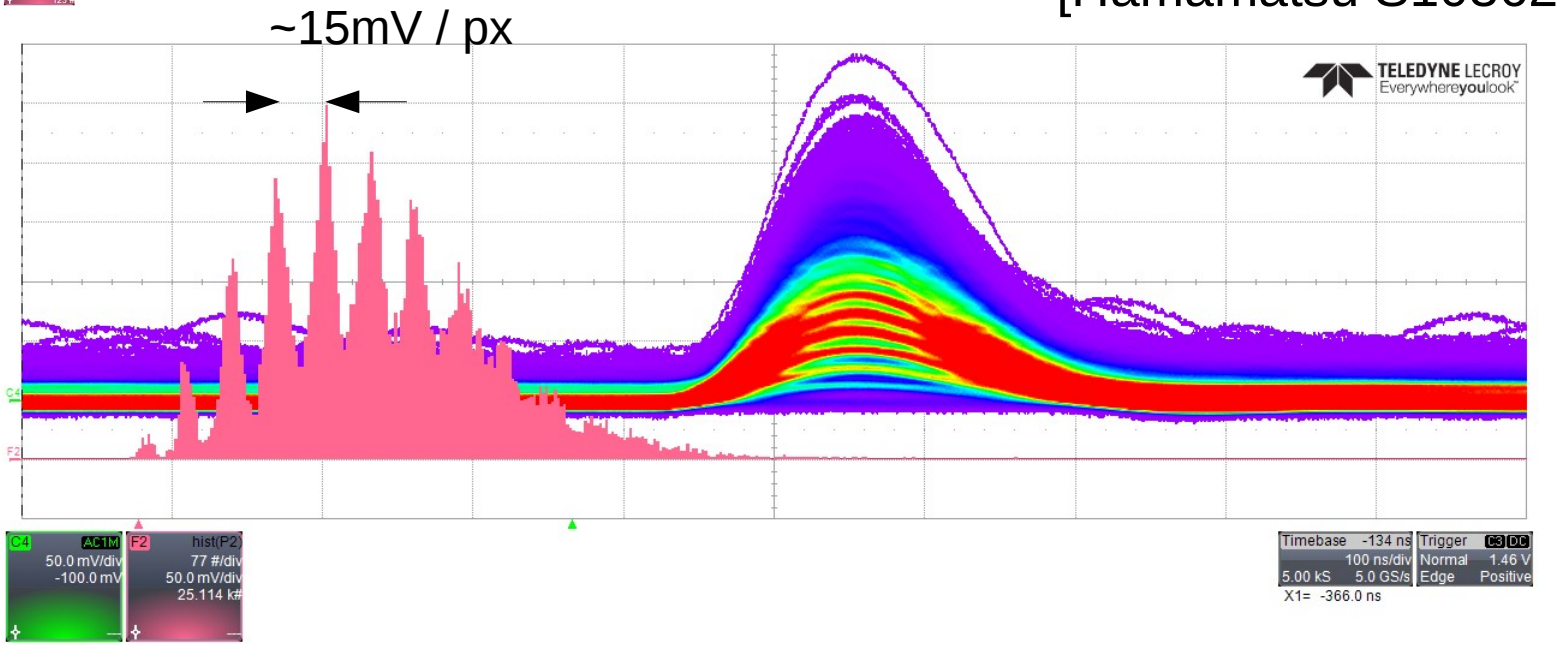
- Pulse shape after integration & shaping
- Dynamic range
  - Sufficient for single pixel spectra
  - Preliminary bias settings
  - Limited by off-chip driver dynamic range





Front-end measurements: test with sensors





Two SiPM models tested

10µm pixel device [Gain ~1.5x10^5]
[Hamamatsu S12571-010C]

25µm pixel device [Gain ~2.75x10^5]
[Hamamatsu S10362-11-025C]

SAR ADC development for KLauS

1 ADC per front-end channel
→ Development of low power ADC

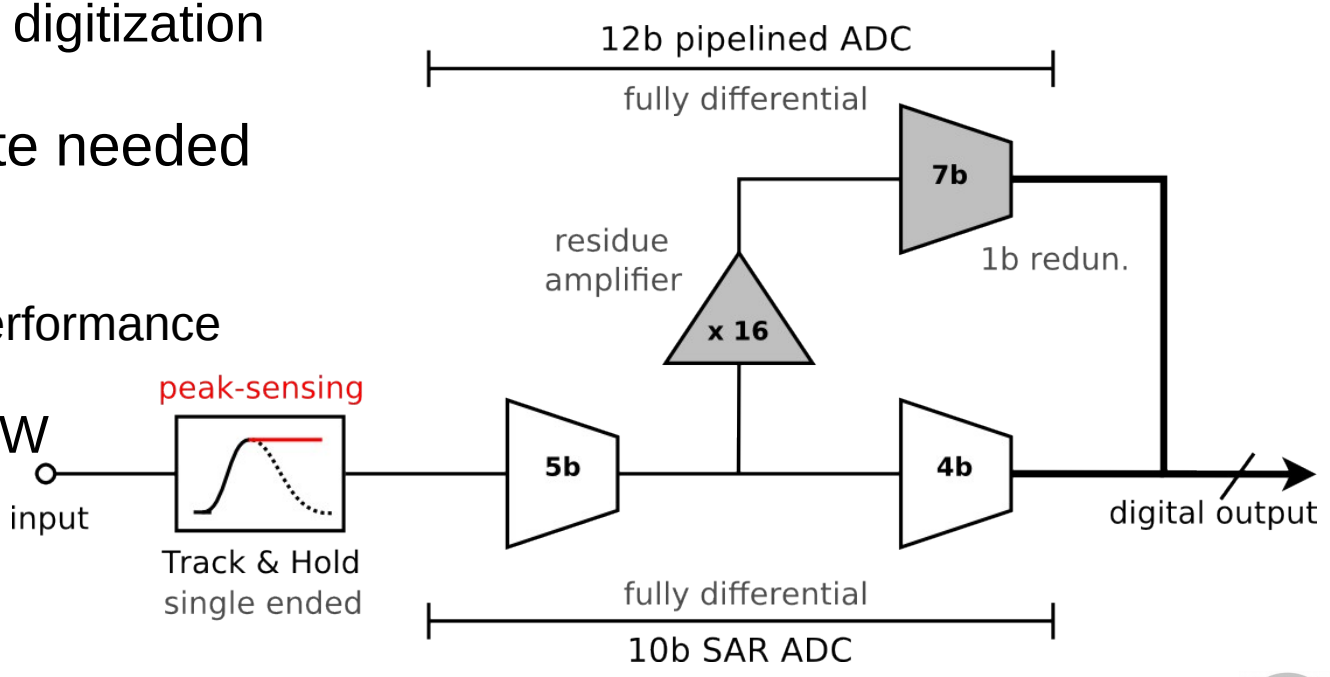
Two operation modes:

MIP quantization – **10bit resolution**
5+4bit SAR ADC

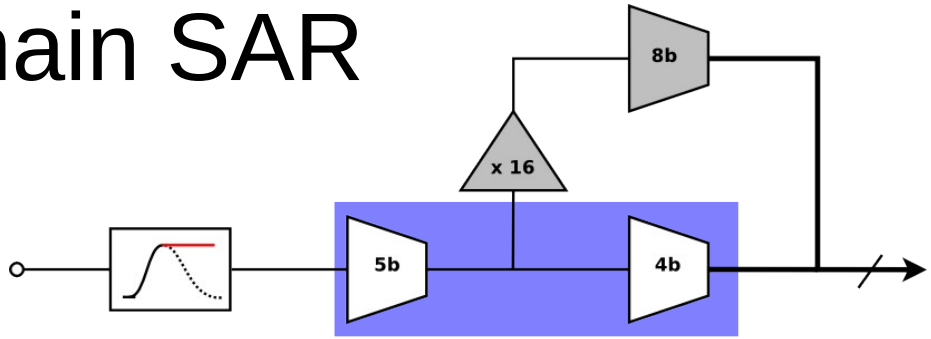
SiPM gain calibration – **12bit resolution**
Additional pipelined stage
Residual amplification & digitization

Relatively low Sampling rate needed
Peak voltage digitization
validated up to 3MHz
No constraint on dynamic performance

DC Power consumption < 1mW

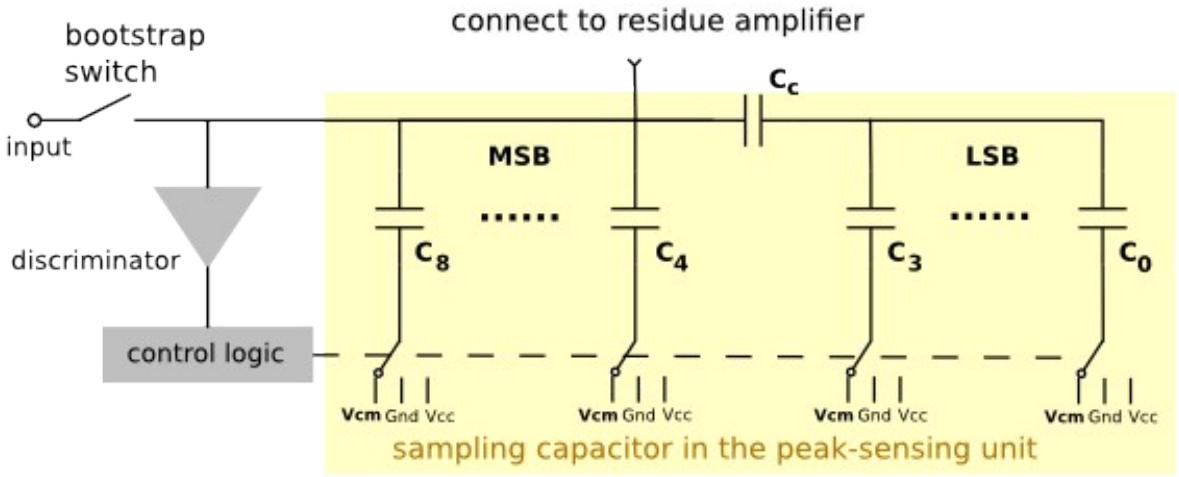


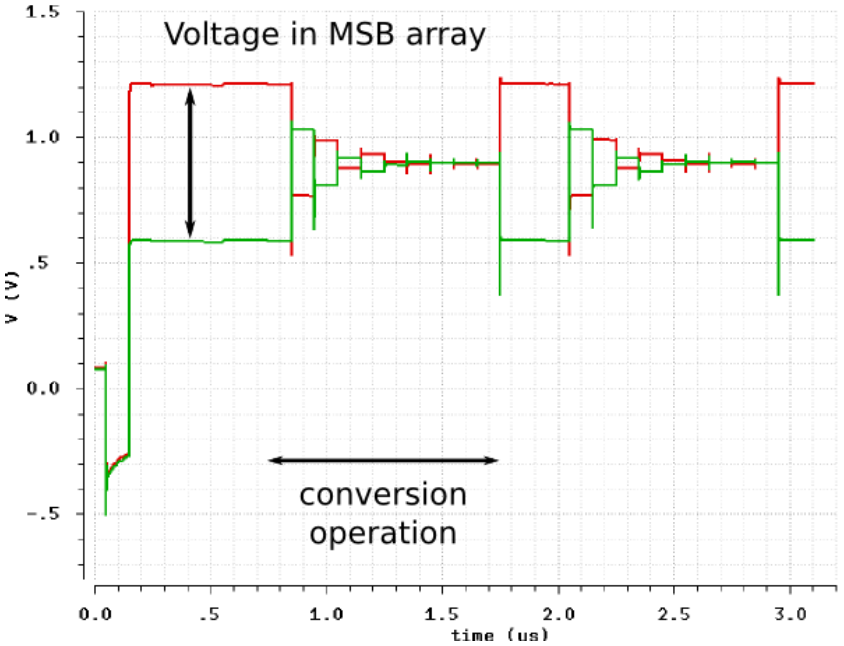
ADC – 10bit main SAR



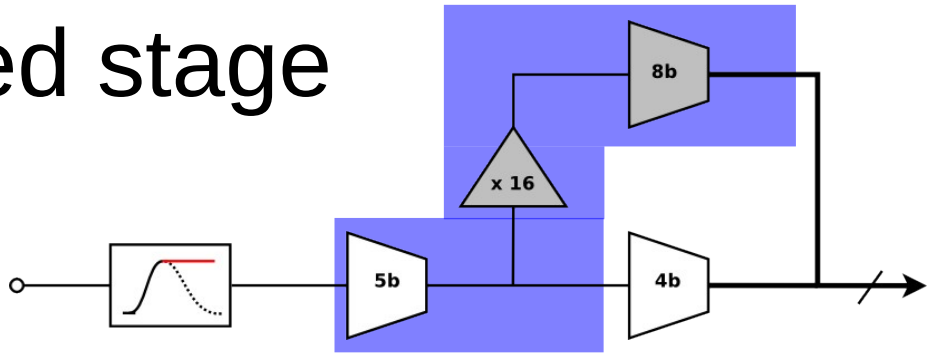
SCA:
5+4bit binary MIM capacitor array
Unit capacitor ~ 34fF

Other blocks:
Dynamic comparator
Bootstrap sampling switch
Control logic in digital part





ADC: Pipelined stage



12b resolution operation mode
for SiPM spectrum digitization

3 digitization steps:

(1) 5b digitization in main SAR

(2) Amplification of residual error

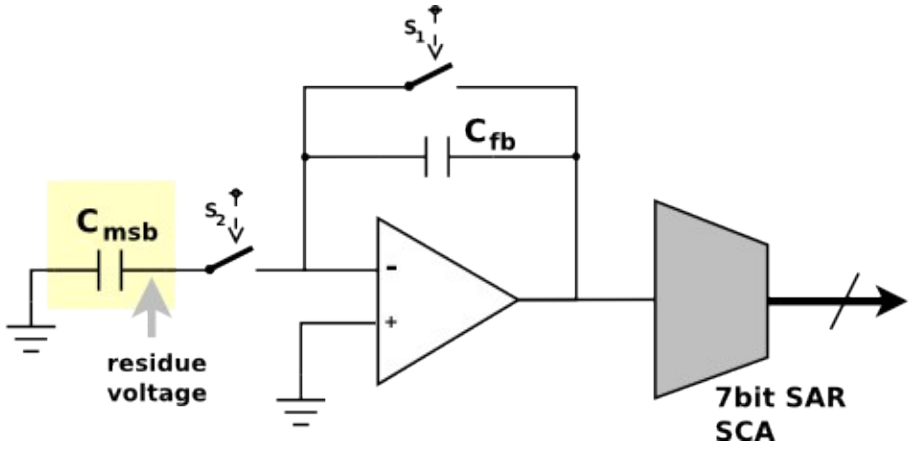
Fully differential folded cascode amplifier

(3) 8b digitization in pipelined stage

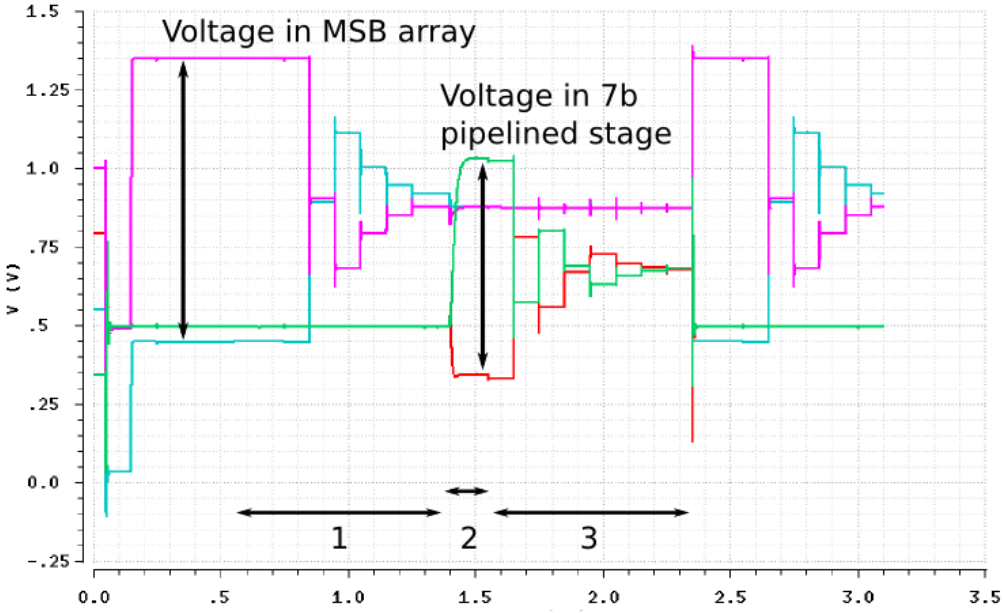
5+4 split MIM capacitor array

Unit capacitor ~ 34fF

remaining bits saved for redundancy



(1) (2) (3)



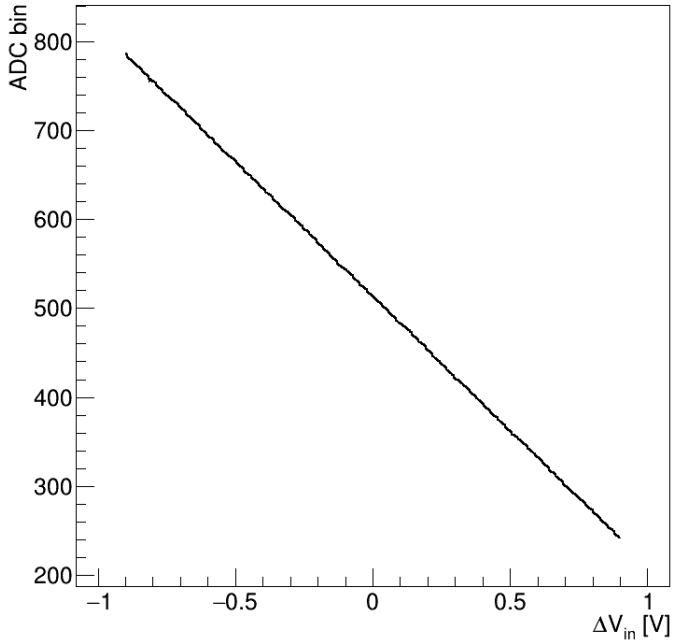
Static voltage measurements

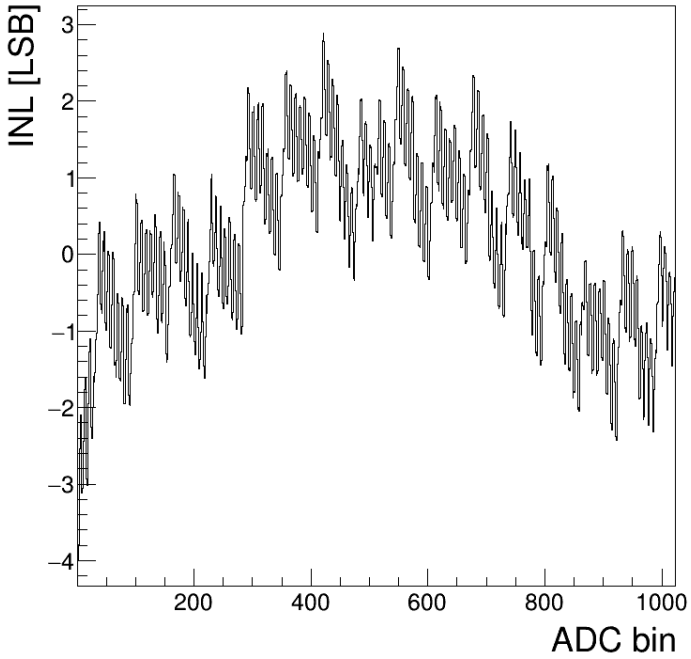
Sweep differential input voltage

Peak-to-peak INL < 7 LSB

Some unexpected DNL patterns in least significant bits

INL modulation every 8 bins (DNL effect)



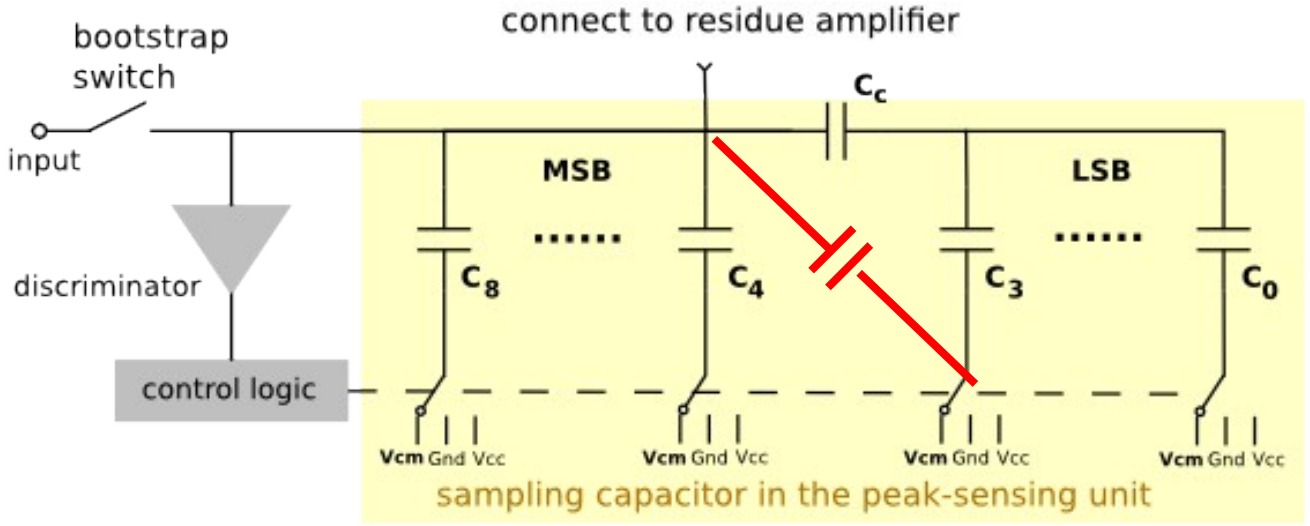


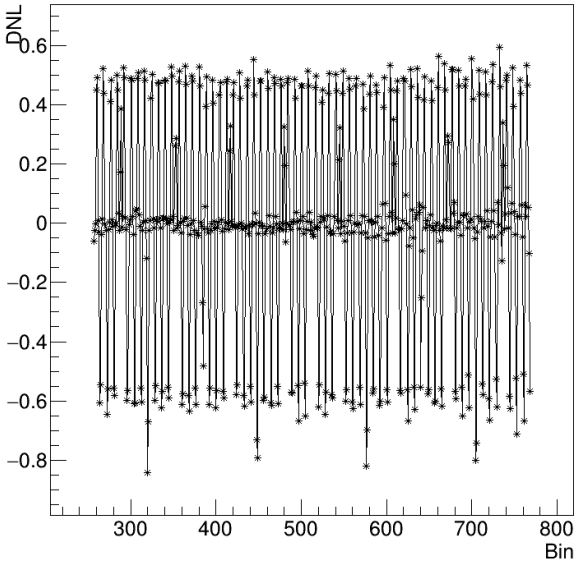
Static voltage measurements: DNL

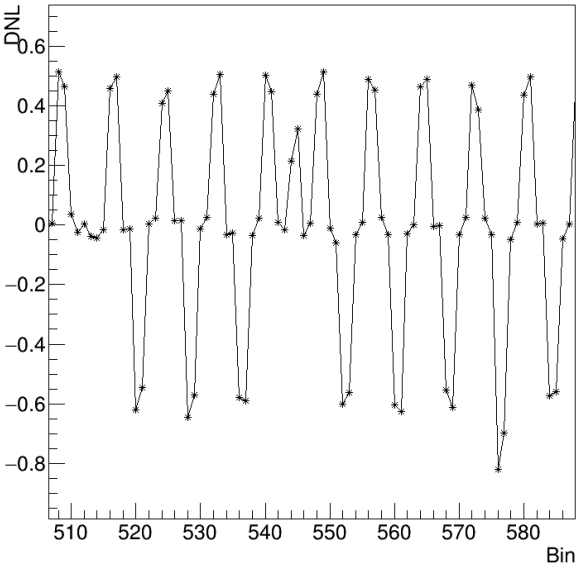
DNL analysis
- Overall DNL < 0.8 LSB

Dominant DNL pattern on less significant bits
- This effect ~ 0.6 LSB

Cause for effect: 600aF line coupling
- LSB array switch line ↔ MSB array signal line
- Effective Parasitic ~ 9fF







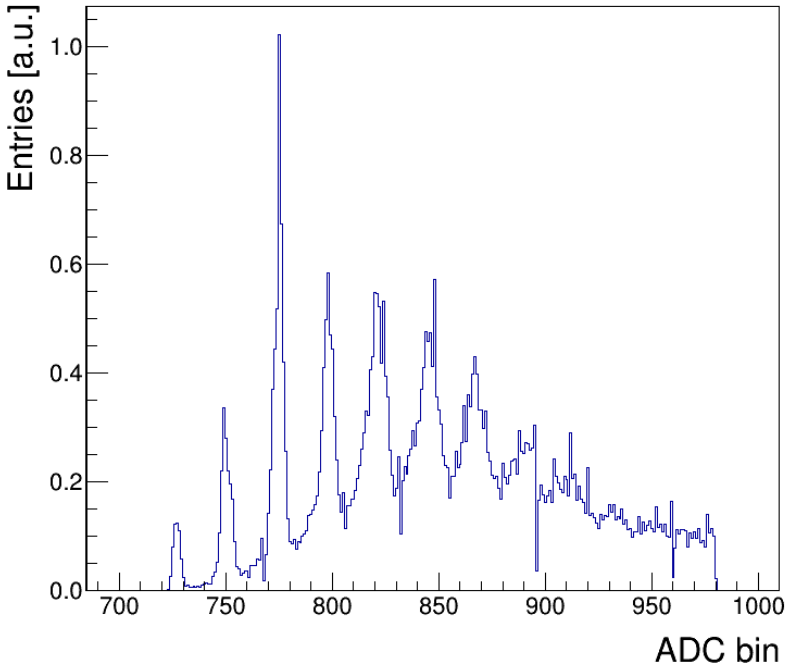
Front-end & ADC: combined operation

Due to DNL effects:

- Modulation of bins can fake Single Photon spectrum

Use large gain (50um pixel) SiPM

- Simple DNL correction performed



Summary and Outlook

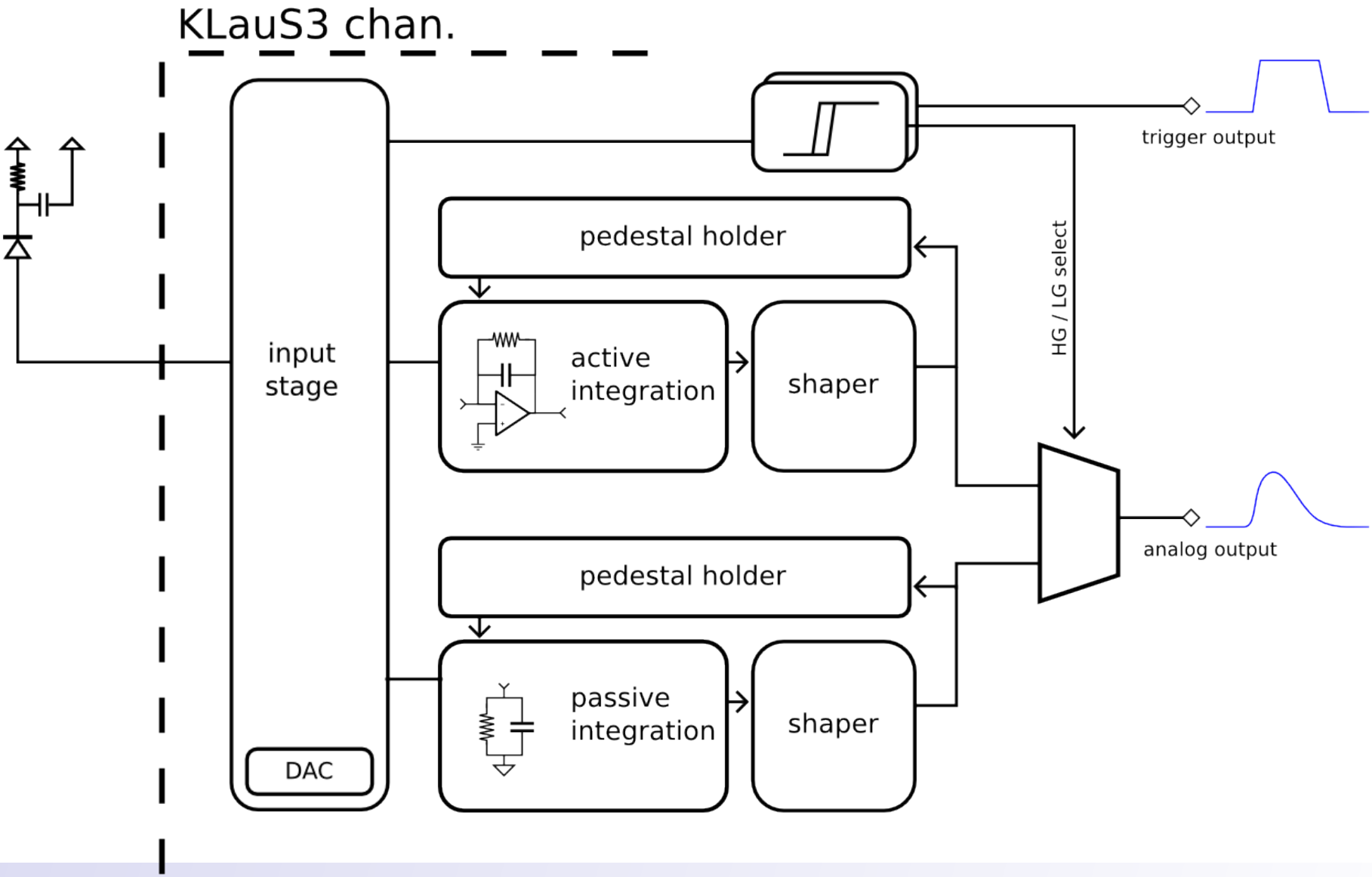
KLauS
- Low power charge readout ASIC for low gain SiPM
- Two Prototype ASICs submitted in 2015
  - New Analog Front-end
  - 10B / 12B SAR ADC

Preliminary measurement results
- Front-End
  - Bias tuning range verified
  - Visible single pixel separation for 10um SiPMs
- ADC working in 10b mode
  - 0.5 LSB DNL effect found, will be corrected in November submission
  - Visible single photon spectrum in combined Front-end & ADC measurement

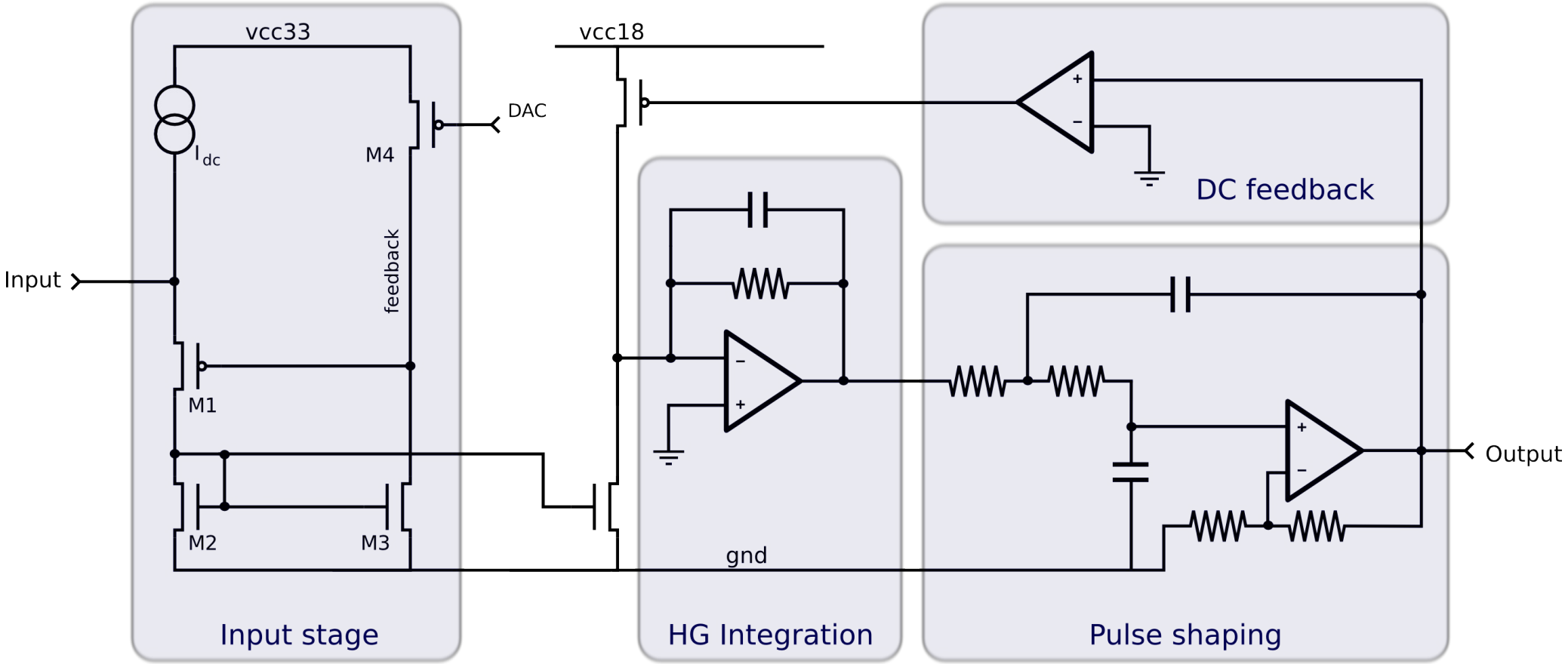
Further development plans
- November: Multi channel ADC with corrected layout
- Until summer 2016: Full multi channel version (FE & ADC)

Thank you!

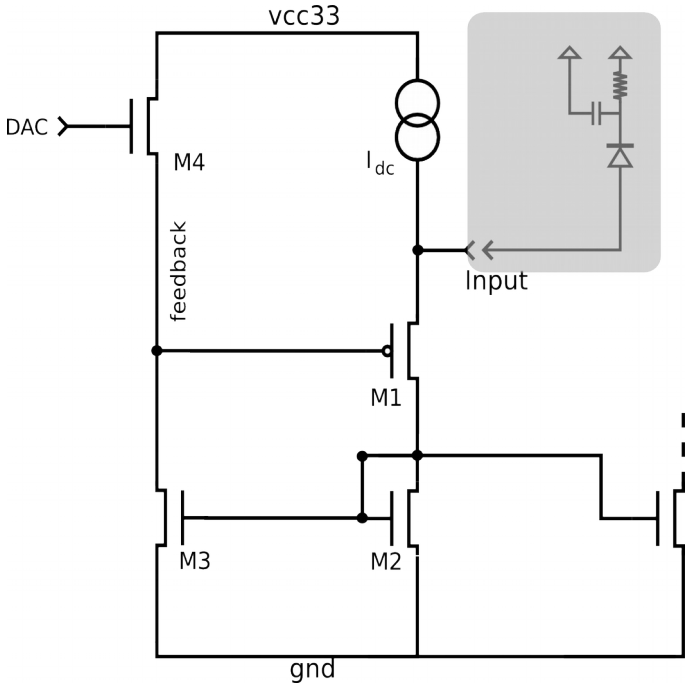
Front-end: block level schematic



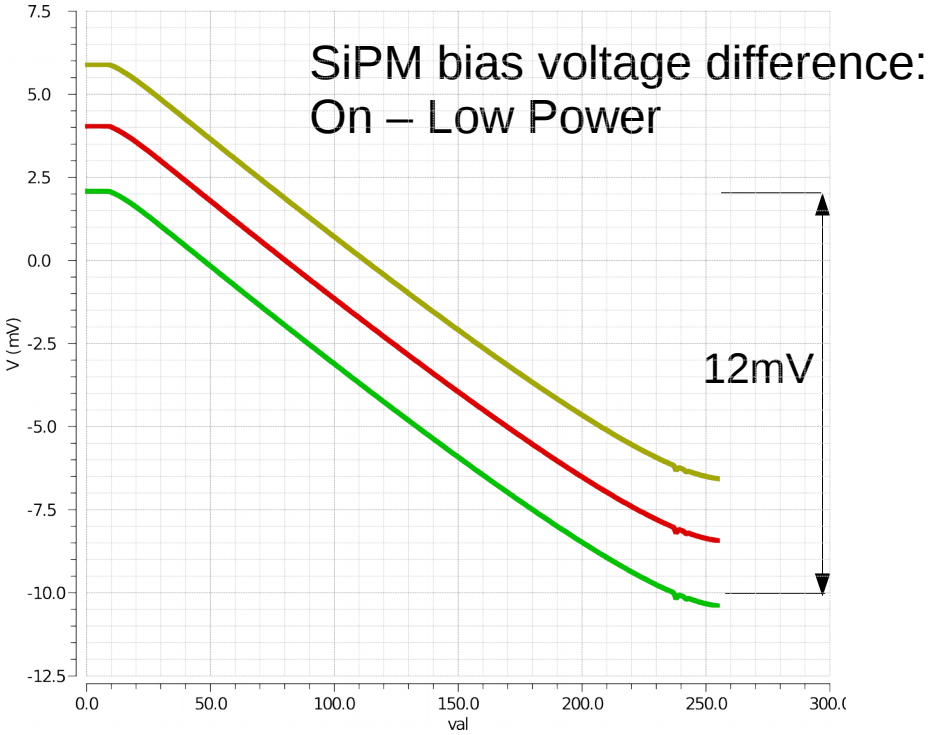
Input stage & HG branch



Input stage : Power gating



[input stage: simplified schematic]

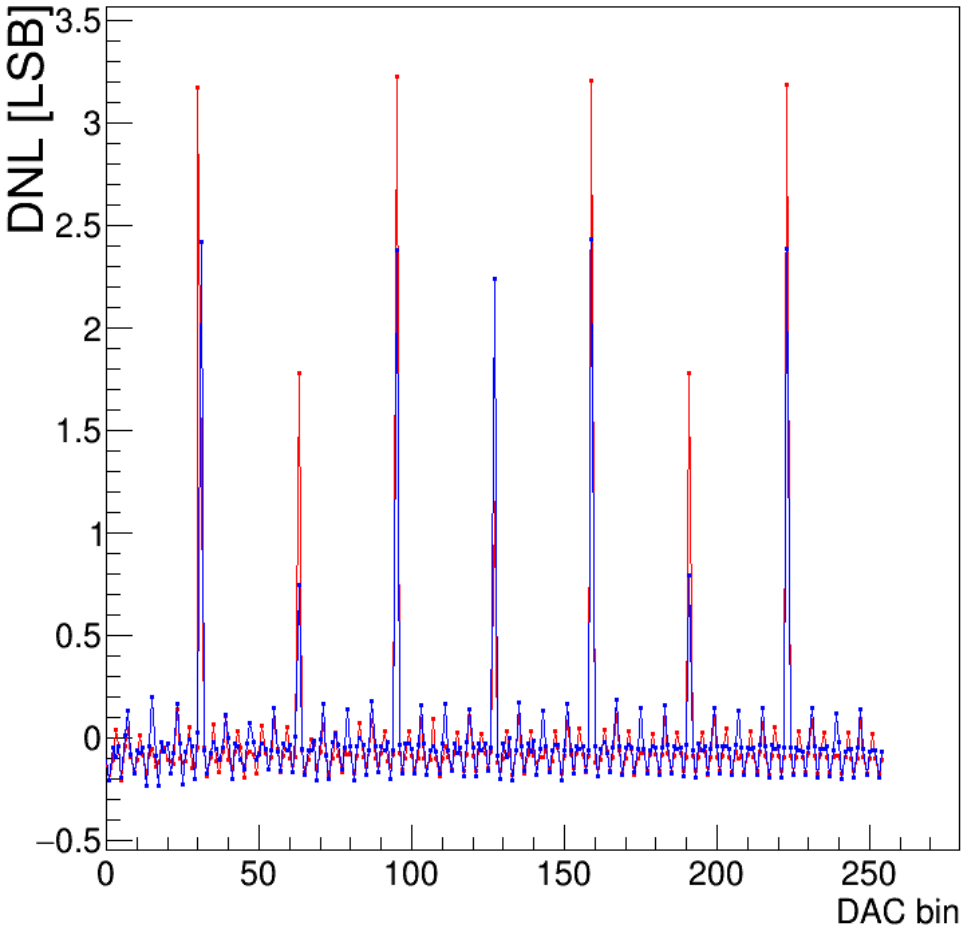


During Power down:
- Lower Bias current ('Idc' source)
- Disable feedback mirror
- O(100nA) compensation current in feedback path

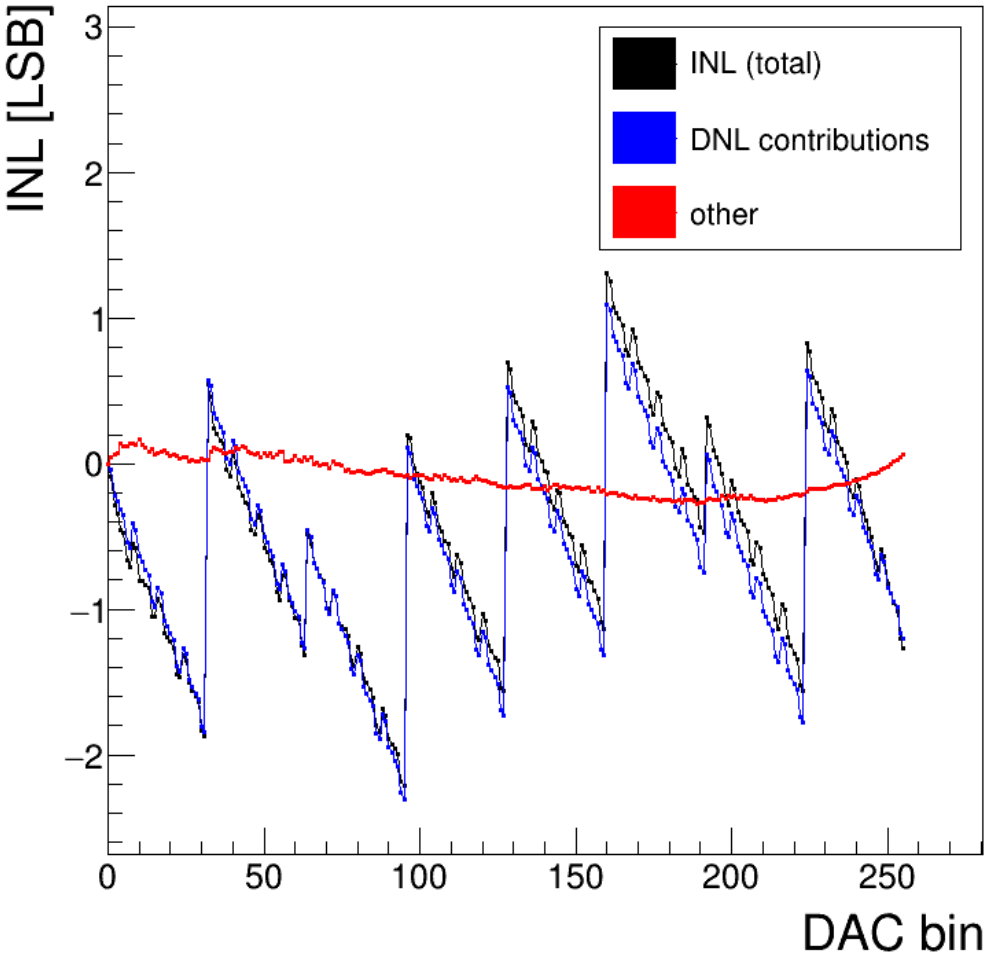
Compensation current:
- Minimize SiPM bias voltage difference
- 4b subthreshold DAC
- Offset < ±6mV

Front-end characterization: SiPM bias voltage DAC

DNL [2 Chips]



INL contributions



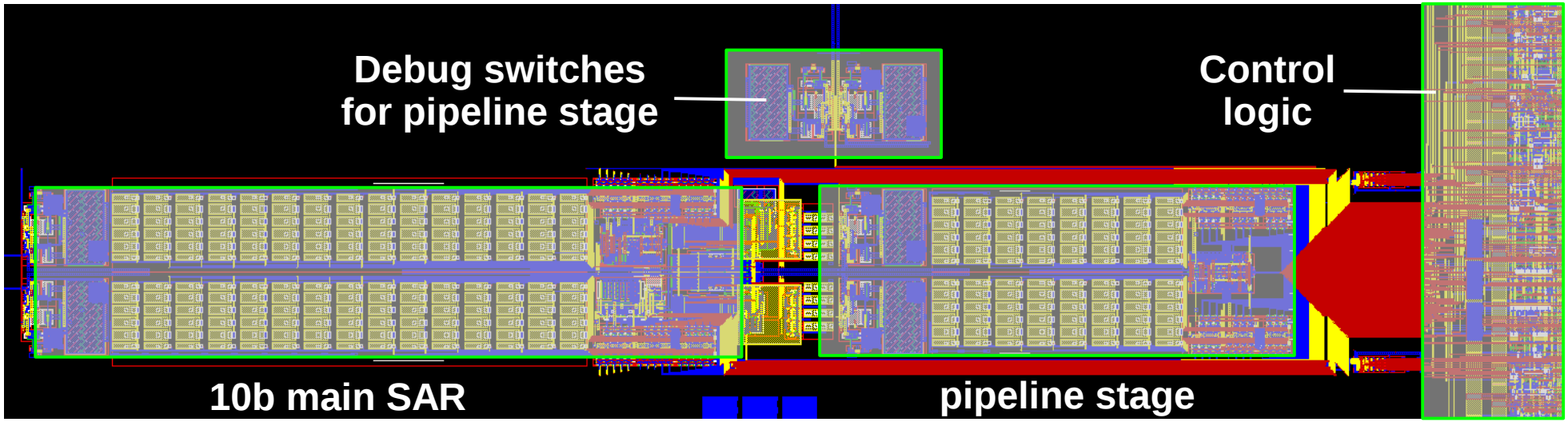
ADC: first prototype

Prototype in March '15:

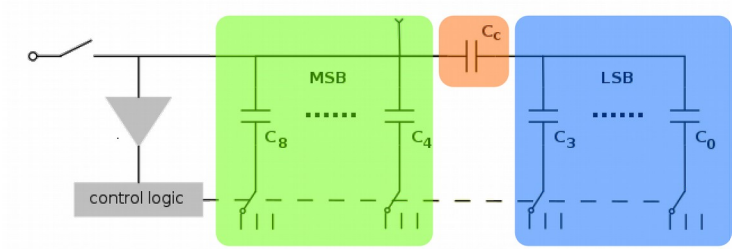
- Main SAR & Pipelined stage
  - Simple serial readout link
  - Size: 670x120 um

Submission in May '15:

- bug fix in digital control logic - pipeline mode not operational



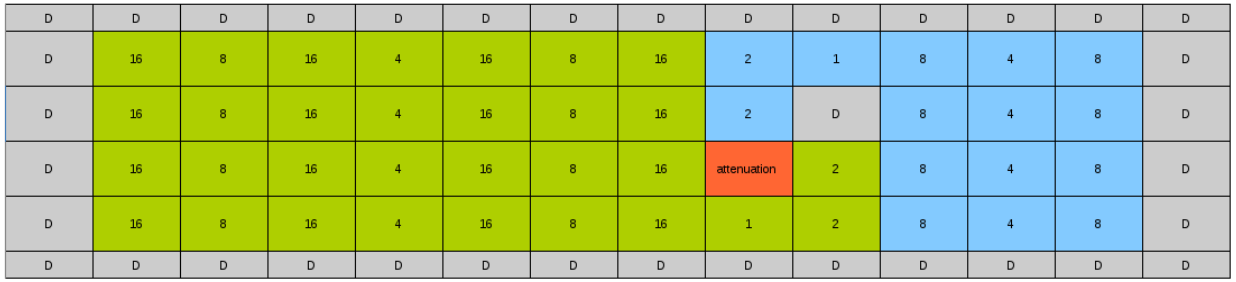
ADC: Corrected Layout



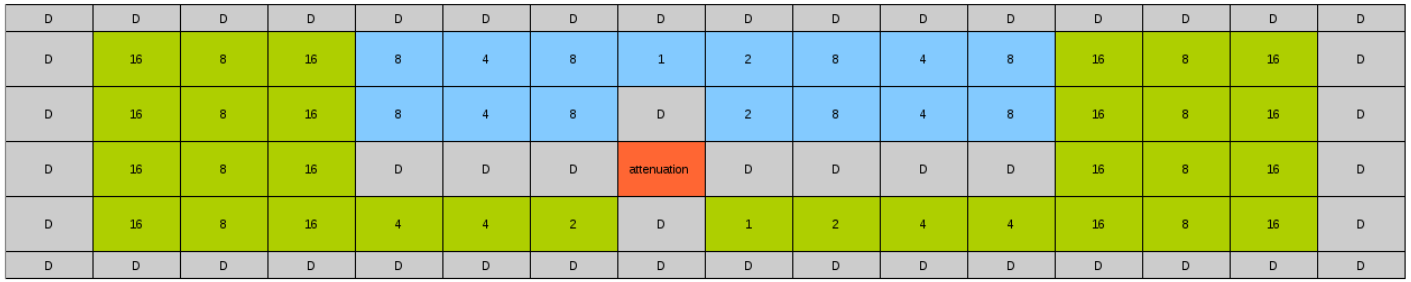
Stronger separation of MSB and LSB array
- Signal lines
- Bridge capacitor

More symmetric layout
Match parasitics in MSB and LSB subarrays
Re-submission in November

Array layout sketch



Current version



Updated