Contribution ID: **223** Type: **Oral**

KLauS: A low power Silicon Photomultiplier Charge Readout ASIC in .18 UMC CMOS

Thursday, 1 October 2015 11:10 (25 minutes)

We present the development of a low power Silicon Photomultiplier readout ASIC for imaging calorimetry detectors at future linear colliders. The analog front-end is designed to achieve sufficient SNR for single pixel signals using low gain SiPMs, while allowing charge measurements over the full sensor dynamic range.
It consists of an input stage, two charge measurement branches and a fast comparator.
A SAR ADC with a resolution of 10 bit digitizes the pulse height information.
An additional pipelined SAR stage allows to increase the quantization resolution to 12 bit.
Design details and first characterization measurements will be shown.

Summary

For calorimetry systems in future linear collider experiments, an unprecedented granularity is needed, resulting in a large number of individual channels. In the analog hadronic calorimeter concept of the CALICE collaboration, the individual channels consist of scintillating tiles read out by Silicon Photomultipliers. The readout electronics, integrated into the detector layers, is required to have a power consumption of 25uW per channel, using power gating schemes with a duty cycle of 1%.

For the measurement of large signals, spanning the full dynamic range of the sensors, a large dynamic range of 150pC is required.
For calibration measurements however, a signal to noise ratio > 5 for single pixel signals should be achieved.
The front-end development seeks to allow operation of SiPMs with 10kpx/mm^2, where the intrinsic gain can be as low as 10^5, contradicting the dynamic range requirements.
Therefore, both the front-end and ADC implement two stages or operation modes to cope with the different requirements for calibration and large signal readout.

The input stage is using a current conveyor structure to lower the input impedance. It allows to tune the SiPM bias voltage in a range of 2V to equalize the sensor response.
During power gating, the bias current is decreased to sub uA - levels. Compensation methods are implemented to keep the DC voltage at the input terminal at the desired point in this mode.
The later signal processing stages consist of a trigger branch and two paths for charge integration: A high gain stage for single pixel signals, and a low gain stage spanning a large charge range.
The high gain stage uses an active integrator. For the low gain stage, passive integration using low voltage cascode mirrors is used. The signal shaping is performed using a 2nd-order filter.
The equivalent noise charge for the high gain stage is expected to be 3fC for a total input capacitance of 50pF.
The low gain stage can achieve 1% INL/FSR linearity for up to 150pC. An additional signal processing branch is used to generate a digital trigger signal for time stamping with nanosecond resolution and is used to initiate the ADC conversion.

For each front-end channel, the charge signals will be digitized by an individual ADC. To minimize the power consumption, a successive approximation registration ADC using MIM capacitor arrays is used. Design details of the ADC were already presented in TWEPP14. During normal operation, the signals are digitized with 9+1 bits resolution using a split binary capacitor array. For sensor calibration, an additional 1+7 bit pipelined stage is implemented to increase the quantization resolution.
The relatively low nominal sampling frequency of 2MHz is used effectively by the auto-triggered operation.

Two mini-ASICs were submitted, implementing one front-end, ADC channel and a digital part for ADC control and configuration.
After verification, the modules will be combined into a 36 channel mixed-mode ASIC.
We present the front-end and ADC design and show first characterization measurements of the blocks.

Primary authors: BRIGGL, Konrad (Heidelberg University); SHEN, Wei (Kirchhoff Institute for Physics)

Co-authors: SCHIMANSKY, David (Heidelberg University); SCHULTZ-COULON, Hans-Christian (Ruprecht-Karl-s-Universitaet Heidelberg (DE)); CHEN, Huangshan (Ruprecht-Karls- Universität Heidelberg); STANKOVA, Vera

Presenter: BRIGGL, Konrad (Heidelberg University)

Session Classification: ASICs

Track Classification: ASICs