The SST-1M prototype camera for the Cherenkov Telescope Array

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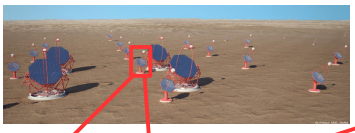
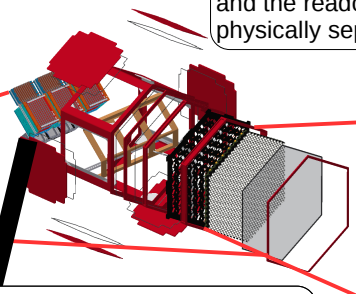
The Cherenkov Telescope Array (CTA)

1400 scientists (28 countries) propose to build an array of more than 100 telescopes deployed in two sites (North and South hemisphere) to study gamma-rays with 10 GeV < E < 300 TeV.



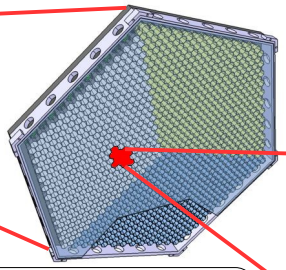
The SST-1M camera

Designed to be very compact and light (<200 kg). The photo-detection plane and the readout are physically separated.



The single mirror Small Size Telescopes (SST-1M)

Among the three types of telescopes (Large, Medium and Small size – LST, MST and SST), the SSTs are meant for covering the 5-300 TeV energy region.



The photo-detection plane

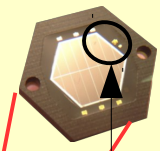
A hexagonal matrix of 1296 Silicon photomultipliers (SiPMs) coupled to hollow light concentrators, arranged on 108 modules (12 pixels each).

The Hamamatsu large area hexagonal sensor

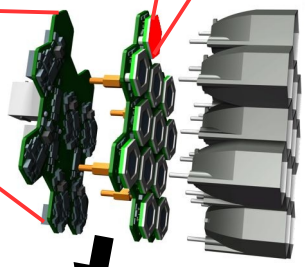
Challenge #1: we use hexagonal hollow light concentrators → we custom designed a large area (93.56 mm^2) hexagonal sensor

Challenge #2: the sensor has a high capacitance (3.4 nF) → complex fine-tuning of the preamp

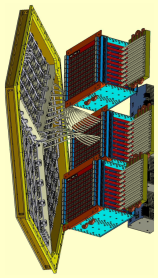
Challenge #3: we have to stabilize the operational point of the sensor → we implemented a compensation logic in the front end



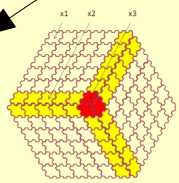
NTC temperature sensor

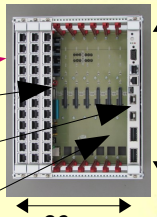


DigiCam: a fully digital readout and trigger system



3 DigiCam minicrates





9 FADC boards

1 trigger board

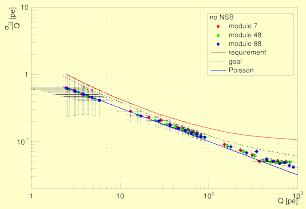
High throughput backplate

30 cm

20 cm

The photo-detection plane is divided in **3 logical sectors**. Each minicrate controls one sector.

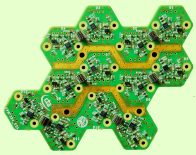
The FADC board digitizes the signals at 250 MS/s on 48 channels (4 modules). The samples are sent through high speed multi-gigabit serial links to the Xilinx XC7VX415T **FPGA**, where they are pre-processed and stored in **ring buffers**, so that the system is **dead-time free**.



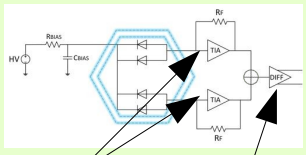
Although we use a non-linear input stage, the charge resolution of the full system complies with the CTA requirements.

The trigger board receives data from the FADC boards, resampled in sets of 3 pixels. A highly parallelized trigger algorithm implemented in the Xilinx XC7VX485T **FPGA** is applied, based on the recognition of geometrical patterns on pixels above threshold. Selected events are sent to the central system via a 10Gb fiber link.

The preAmp Board



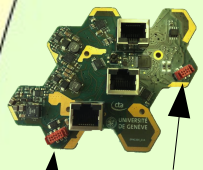
The PreAmp Board reads out the **12 pixels** of a module. The **4 channels** of each sensor are biased with a single high voltage and their signal is re-summed to provide 1 readout. The sensor is **DC coupled** to the front-end, to estimate the background light contribution from the baseline level. The board has been designed with the aim of minimizing **power consumption**.



Texas Instruments OPA846 low-noise trans-impedance

Differential output LMH6551

The Slow Control Board

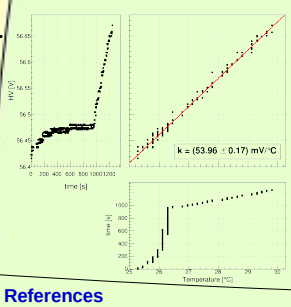


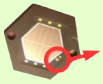
CANbus connector

Power connector

The Slow Control Board functions are:

- Route the **analog signals** from the photo-detection plane to DigiCam via 3 RJ45 connectors per module;
- Read/Set the **bias voltage** of each sensor individually;
- Read the **temperature** of each sensor individually;
- Stabilize the operational point of each sensor via the **compensation loop**.

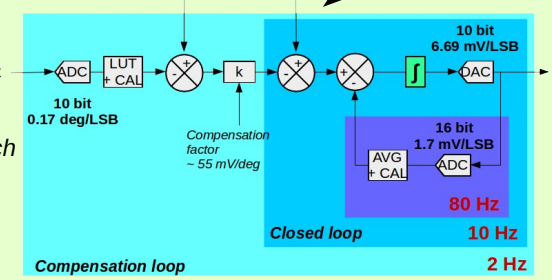




NTC

The bias voltage of each of the 1296 pixels is adjusted as a function of temperature

Implemented in μ-controller



The sensor bias voltage is updated every 0.5 s

Acknowledgements

We gratefully acknowledge support from the agencies and organizations listed under Funding Agencies at this website: http://www.cta-observatory.org/. In particular we are grateful for support from the NCN grant DEC-2011/01/M/ST9/01891 380 and the MNiSW grant 498/1/FNiTP/FNiTP/2010 in Poland and the University of Geneva and the Swiss National Foundation.

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