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A Pattern Recognition Mezzanine based on Associative Memory and FPGA technology for Level 1 Track Triggers for the HL-LHC upgrade

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The increase of luminosity at the High Luminosity Large Hadron Collider (HL-LHC) will require the main experiments to use the tracker information at Level-1 trigger system in order to maintain an acceptable trigger rate. To extract the track information at the required latency –few microseconds - a dedicated hardware has to be used. We present the tests of a prototype system based on pattern recognition mezzanine as core of pattern recognition and track fitting for HL-LHC ATLAS and CMS experiments, combining the power of both Associative Memory custom ASIC and modern Field Programmable Gate Array (FPGA) devices.

Summary

With the increase of luminosity at 5×10ˆ34 cm−2 s−1, the number of minimum bias interactions per bunch crossing will increase up to about 140, causing an unmanageable increase in the trigger rate due to background, if the thresholds are not increased. The tracker information is the key to solve this problem.

A dedicated hardware processor is hence needed to select interesting event configurations at the 40 MHz bunch-crossing rate. Currently such class of processor is provided by the Associative Memory (AM) [1] technology, already adopted in the CDF experiment [2] and recently in the ATLAS Level-2 trigger, the Fast Tracker processor [3], where a longer latency is allowed.

CMS is pursuing a vigorous R&D to demonstrate the feasibility of such an approach with state of the art AM technology embedded in ATCA board crates, and a similar approach is also studied for the ATLAS upgrade. For this purpose a prototype has been developed: the Pattern Recognition Mezzanine (PRM) at INFN. The prototype is designed to combine the pattern recognition task [1] using the new version of the AM device with the precise track fitting [4], performed by the last generation of FPGA devices, to send out the track information to the higher trigger levels within a latency of few microseconds. The PRM is a 14.9x14.9 cm2 card hosting two FMC connectors designed to satisfy the VITA 57.1 standard specification, a Kintex FPGA and 16 AM chips. The board has been first developed to host AM chips, to test the basic functionality of the serial links, even if the number of patterns stored in each chip will be modest (2,000). A second version will use a newer AM chip version (AM06) where the number of patterns per chip will be increased to 128,000.

The FPGA has the role of distributing the hits to AM chips, collecting the candidate tracks, performing a track fitting on them using different algorithms (PCA [4], Hough Transform, etc.) and then send out the results to the following trigger level. The electronics layout has been designed to reduce as much as possible the latency of the Level-1 trigger decision and to integrate all the functionalities in one single board. An external low latency memory is added to increase the data storage capability of the device, in view of possible needs by the different fitting algorithms to be tested.

A mini FMC test-board was also developed for configuration and standalone tests to check the basic functionalities of the board, such as the bit error rate of GTX serial links. The results of the first tests will be

reported.

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[2] J. Adelman et al., Nuclear Instruments and Methods in Physics Research A 572 (2007) 361–364
[3] A. Andreani et al., IEEE Trans, Nucl. Sci. 59, pp 348-357, 2012
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