# Performance of the TilePPr demonstrator for the ATLAS Tile Calorimeter Phase II Upgrade

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## ATLAS Calorimeter Phase II Upgrade

The Tile Calorimeter (TileCal) is one of the several sub-detectors which compose the ATLAS experiment at the Large Hadron Collider (LHC) at CERN. A total of 9852 photomultipliers (PMTs) are needed for the complete readout of the TileCal cells. The LHC plans a series of upgrades culminating in the High Luminosity LHC (HL-LHC) with the aim of increasing the nominal instantaneous luminosity to a value of around 5-7·$10^{34}$ $cm^{-2}s^{-1}$. A new trigger and readout architecture will be implemented in ATLAS for Phase II Upgrade. The new calorimeter trigger will use digital information and improved granularity requiring the complete redesign of the front-end and back-end electronics. The new front-end electronics will transmit readout data at the LHC frequency to the first element in the back-end electronics: the Pre-Processors (TilePPr). The TilePPr will provide an interface path for the readout, configuration, control and monitoring of the front-end electronics, and will send pre-processed data to the ATLAS Level 0 trigger system for trigger decision.

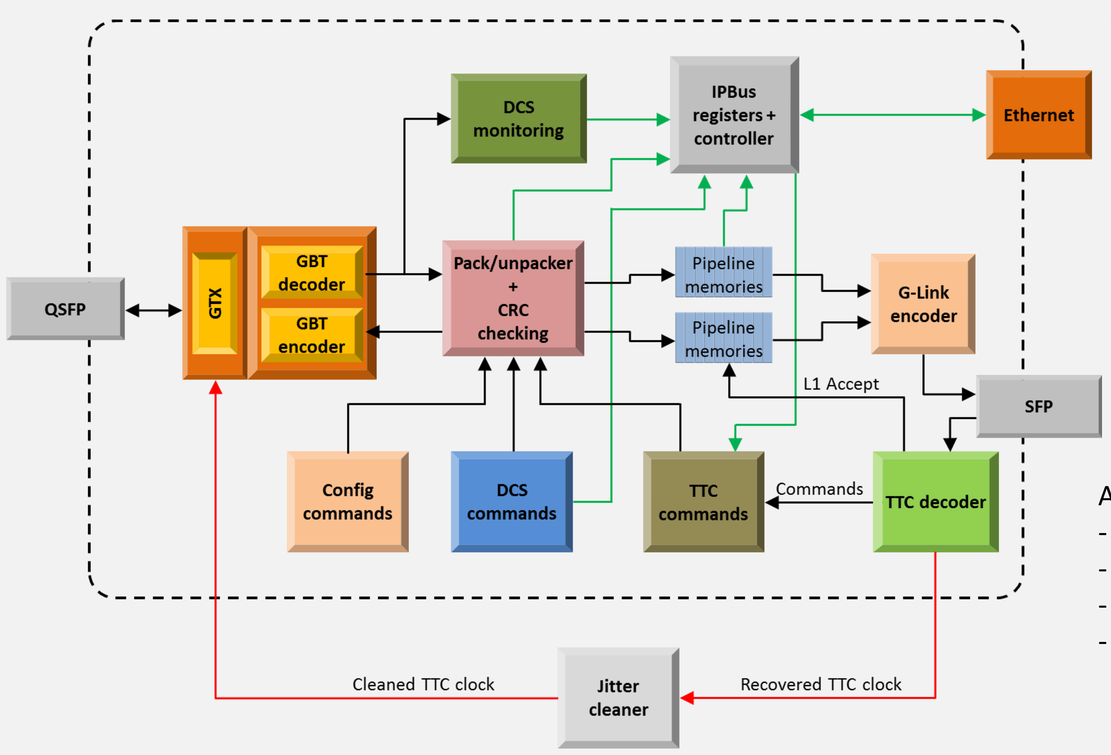
| | Present | Phase II |
|---|---|---|
| Total BW | ~205 Gbps | ~80 Tbps |
| N. fibers | 256 | 8192 |
| BW/module | 800 Mbps | 320 Gbps |
| Nb. boards | 32 | 32 |
| Nb. crates | 4 (VME) | 4 (ATCA) |

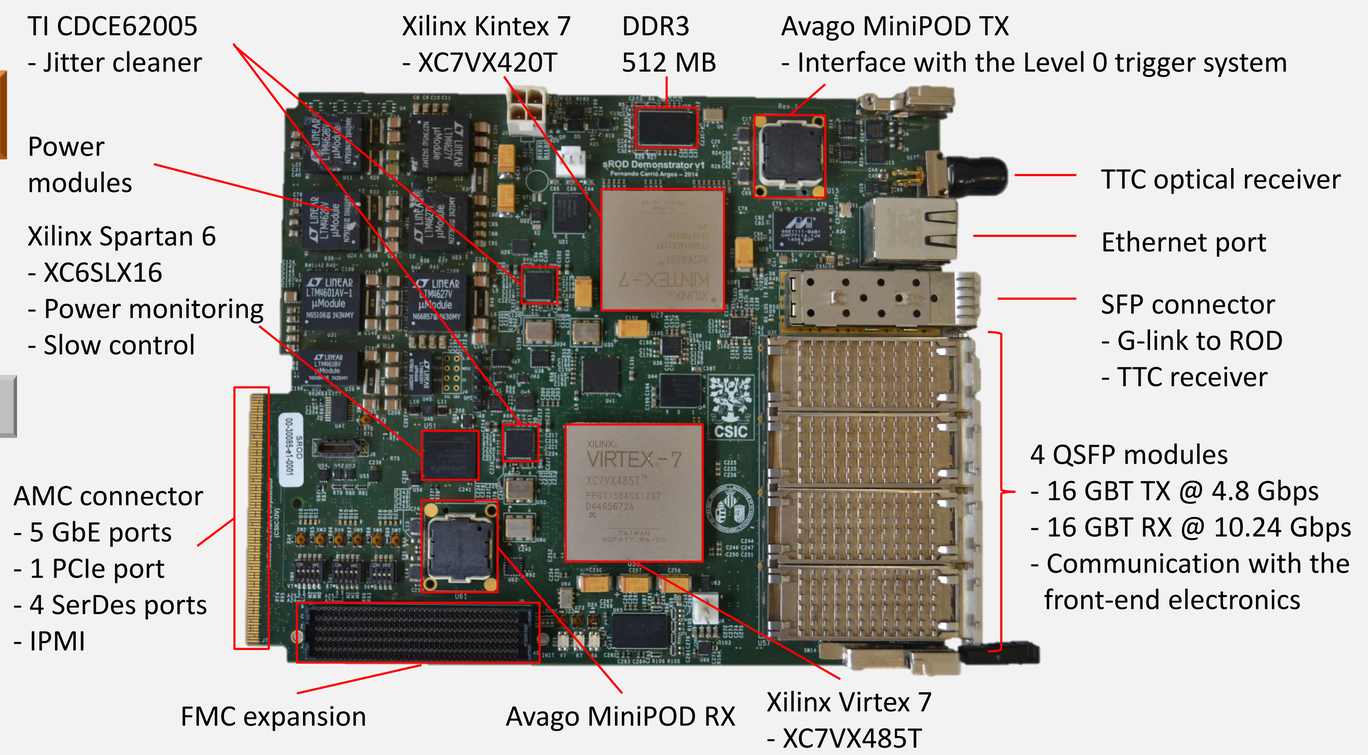
*TileCal readout features comparison*

## TilePPr prototype

The TilePPr prototype has been designed in the framework of the TileCal Demonstrator, which aims to validate the performance of the new readout electronics and trigger system designs before the complete replacement of the system for Phase II Upgrade. It can operate one TileCal module (48 PMTs), representing 1/8 of the final TilePPr module.

Four QSFPs connected to the Virtex 7 FPGA are used to read-out and operate the Tilecal module. Asymmetric GigaBit Transceiver (GBT) links are implemented for the communication with the front-end electronics. Detector Control System (DCS) commands and Timing, Trigger and Control (TTC) information are encoded and transmitted at a data rate of 4.8 Gbps while readout data are received and decoded at 10.24 Gbps. The data are stored in circular pipeline memories while waiting for the trigger decision. Once the trigger acceptance signal has been received the selected events are copied to the derandomizer buffers, packed and sent to the present Read-Out Drivers (RODs) in order to keep backward compatibility with the current system. TTC information is deserialized and extracted in the Virtex 7 using GTX transceivers configured for fixed and deterministic latency operation. The recovered TTC clock is cleaned using an external jitter cleaner chip which drives the GTX transceivers for the communication with the front-end electronics synchronously with the LHC clock. All the data flow and control of the TilePPr is implemented over an Ethernet network using the IPBus protocol. The interface with the Level 0 trigger system will be implemented through an Avago MiniPOD TX which is connected to the Kintex 7 FPGA. A Spartan 6 FPGA performs slow control functionalities as clocking configuration, status monitoring and power consumption measurements.



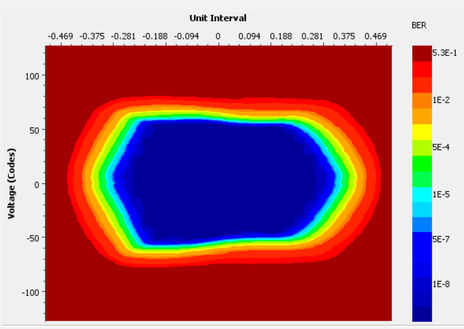




The TilePPr board has been designed in a double mid-size AMC form factor which can be operated in a ATCA carrier or in a µTCA crate. The PCB stack-up is a 16 layer design based on NELCO 4000-13 SI dielectric material to get low losses at high frequency, where 8 layers are dedicated for power and ground planes and 8 layers for signals. The total PCB thickness is 1.6 mm, compliant with the AMC standard.

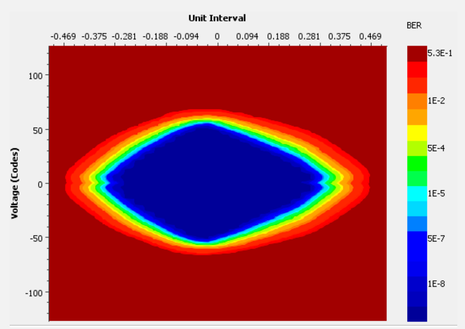
## Status

The first TilePPr prototypes have been designed, produced and evaluated as part of the TileCal demonstrator project. Xilinx IBERT IP core has been implemented for signal integrity validation of the QSFP lines using an external optical loopback. During the BER tests, no errors were observed on sixteen links running at 10.24 Gbps with a PRBS-31 data pattern over a period of 54 hours, which corresponds to a BER ≤ 9.5·$10^{-17}$ with a confidence level of 95%. Firmware has been developed using a Xilinx VC707 evaluation board and has been migrated to the TilePPr showing promising results. It includes all the functionalities to operate and read-out the TileCal demonstrator module using asymmetric GBT links (4.8 Gbps / 10.24 Gbps) where the clock domain crossing between transmission and reception is performed using internal dual clock FIFO memories. A set of C++/Python scripts allows remote operation of the TilePPr through the GbE ports using the IPBus for monitoring, data taking and calibration. Different tests are now available as pedestal stability, pedestal linearity, high voltage stability or calibration tests using charge injection pulses.

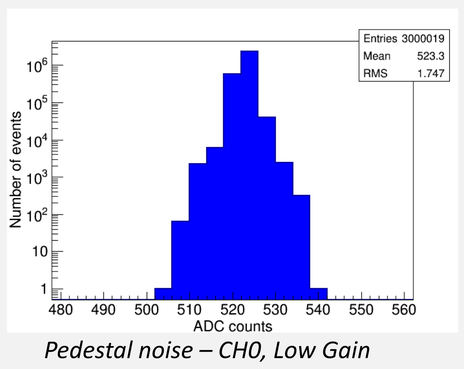
The TilePPr will be used for the evaluation of the new readout architecture in the test-beam campaigns during 2015-2016 and for the operation of the new electronics which will be inserted in the ATLAS detector at the end of 2016.



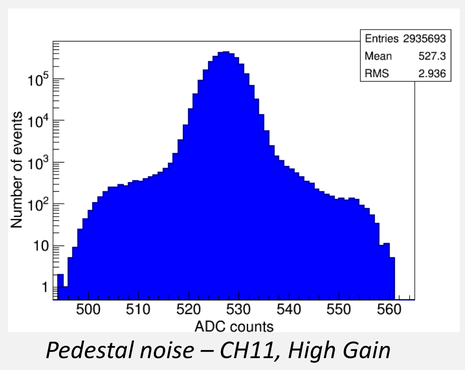

*Eye diagram at 4.8 Gbps*




*Eye diagram at 10.24 Gbps*




*Pedestal noise – CH0, Low Gain*




*Pedestal noise – CH11, High Gain*

*Poster presented at TWEPP 2015, Topical Workshop on Electronics for Particle Physics – Lisbon, Portugal*