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Performance of the sROD demonstrator for the ATLAS Tile Calorimeter Phase II Upgrade

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The super Read Out Driver (sROD) demonstrator is a high performance double AMC board based on FPGA resources and QSFP modules. This board has been designed in the framework of the ATLAS Tile Calorimeter (TileCal) Demonstrator Project for the Phase II Upgrade as the first stage of the off-detector electronics. The sROD demonstrator has been conceived for receiving and processing the data coming from the on-detector electronics of the TileCal Demonstrator module, as well as for configuring it. Moreover, the sROD demonstrator handles the communication with the Detector Control System to monitor and control the on-detector electronics.

Summary

The Tile Calorimeter (TileCal) is one of the several subsystems which compose the ATLAS experiment at the Large Hadron Collider (LHC) at CERN. Plans for the Phase II Upgrade comprise the complete redesign of the on- and off-detector electronics including the implementation of a new readout architecture with a full digital trigger system and continuous data transfer between the on- and off-detector. The total bandwidth needed to read out the complete detector will increase from ˜165 Gbps to ˜80 Tbps.

The Demonstrator Project aims to evaluate and qualify the proposed readout architecture before its full replacement during the Long Shutdown 3 (2023-2024). The new system will be validated using beam tests at CERN this year. In the upcoming years a super-drawer demonstrator with the new electronics will be installed in the ATLAS detector.

The super Read Out Driver (sROD) demonstrator is the first element of the off-detector electronics and represents 1/8 of the final sROD for the Phase II. This board is not only responsible for the reception and processing of the detector digital data, but also for the reception and distribution to the on-detector electronics of Trigger Timing and Control (TTC) signals. The sROD demonstrator also interfaces with the Detector Control System for configuring and monitoring the on-detector electronics.

The first prototypes of the sROD demonstrator have been produced. This module has been design on a double mid-size AMC format which can be operated in an ATCA carrier or a µTCA shelf.

The sROD demonstrator is populated with 4 QSFPs connected to the Virtex 7 FPGA for the readout and communication with the on-detector electronics. The readout architecture for the demonstrator requires the implementation of 16 GBT links per TileCal module with an asymmetric bandwidth which receive continuously digitized data from the on-detector electronics at 10.24 Gbps per link, and transmit configuration and control commands to the on-detector electronics at 4.8 Gbps per link. The received data is stored in pipeline memories upon the reception of a Level-1 Accept signal when the data is packed and transferred to the present RODs through an SFP connector. In parallel, reconstruction algorithms for the Phase II will be running in the Virtex 7 FPGA for evaluation purposes.

The SFP connector also receives and distributes the TTC signals to the Kintex 7 and Virtex 7 using dedicated firmware.

This prototype also includes an Avago MiniPOD transmitter which is connected to the GTX transceivers of the Kintex 7 providing data rates up to 120 Gbps. The Kintex 7 FPGA is intended for the evaluation of new trigger

algorithms, as well as for testing different options for the communication with the future L0/L1 calorimeter trigger system.

This contribution shows a detailed description of the hardware and firmware developments, and also presents the first results with the sROD demonstrator during the commissioning of the TileCal Demonstrator module.

Primary author: TILECAL SPEAKERS COMMITTEE, Atlas (CERN)

Presenter: CARRIO ARGOS, Fernando (Instituto de Fisica Corpuscular (ES))

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