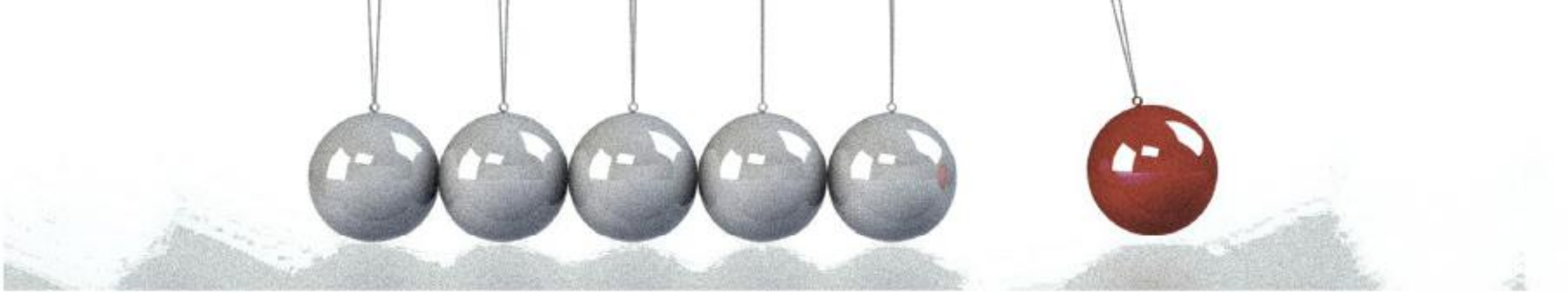

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First Performance Results of the ALICE TPC RCU2

Chengxin Zhao

University of Oslo, Norway

On behalf of the ALICE TPC collaboration

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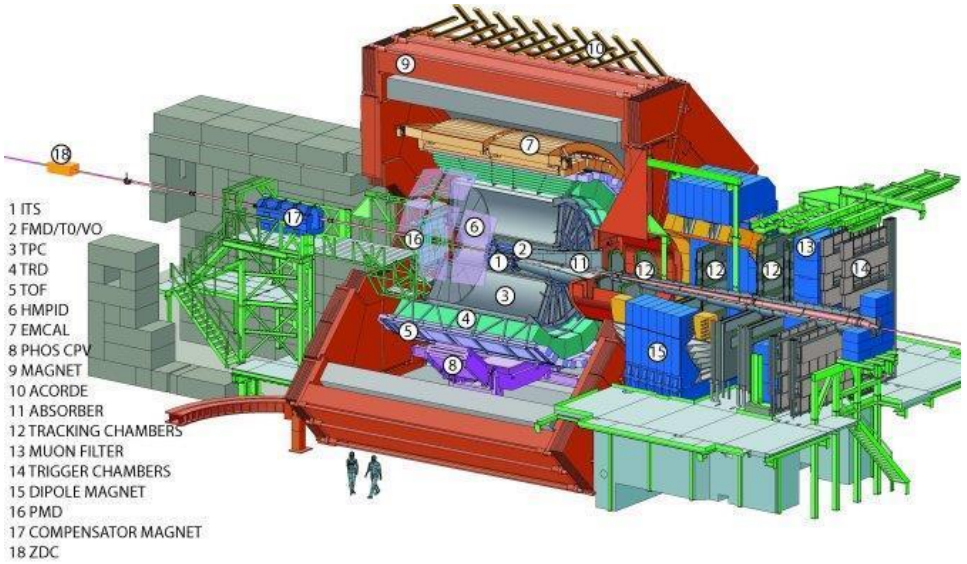
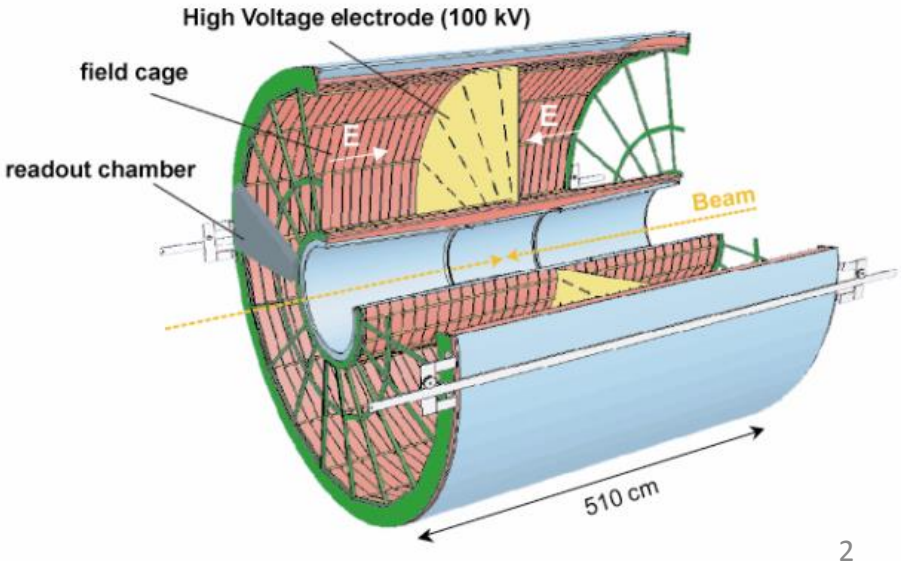
The ALICE TPC Readout electronics

- **ALICE TPC Readout electronics**
  - 557568 detector pads divided between the two end-plates.
  - 4356 Front-end cards (FEC)
  - 216 Readout Control Units (RCU)
  - Each RCU connects to 18 to 25 FECs



- **In LHC RUN2**
  - Pb-Pb collision rate is increased from 3kHz to 20kHz → **Higher Readout Speed needed!**
  - Expected radiation flux increased from 0.8kHz/cm^2 to 3kHz/cm^2 → **Improved Radiation tolerance required!**



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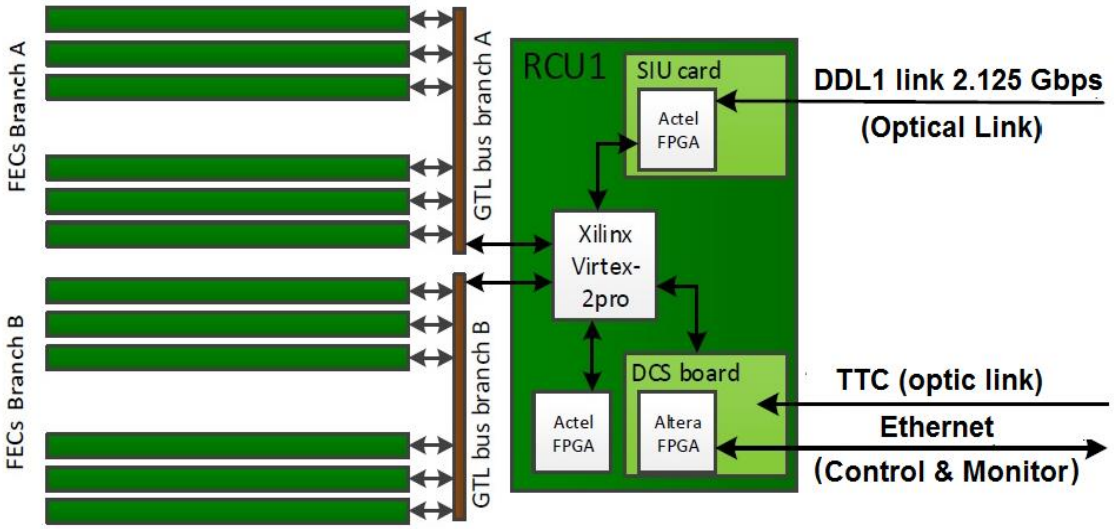
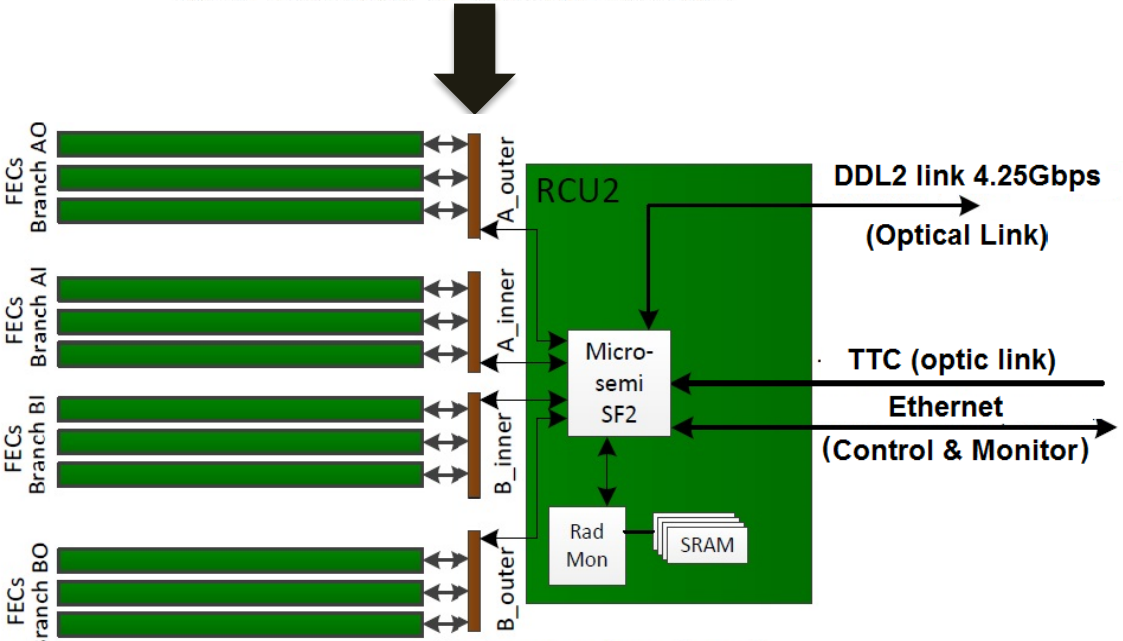
RCU1 to RCU2

- **Two branches → Four branches**
- **Detector Data Link (DDL) with higher bandwidth:**
  - DDL1@2.125Gbps → DDL2@4.25Gbps
- **3 PCB boards → 1 PCB board**
- **Four FPGAs -> One FPGA:**
  - Two Flash based FPGAs and two SRAM based FPGAs in RCU1
  - Microsemi Smartfusion2 Flash based FPGA in RCU2
- **Detector pad row based readout scheme**
  - Utilize the parallelism of RCU2 hardware structure



RUC1 readout electronics sketch



RCU2 readout electronics sketch

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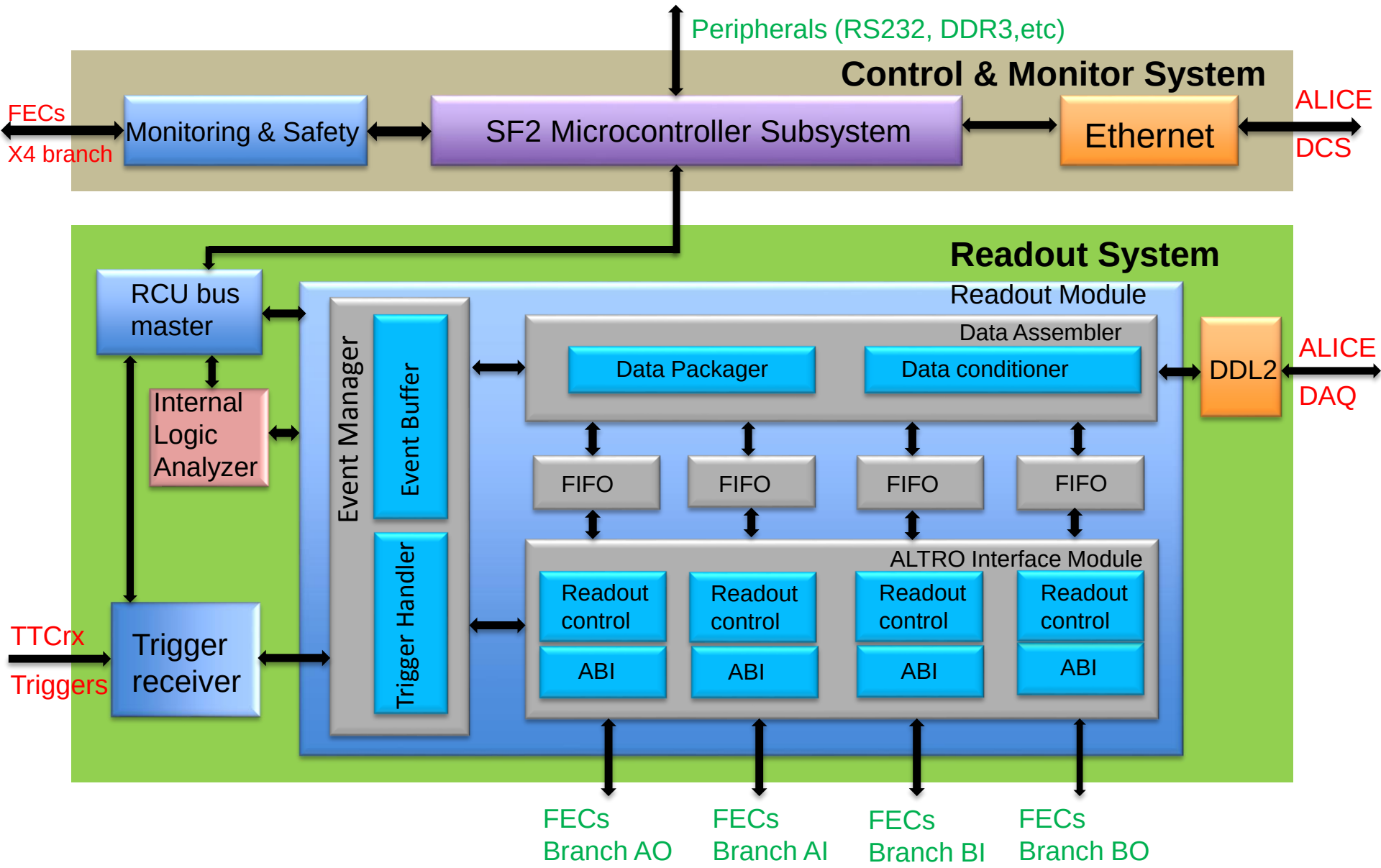
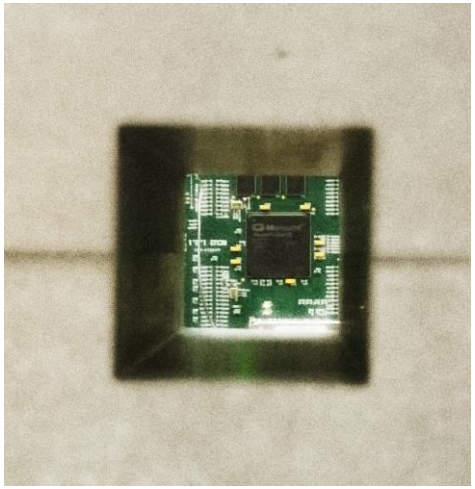
System overview of RCU2



System Irradiation Test

- System Irradiation Campaign @ TSL Uppsala
  - 170 MeV Protons
  - 28 – 29 April 2015
  - Irradiation test of the RCU2 with all surrounding systems (Trigger, DCS & DAQ) in place.



- The focus in this presentation are:
  - Readout stability
  - Linux system Stablity
  - Trigger Interface stability
  - Ethernet stability

- The test results are presented as follows:
  - Cross Section for the different tests have been calculated
  - **Mean Time Between Failure (MTBF)** for LHC RUN2 has been calculated, assuming (Worst Case):
    - >20MeV Hadrons: 3.0 kHz/cm^2 *
    - 216 RCUs
    - 4356 FECs

* Preliminary number for Run 2 inner partitions.

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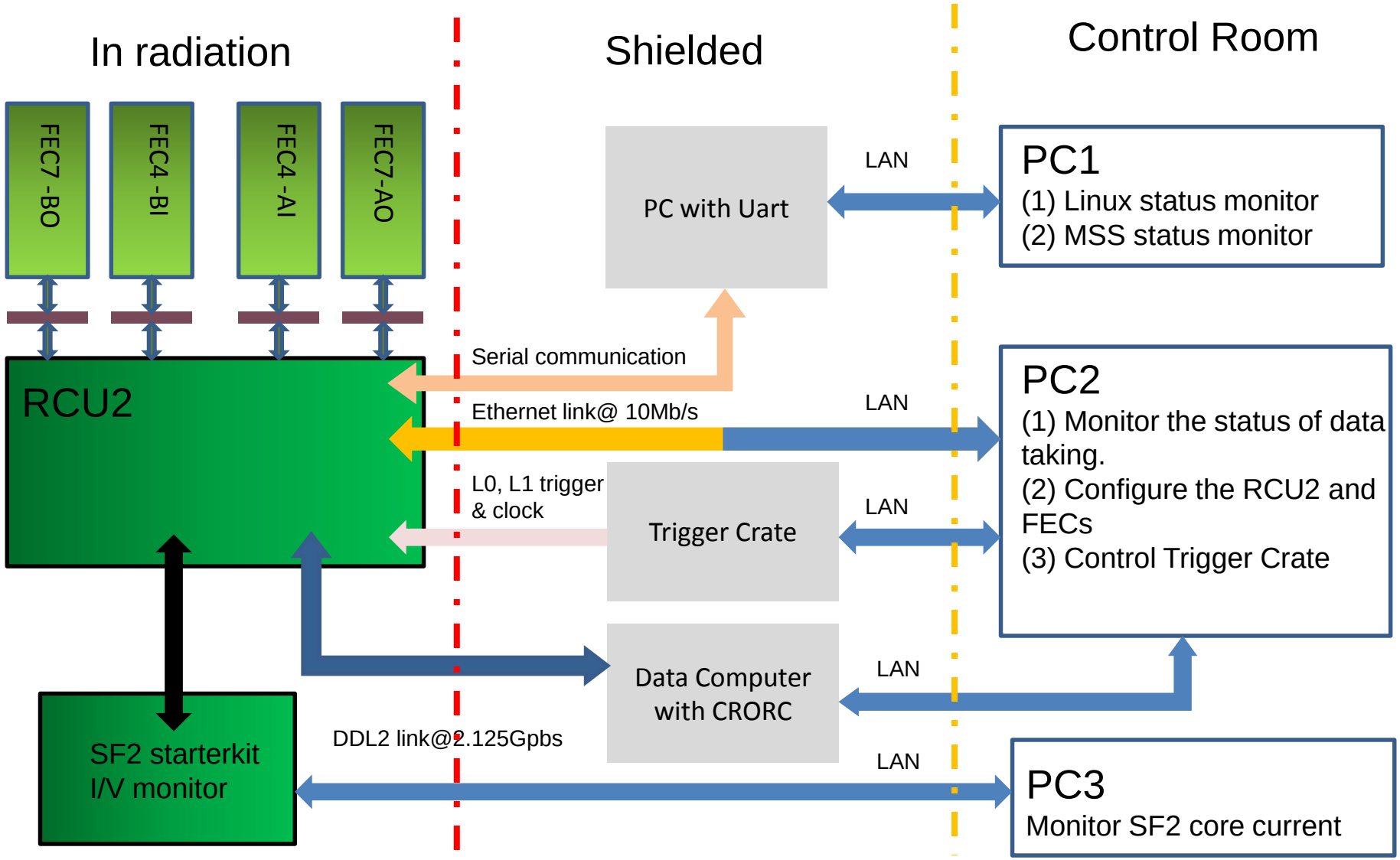
Irradiation Test Setup I



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Irradiation Test Setup II

Readout Stability - Observations

	PLL lose lock	*FEC error RCU2 irradiated*	*FEC error SF2 irradiated*	*Data transmission error RCU2 irradiated*
Cross-section	8.8E-11 ±38% (7 errors)	3.9E-11±71% (2 error)	3.6E-11±100% (1 error)	2.0E-11±100% (1 error)
Mean Time Between Failure in RUN2	4.9 ±1.8 hours	0.5 ±0.4 hours	0.6 ±0.6 hours	21.4 hours±21.4 hours

- Irradiated the whole RCU2 and only SF2 (using collimator)
  - FECs are always irradiated.
    - Note: collimator shields also the FECs
- Data taking was monitored with trigger rate@10Hz.
  - Readout stopped several times.
- Three categories of errors lead to the stops of data taking:
  (1) Reset due to PLL lose lock
  (2) SEUs induced error on FECs.
  (3) Data transimission error*
- **No scenario that can be interpreted as a FPGA fabric error has been seen.**

*Data transimission error was observed only when complete RCU2 is irradiated

Mitigation – Reset Strategy

- In SF2, PLL lock has three options:

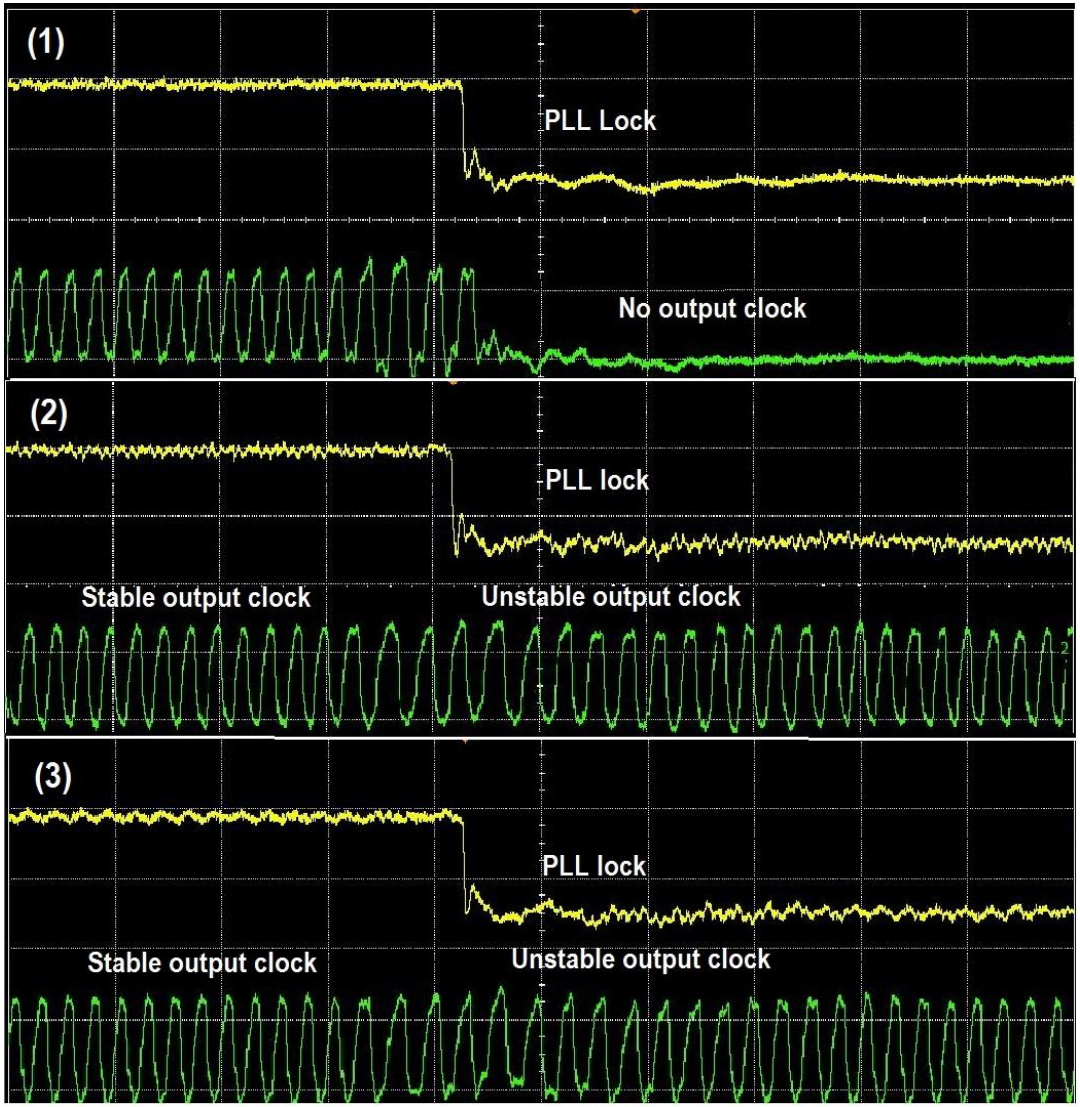
(1) PLL hold reset before get lock

(2) PLL output before lock and do NOT synchronize after getting lock

(3) PLL output before lock and synchronize after getting lock

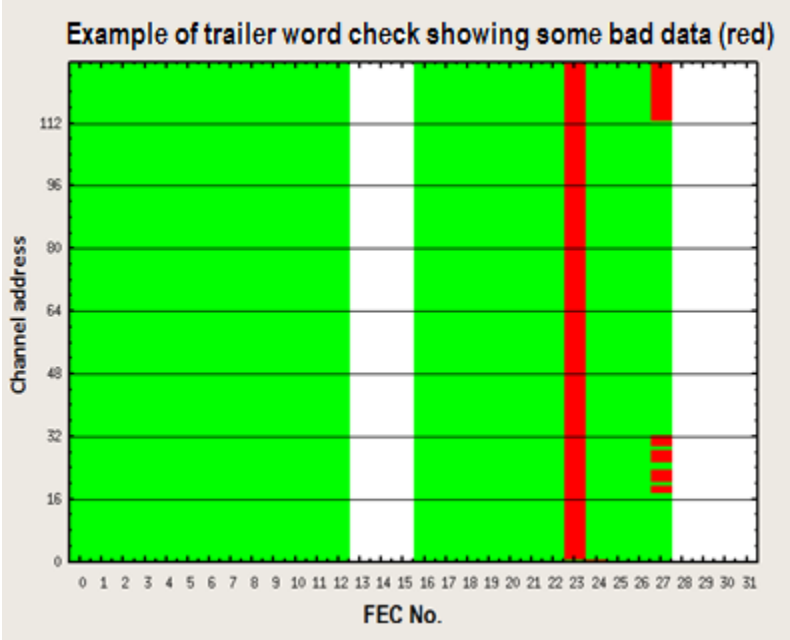
- PLL clock is not realiable when it loses lock -> Minimize the use of PLL.
  - Can not fully avoid the use of PLLs

- Reset strategy has been redesigned following irradiation test
  - Reset no longer depends on PLL lock signal after power on.



Mitigation - FEC, DDL & Fabric

- **SEUs induced error on FECs -> The following error handling are implemented:**
  - Front-end bus on the FECs are continuously monitored.
  - Communication between the RCU2 and FECs are monitored.
  - Trailer word of each data package, which contains the infomation like channel address, length of data, etc, is verified.
  - **Purpose: Detect (& possibly correct) error situations early**



- **Data Transmission error**
  - ALICE DAQ enters in Pause and Recover (PAR) state if there is some data transmission error so that the physics run does not need to stop.
  - The PAR scheme is to be supported by the RCU2.
  - **PAR is also a solution to FEC induced erros.**

- **Fabric errors**
  - Critical locations in the design will be considered for TMR or hamming protection

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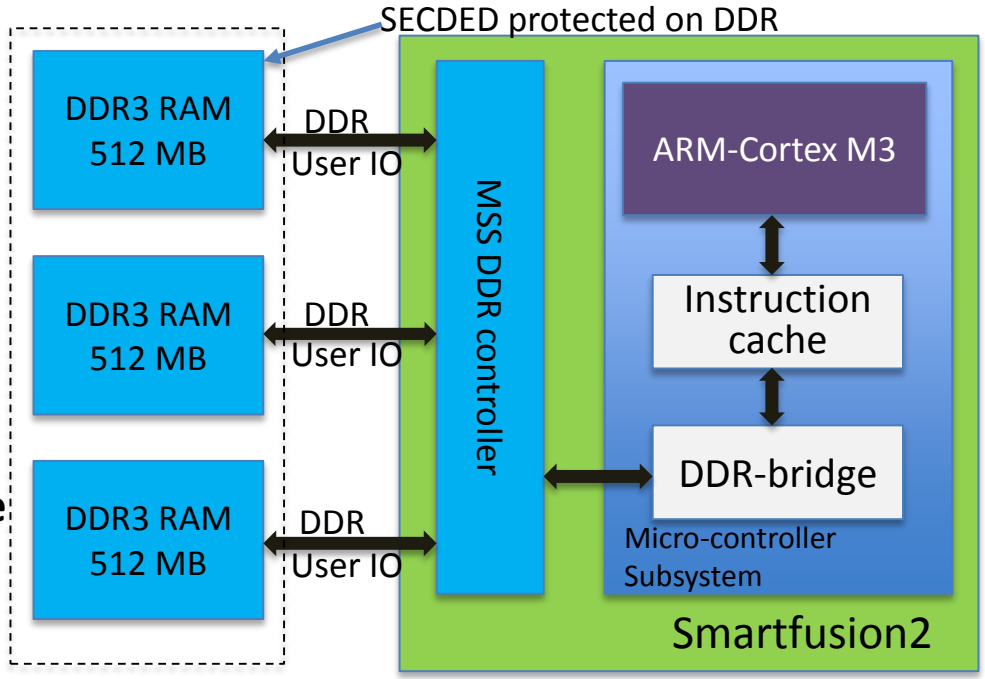
Linux Stability - Observations

- **Irradiated RCU2 and SF2 only**
  - DDR3 memory protected by SECDED, which could enabled/disabled manually
- **Two kind of errors observed:**
  - Linux rebooting
  - Linux frozen
- **Estimantion of Mean Time Between Failure (MTBF) in RUN2 is based on the WORST CASE environment**
- **SECDED on MDDR will most likely not help**
  - Awaiting response from Microsemi



	RCU2 irradiated MDDR SECDED OFF	*ONLY SF2 irradiated MDDR SECDED OFF*	*ONLY SF2 irradiated MDDR SECDEC ON*
Cross-section (reboot)	5.04E-10±22% (20 errors)	2.57E-10±38% (7 errors)	2.48E-10±50% (4 errors)
MTBF in RUN2 (reboot)	0.9 ± 0.2 hours	1.7 ± 0.6 hours	1.7 ± 0.9 hours
Cross-section (frozen)	1.26E-10 ±45% (5 errors)	1.10E-10±58% (3 errors)	0.5E-10 ±100% (1 error)
MTBF in RUN2 (frozen)	3.4 ± 1.5 hours	3.9 ± 2.3 hours	8.6 ± 8.6 hours

Linux Stability - Mitigation

- **Possible reasons of Linux reboots and Linux freeze:**

- Single-event upsets (SEUs) and multi-bit upsets (MBUs) in the DDR memories which leads to Linux Kernel panic
- SEUs (and MBUs) in the ARM processor

- **Actions taken to improve RCU2 stability:**

- Stand-alone module for DDL2 SERDES initalizing.
  - Default is initializion by MSS on System boot-up
- Configuration of the FECs/ALTROs via the DDL2
- *Ongoing:*

(1) Exploring Linux replacement

- freeRTOS that ONLY resides on the internal eSRAM in the SF2

(2) Exploring the proper use of SECDED on MDDR

Some Other Observations

- Trigger Reception (TTCrx) is stable: *no error was seen*
- Monitoring and Safety Module is stable: *no error seen on RCU2 side*
- Ethernet is stable
  - Two errors observed → cross-section = 2.52E-11 ±71%.
  - Mean Time Between Failure (MTBF) in RUN2 is 17.0±12.1 hours

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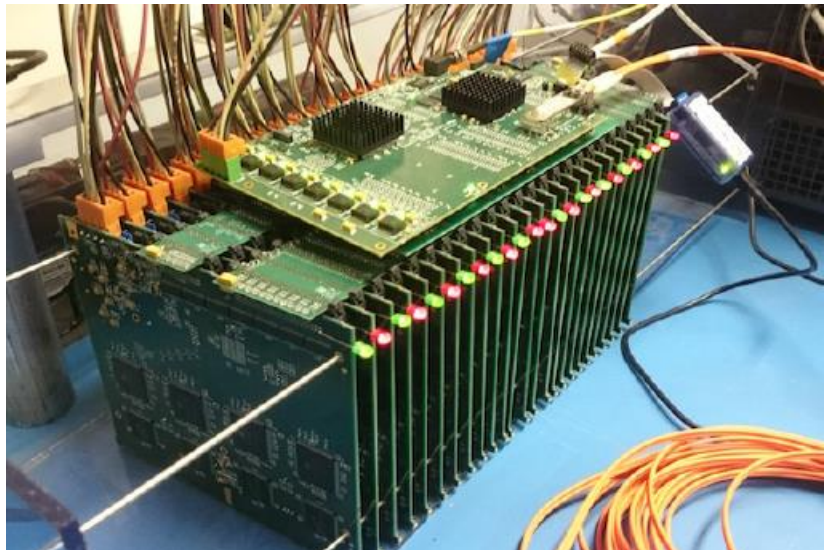
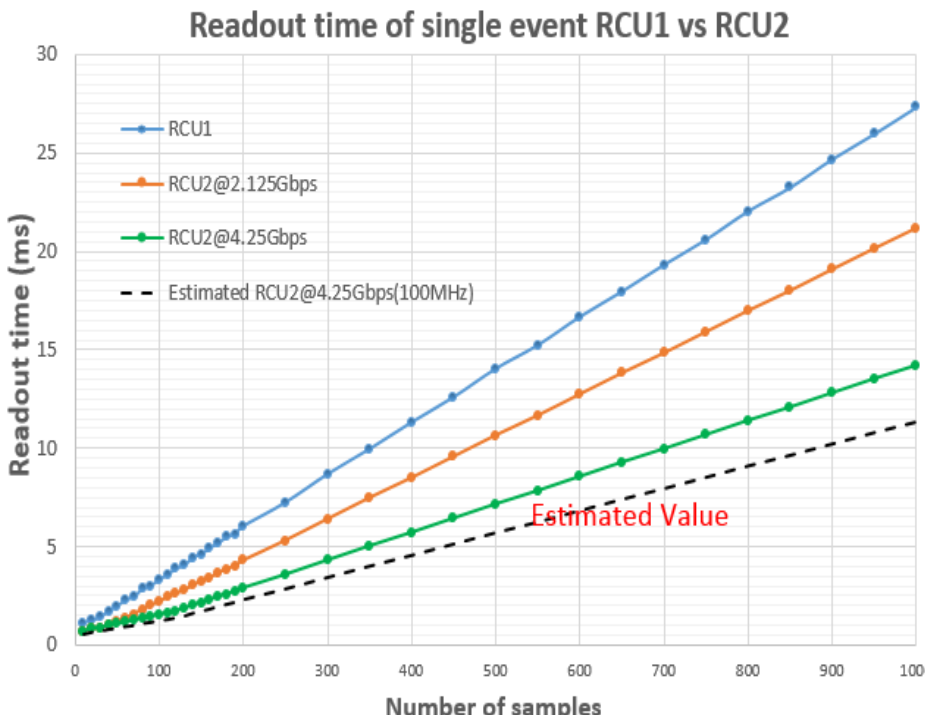
Readout Speed

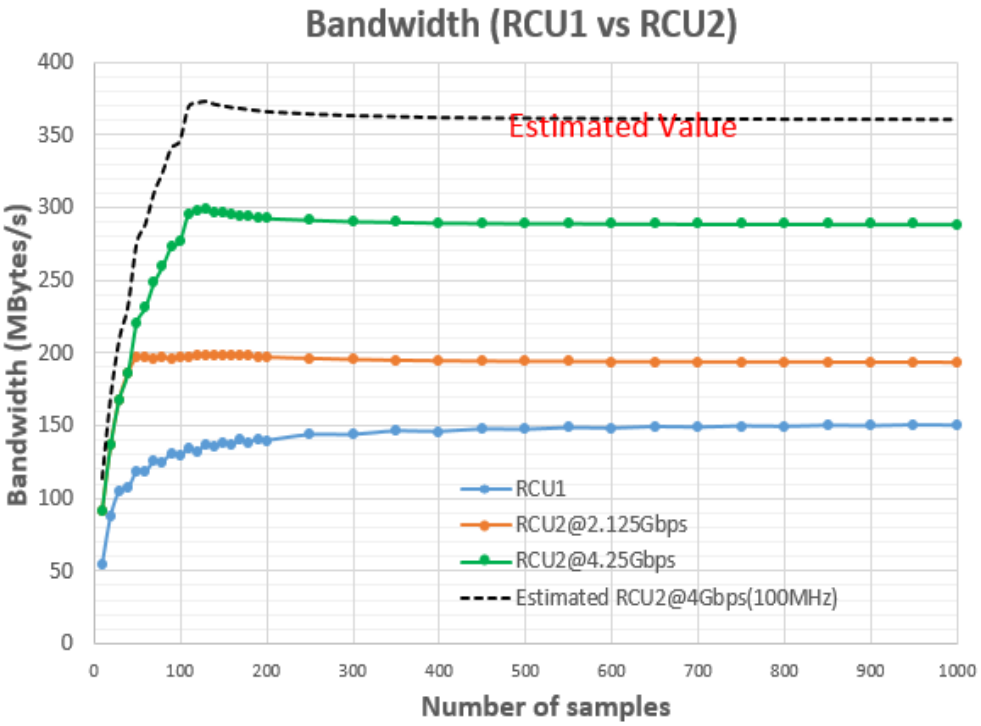
- **One full readout partition with 25 FECs used for test**
- **DDL link@2.125Gbps**
  - DDL link saturated from number of samples set to be ~50
- **DDL link@4.25Gbps**

– Readout Unit@80MHz → Speed improved with a factor of ~2

– Readout Unit@100MHz → Speed wil be improved with a factor of ~ *2.6*







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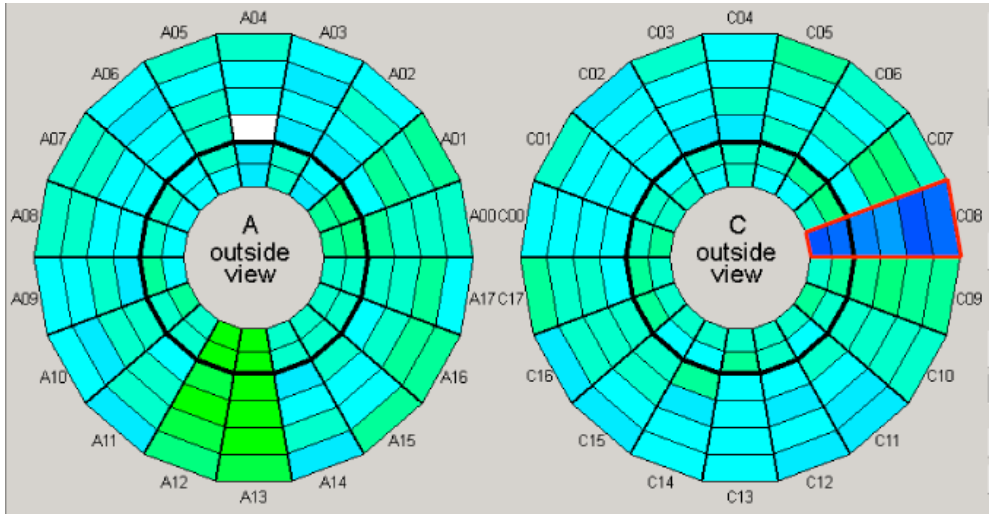
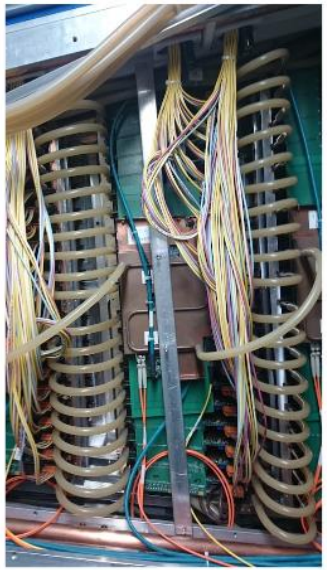
RCU2 Commissioning





- **240 RCU2 boards have been produced**
- **6 boards have been installed and commissioned since Jan. 2015**
- **Trigger reception is stable**
- **Readout with DDL@2.125Gbps is stable**
  - No corrupt data observed.
  - No readout stop has been observed.
- **No linux reboot/frozen has been observed.**
  - ~10 reboots were observed on 210 RCU1s
  - Statistics too low to draw any conclusion
- **Monitoring & Safety Module is stable**
- **Ethernet is working stable**
- **ISP programming works**
  - Stops prematurely 10-15 % of the times
  - Retry always works

RCU2 FPGA Design Ongoing

- Readout system plans:
  - Integration and verification of DDL@4.25Gbps
  - Increase the sys clock frequency from 80MHz to 100MHz
    - External Oscillator is 100 MHz – avoid use of PLLs.
  - Implement data sorting algorithm (for High Level Trigger)
  - Implement handling of triggers for Multi-Event-Buffering.
- Test & benchmark:
  - Additional benchmark counters and pattern generators at various points in the firmware.

Conclusions

- **RCU2 System irradiation campaigns have been performed**
  - It revealed some stability issues, especially regarding Linux and Readout
  - All the radiation related problems have so far been solved or planned with mitigation actions.
- **With the DDL2@4.25Gbps and System Clock @100Mhz, the readout speed will be improved with a factor of ~2.6 compared to the RCU1.**
- **The RCU2 with DDL2@2.125Gbps has been verified to be working stable at TPC.**
  - integration and verificaion of DDL2@4.25Gbps is onging
- **FPGA Fabric Design is in finalizing phase**
- **Installation is scheduled for the Winter Break (Dec 2015 – March 2016)**

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Thanks for Listening

- RCU2 team *(no particular order)*:

  Chengxin Zhao (chengxin.zhao@fys.uio.no) – *University of Oslo, Norway*

  Johan Alme – *Bergen University College, Norway*

  Harald Appelshäuser, Torsten Alt, Stefan Kirsch – *Goethe University Frankfurt, Germany*

  Lars Bratrud, Jørgen Lien, Rune Langøy – *Vestfold University College, Norway*

  Fillipo Costa – *CERN, Switzerland*

  Taku Gunji, Yuko Sekiguchi – *University of Tokyo, Japan*

  Tivadar Kiss, Ernö David – *Cerntech, Budapest, Hungary*

  Christian Lippmann– *GSI Darmstadt, Germany*

  Anders Oskarsson, Lennart Osterman – *University of Lund, Sweden*

  Ketil Røed – *University of Oslo, Norway*

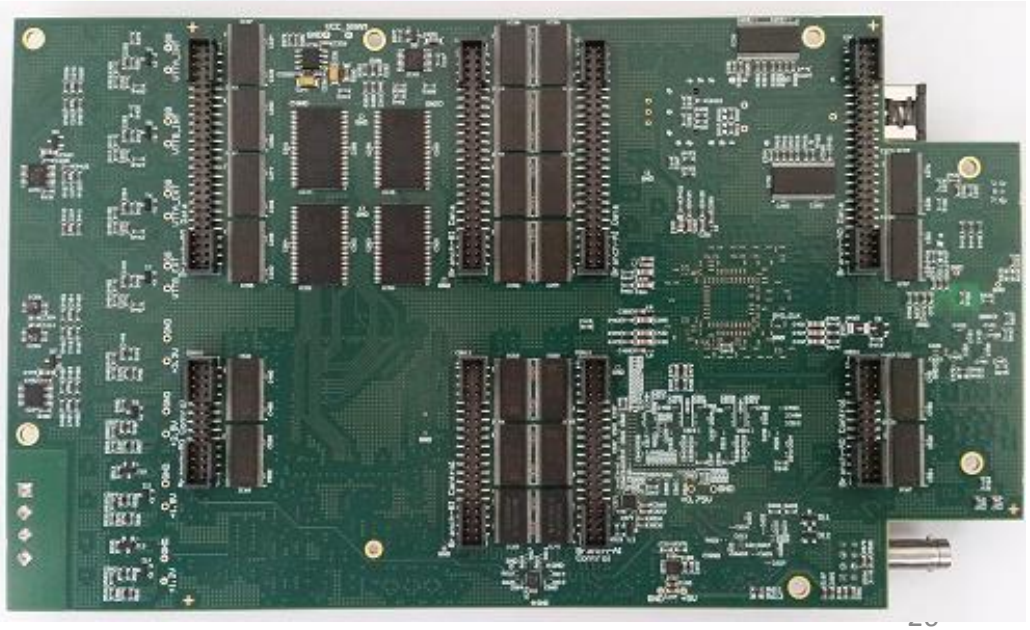
  Attiq Ur Rehman, Kjetil Ullaland, Dieter Röhrich, Shiming Yang, Arild Velure – *University of Bergen, Norway*

  Meghan Stuart, Andrew Castro – *University of Tennesse*

- Backup Slides

Status of RCU2

- **240 RCU2 boards have been produced**
  - 216 boards for installation
  - 24 for testing and backup
- **6 boards have been installed and commissioned at one out of the 36 TPC Sectors since Jan. 2015**
- **System irradiation campaign**
  - April 2015 at TSL laboratory
- **Linux and Firmware are in the finalizing phase**
- **Remotely monitoring and upgrading of the RCU2 in place**
- **Installation planned in LHC winter break**
  - Between Dec. 2015 and March 2016



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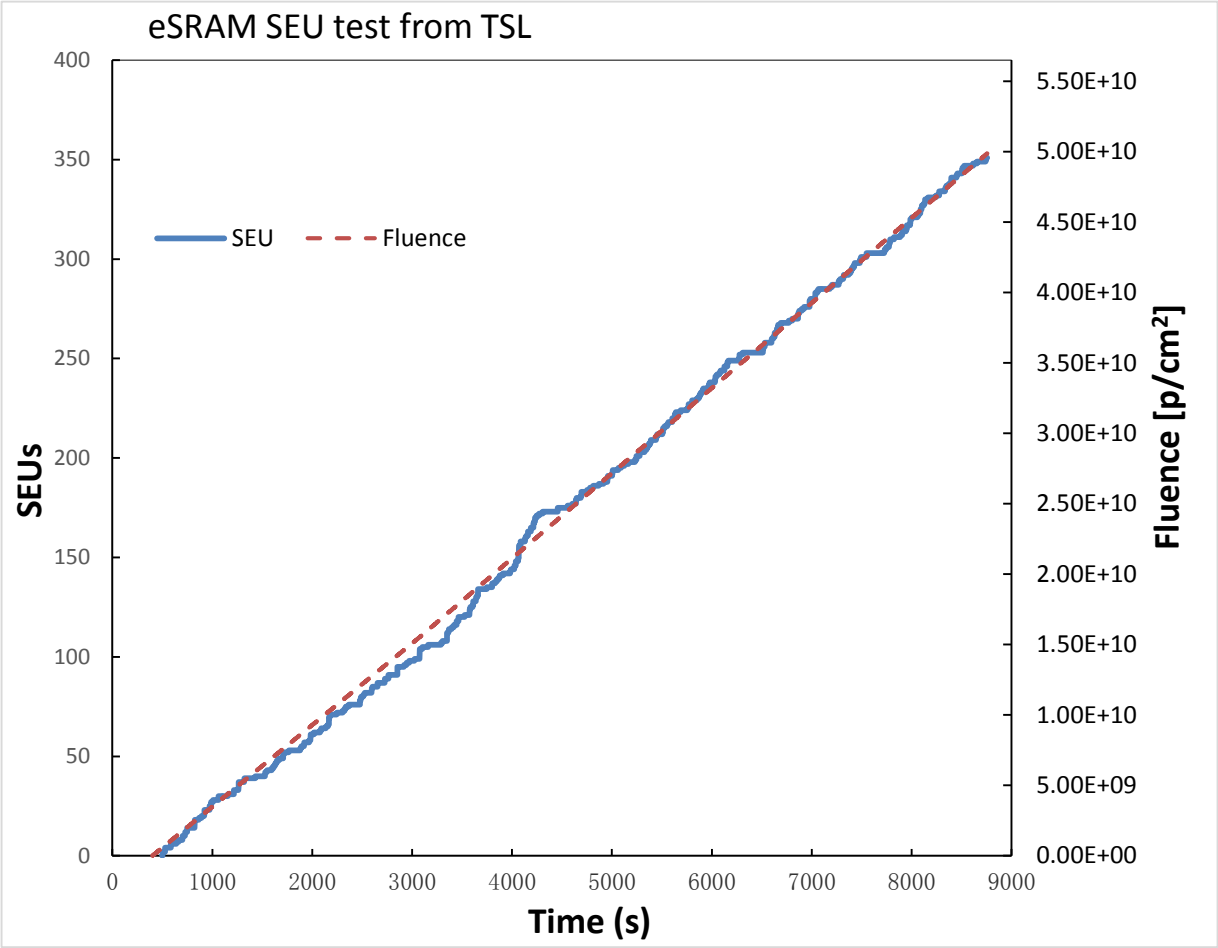
SF2 eSRAM Tests

- **Smartfusion2 MSS has two eSRAM memories**
  - size of each of is 256 Kbits
  - SECDED can be enabled/disabled manually
- **Test were performed on eSRAM_1:**
  - Write a pattern to all eSRAM_1 locations.
  - SECDED mechanism stores the number of 1-bit and 2-bit errors into the error counter registers.
  - Read the register of error counter every second.



	SF2 eSRAM (single eSRAM per RCU2)
Cross section [cm^2/bit]	2.70E-14 ±5% (352 errors)
Mean Time Between SEUs in RUN2	219±11 seconds