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First Performance Results of the ALICE TPC RCU2

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This paper presents the first performance results of the ALICE TPC Readout Control Unit2 (RCU2). With the upgraded hardware typology and the new readout scheme in FPGA design, the RCU2 is designed to achieve twice the readout speed of the first RCU. Design choices such as using the flash-based Microsemi Smartfusion2 FPGA and applying mitigation techniques in interfaces and FPGA design ensure a high degree of radiation tolerance. This paper presents the system level irradiation test results as well as the first commissioning results of the RCU2. Furthermore, it will be concluded with a discussion of the planned updates.

Summary

The ALICE Time Projection Chamber (TPC) consists of 4356 Front-end cards (FECs), which are controlled by 216 Readout Control Units (RCU). Each RCU connects to between 18 and 25 FECs using a multi-drop parallel Gunning Transfer Logic (GTL) bus. In LHC RUN1, the readout speed is limited by this parallel bus structure. In addition, instabilities due to the radiation environment have been observed. In LHC RUN2, the interaction rate of Pb-Pb collision is increased from 3kHz to 20kHz and the expected radiation flux is increased from 0.8kHz/cm2 to 3kHz/cm2. This implies requirements of higher readout speed and improved radiation tolerance on the RCU. Therefore, the Readout Control Unit 2 (RCU2) is designed.

For the RCU2, each GTL bus is split into four branches instead of two branches as was the case for the RCU1. This provides at least twice the readout speed of RCU1. Correspondingly, the data rate of DLL bus is increased from 1.28Gbps to 4.2Gbps. In order to utilize the improved parallelism of RCU2 hardware, a new readout scheme in FPGA is currently being implemented, where the data is ordered after the physical location of the pad and the padrow. The pad is essentially the sensoring element in the TPC detector. To provide the improvement in data rate, the FPGA design requires several different clock domains, which increases the complexity with regard to the RCU1 design.

The FPGA on the RCU2 is the Microsemi Smartfusion2 (SF2) SOC FPGA, where the configuration is stored in Single Event Upset immune flash cells. Additionally, several of the interfaces on the SF2, such as the Ethernet and the DDR interface, are protected by mitigation techniques in the hardware. The RCU2 have been through several irradiation campaigns at The Svedberg Laboratory (TSL) in Uppsala, and the results on the final version of the RCU2 hardware have so far been promising. A new irradiation campaign has be performed in April 2015, where the RCU2 was operated in a close to normal running situation while exposed to a wide proton beam at a moderate flux. In this irradiation campaign, the RCU2 was receiving and processing triggers upon where it was performing the basic data taking operation. At the same time all available registers in the RCU2 were monitored. This paper will present and discuss the outcome of this system-level irradiation test.

One full sector (6 RCUs) have already successfully been installed and the complete installation is planned in June 2015. At the time of writing, the RCU2 mass production and testing is ongoing, and the project is entering commissioning phase. The FPGA design is done incrementally and several versions are expected in the near future. By the time of installation all major building blocks will be in place. The outcome of the commissioning and the results from the first running period will be discussed in the paper, where special attention will be given to the two main objectives of the upgrade: Readout rate and stability.

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