Contribution ID: **64** Type: **Poster**

Characterization of a Three-Side Abutable Cmos Pixel Sensor with Digital Pixel and Data Compression for Charged Particle Tracking : PIXAM

Tuesday, 29 September 2015 16:37 (1 minute)

CMOS pixel sensor technology has been chosen to equip the new trackers in ALICE foreseen for HL-LHC. PIXAM is the final prototype from a R&D program specific to the Muon Forward Tracker which intends to push significantly forward the performances of the mature rolling shutter (RS) architecture. By implementing a digital pixel in addition with group of rows for the readout operation, the PIXAM sensor increases the RS readout speed while keeping constant the power consumption. This paper will describe shortly the ASIC architecture and will focus on the sensor analogue and digital performances obtained in laboratory.

Summary

CMOS Monolithic Active Pixel Sensors (MAPS) in the TowerJazz 0.18 µm CIS process have been chosen for the upgrades of internal trackers of ALICE experiment at CERN, namely the ITS (Inner Tracking System) and the MFT (Muon Forward Tracker). Rolling shutter readout is a classical architecture in MAPS usually well suited to reduce the power consumption in the active area of the sensor by activating only one row at a time for reset and readout operations. Its benefits are widely used from imaging sensors to high energy physics sensors where large sensing area and low power consumptions are issues. One drawback of the rolling shutter architecture is that the integration time is proportional to the number of rows of the matrix, limiting one of the dimensions of the sensor active area to keep readout speed to a reasonable value lower than few tens of µs.

In order to overcome this limitation, a new architecture was proposed for the ALICE-MFT project consisting to integrate a discriminator inside the pixel. Indeed, thanks to the in-pixel digital processing of the signal, the total power dissipation is reduced and the rolling shutter readout architecture could activate several rows at the same time, increasing the readout speed. This paper presents the prototype PIXAM, which represents 1/3 of the final ASIC, gathering all the previously described architecture concepts into a large size chip of 10 mm × 6.9 mm. Thus, each pixel of 25 µm × 25 µm includes: a charge collection diode, an amplifier, a CDS (Correlated Double Sampling) circuitry, and an 'autozero'discriminator.
In addition to the matrix performances enhancement, a zero suppression algorithm, based on a 3 by 3 cluster finding (position and data), has been integrated, allowing adequate data compression for the sensor. The digital section of the ASIC has been hardened against SEU effects. Finally, a standard SPI slow control unit permits to program reference and bias values, registers configurations and the digital timing sequence.

The ASIC has been designed to test separately the analogue signal processing (charges collection and amplification), the analogue to digital signal processing and the zero suppression algorithms. Performances studies of each of these points - in addition with the complete sensor - will be available at conference time.

Primary author: GUILLOUX, Fabrice (CEA/IRFU - Centre de Saclay (FR))

Co-authors: Dr FLOUZAT, Christophe (CEA/IRFU - Centre de Saclay (FR)); MONMARTHE, Estelle (CEA/IRFU - Centre de Saclay (FR)); ORSINI, Fabienne (CEA/IRFU - Centre de Saclay (FR)); VENAULT, Philippe (CEA/IRFU -

Centre de Saclay (FR)); DEGERLI, Yavuz (CEA/IRFU - Centre de Saclay (FR))

Presenter: GUILLOUX, Fabrice (CEA/IRFU - Centre de Saclay (FR))

Session Classification: Poster

Track Classification: ASICs