Redundant SAR ADC Architecture and Circuit Techniques for ATLAS LAr Phase-II Upgrade

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Outline

• Introduction
• ADC Architecture and Redundancy
• Single-Event-Effect (SEE) Protection
• Layout and Simulation Results
• Summary
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ADC Specs for Phase-II LAr Readout

- High resolution: **12-14 bits**
- High speed: **40-80 MS/s**
- Low power, low area
- Radiation-tolerant

Diagram showing the signal processing flow from detector output to back-end with key components such as preamp, analog shaper, ADC, and serializer. The diagram also highlights the use of optical links and the 16-bit differential resolution (DR) with a question mark indicating an unspecified parameter.
Previous TID Results (TWEPP’14)

- 12-bit, 160-MS/s ADC on 40-nm CMOS
- Total radiation dose up to 1 Mrad
- No significant degradation on SNDR, SFDR
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• Split-ADC enables digital background calibration

\[ w_{A,i}(n+1) = w_{A,i}(n) - \mu \cdot \varepsilon \cdot D_{A,i} \]

• LMS update:

\[ w_{B,i}(n+1) = w_{B,i}(n) + \mu \cdot \varepsilon \cdot D_{B,i} \]
Architecture – Pipelined SAR

- Fewer number of bits in first stage
- Amplifier removed from SAR Loop

Fast Conversion
Architectural Redundancies

Sub-binary DAC

RA gain reduction and inter-stage redundancy

Intra-stage and inter-stage redundancies for dynamic error tolerance

- DAC incomplete settling, reference voltage bouncing, etc.
- Comparator hysteresis, noise crosstalk, etc.
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Split ADC for SEE Protection

- If $\Delta D_o$ is large, chose the output of the ADC that is not hit
- A 3-dB SNR gain with normal operation (i.e., no hit)
Modeling SEE Current

\[ I(t) = \frac{Q_{\text{tot}}}{\tau_2 - \tau_1} \left( e^{-t/\tau_2} - e^{-t/\tau_1} \right) \]

Ref. Bonacini, “Redundancy methods in ASICs,” 2013

Summing-Node Hit Detection

- For $Q_{\text{SEE}} = 100\ \text{fC}$ and $C_{\text{TOT}} = 2\ \text{pF}$, $V_{\text{err}} = 50\ \text{mV}$!
- SEE detector is formed by a pair of resistors, a "substrate-current amplifier", and some digital logic
The total charge collected due to SEE is \( \sim 5.5 \) fC, causing a 2.75-mV voltage error on a 2-pF DAC (\( \sim 20 \) LSBs).

The detector is reset at the beginning of each sample period.
Out-of-range error can be detected by observing the code of the 2\textsuperscript{nd} stage: 11…11 (overshoot) or 00…00 (undershoot)
2\textsuperscript{nd}-Stage SAR Error Detection

![Diagram showing 2\textsuperscript{nd}-stage DAC with extra capacitance and voltage transitions.

- Normal condition:
  - \( V_{X^+} - V_{X^-} \) graph.
  - LSB transition.
  - 10

- Normal condition with noise:
  - \( V_{X^+} - V_{X^-} \) graph with noise.
  - LSB transition.
  - 01

- Large error:
  - \( V_{X^+} - V_{X^-} \) graph with large error.
  - LSB transition.
  - 11

Extra cycle detected in 2\textsuperscript{nd}-stage DAC.
Data-latch not TMR-protected to reduce the comparator loading
Data-Latch Error Detection

Data latches hit during residue amplification may cause error.
Data-Latch Error Detection

Parity bit

One data latch may be hit

Sampling

1st SAR Conversion

Amplification

Parity bit stored

Data output
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Layout Screenshot

65-nm CMOS
### Preliminary Simulation Results

<table>
<thead>
<tr>
<th>Corner</th>
<th>Max. Fs [MS/s]</th>
<th>SNDR [dB]</th>
<th>SFDR [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT (w/o noise)</td>
<td>100</td>
<td>86.5</td>
<td>99.9</td>
</tr>
<tr>
<td>SS (w/o noise)</td>
<td>80</td>
<td>86.4</td>
<td>99.2</td>
</tr>
<tr>
<td>FF (w/o noise)</td>
<td>100</td>
<td>86.9</td>
<td>101.8</td>
</tr>
<tr>
<td>TT (w/ noise)</td>
<td>100</td>
<td>76.4, single 79.1, avg</td>
<td>93.3, single 95.3, avg</td>
</tr>
</tbody>
</table>

- **SNDR** = 86.5 dB
- **SFDR** = 99.9 dB
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Summary

- Redundant pipelined SAR ADC is a strong candidate to meet the stringent requirements for ATLAS LAr upgrade
- Split-ADC architecture with SEE detection techniques provides a potential (architecture + analog) solution to SEE
- Various SEE-protection techniques and proven TID-tolerance will result in a fully radiation-tolerant ADC in CMOS in the near future
- Stay tuned…

Thank you for your attendance!
Backup Slides
Split-ADC Bit-Weight Calibration

\[ C_{DAC} \quad C_{CAL} \]

\[ C_0 \quad C_1 \quad \cdots \quad C_N \]

\[ PN \cdot V_{ref} \ (PN=\pm 1) \]

![Diagram showing the connection between \( C_{DAC} \) and \( C_{CAL} \) with an operational amplifier.

Offset injection to the SAR conversion curve to split the decision trajectory

\[ V_{out} \quad V_{in} \]

Injection \( > 0 \)

Injection \( < 0 \)
Behavioral Simulation Results

 Calibration converges within 1 million samples
Comparator-RA Offset

- 150-mV 2nd-stage full scale
- 2-bit inter-stage redundancy
- 16× inter-stage gain

Maximum tolerable offset:

$$V_{OS,\text{MAX}} = \frac{3}{4} \times 150\text{mV} = 7\text{mV}$$

Too small!

Observing the digital code of the 2nd stage enables residue confinement.
Comparator-RA Offset Calibration

Auxiliary DAC used to compensate the comparator-RA offset
TMR Protection for Logic Gates

TMR-protected shift registers are used in other parts, i.e., clock generation, parallel-to-serial conversion, etc.