Redundant SAR ADC Architecture and Circuit Techniques for ATLAS LAr Phase-II Upgrade

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Outline

- Introduction
- ADC Architecture and Redundancy
- Single-Event-Effect (SEE) Protection
- Layout and Simulation Results
- Summary

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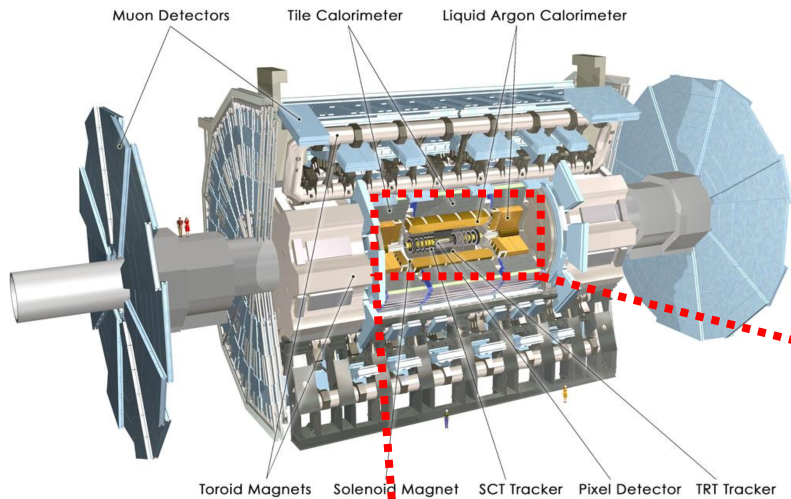
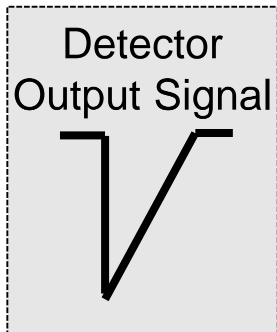
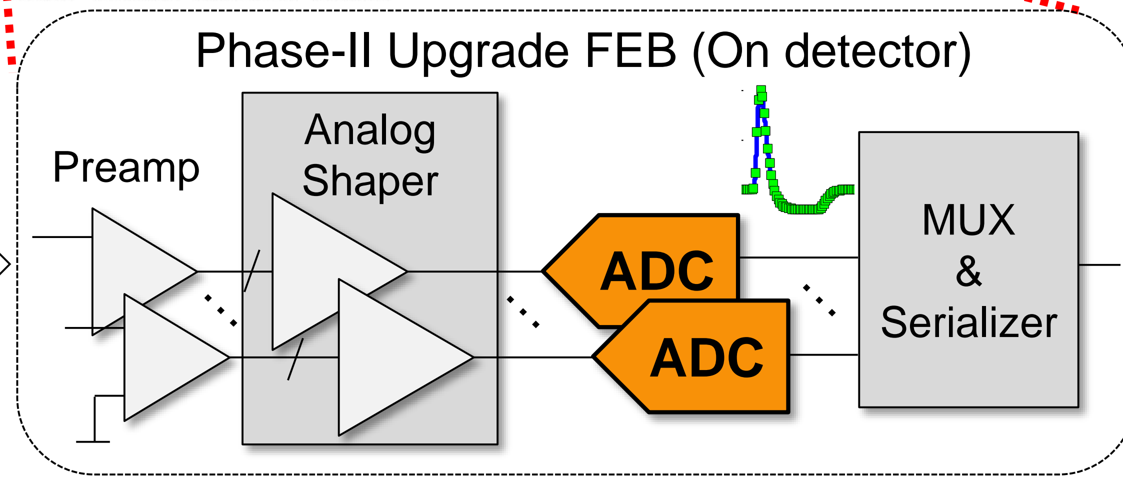
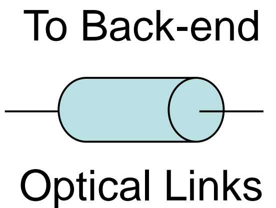
ADC Specs for Phase-II LAr Readout



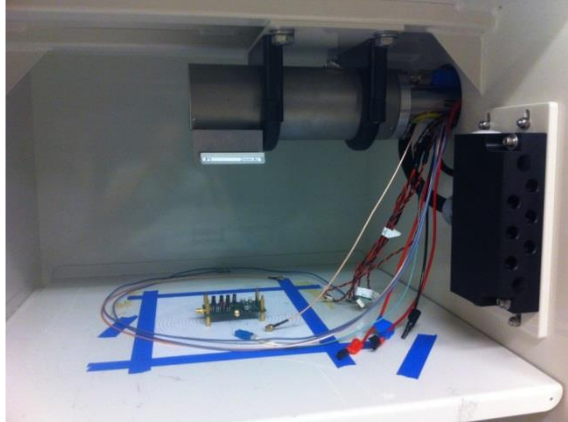
- High resolution: **12-14 bits**
- High speed: **40-80 MS/s**
- Low power, low area
- Radiation-tolerant

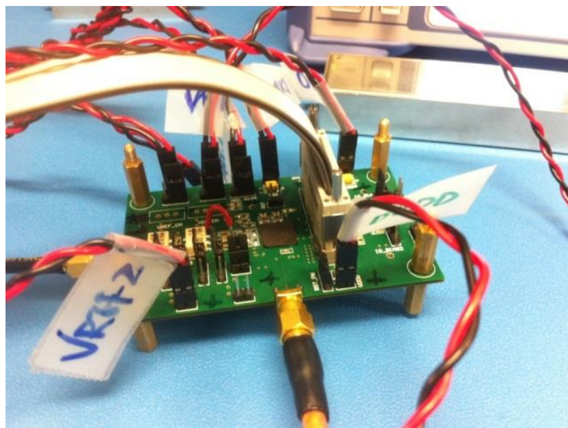






Previous TID Results (TWEPP'14)





fin=10MHz
fin=25MHz
fin=40MHz
fin=70MHz

SNDR [dB] / ENOB [bit] vs. Radiation dose [krad]

SFDR [dB] / ENOB [bit] vs. Radiation dose [krad]

- 12-bit, 160-MS/s ADC on 40-nm CMOS
- Total radiation dose up to 1 Mrad
- No significant degradation on SNDR, SFDR

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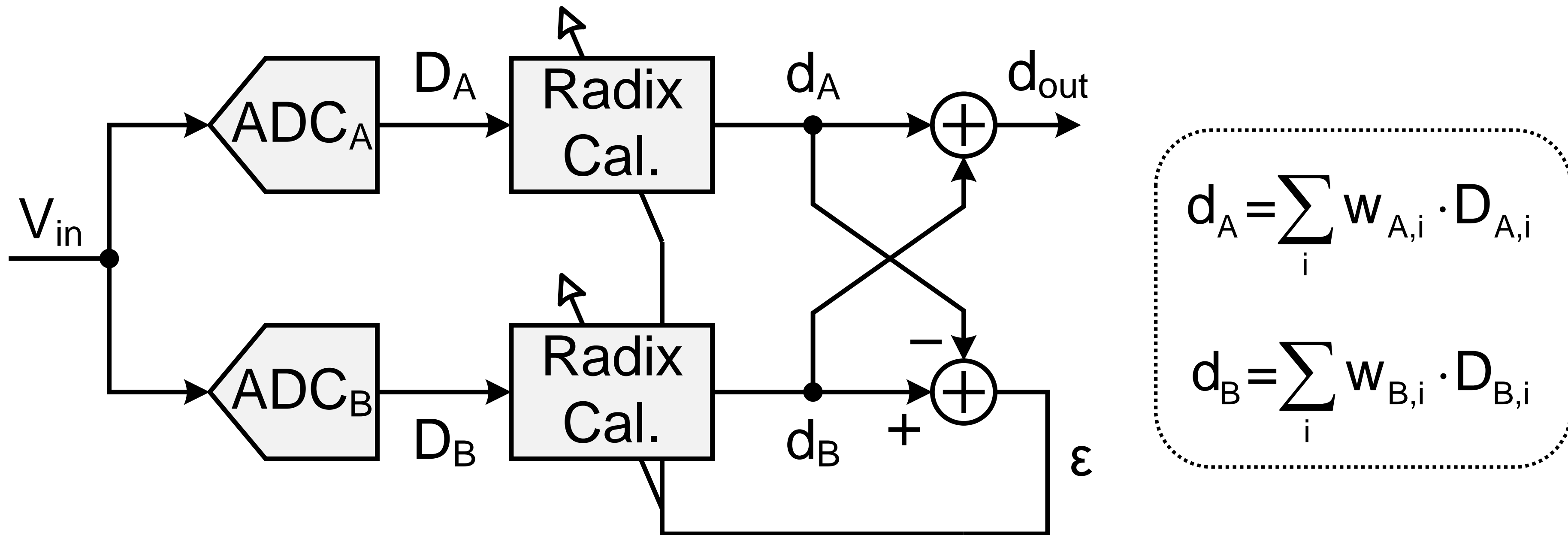
Architecture – Split ADC



- Split-ADC enables digital background calibration
- LMS update:

$$w_{A,i}(n+1) = w_{A,i}(n) - \mu \cdot \varepsilon \cdot D_{A,i}$$

$$w_{B,i}(n+1) = w_{B,i}(n) + \mu \cdot \varepsilon \cdot D_{B,i}$$

Architecture – Pipelined SAR

V_{in} + − Amp + − Cap DAC SAR logic Cap DAC SAR logic

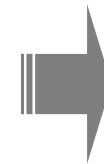
9 bits

First stage

7 bits

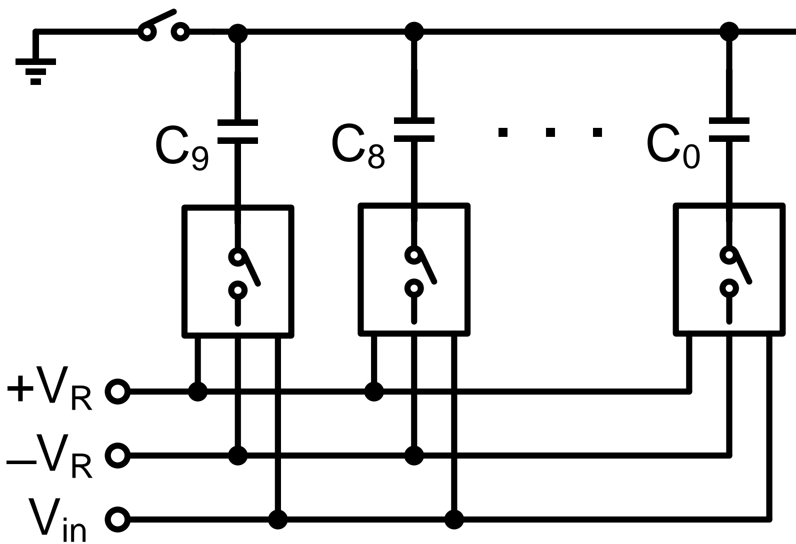
Second stage

- Fewer number of bits in first stage
- Amplifier removed from SAR Loop

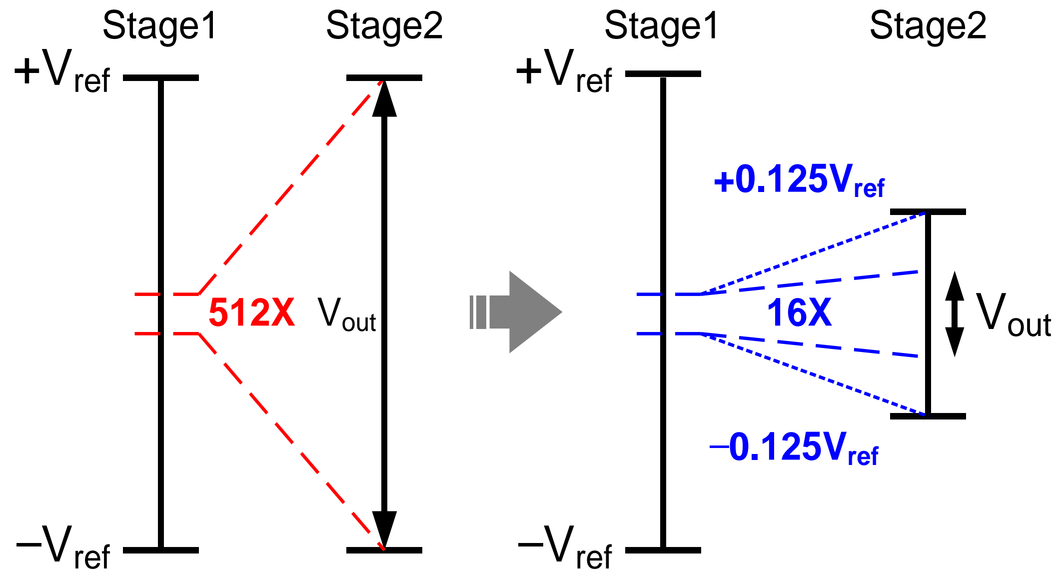


Fast Conversion

Architectural Redundancies



Sub-binary DAC



RA gain reduction and inter-stage redundancy

Intra-stage and inter-stage redundancies for dynamic error tolerance

- DAC incomplete settling, reference voltage bouncing, etc.
- Comparator hysteresis, noise crosstalk, etc.

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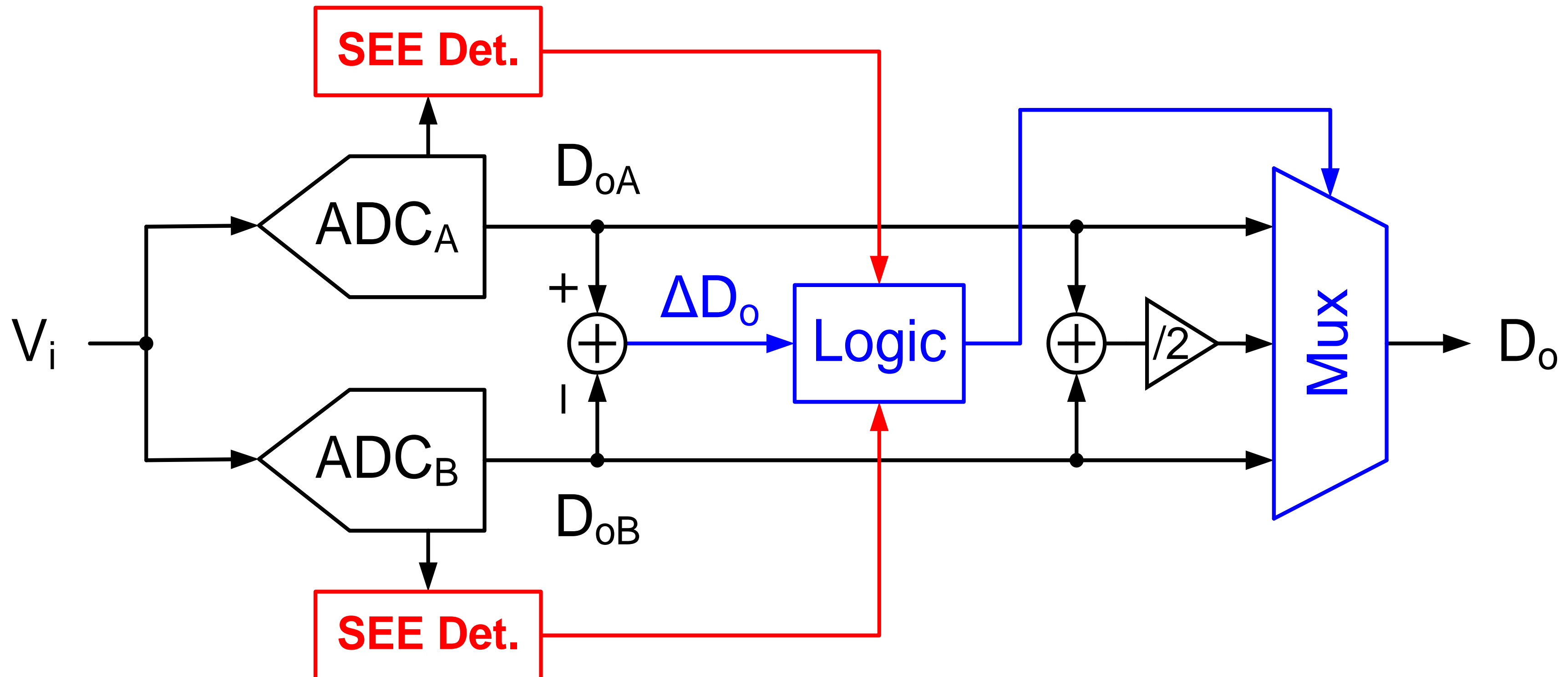
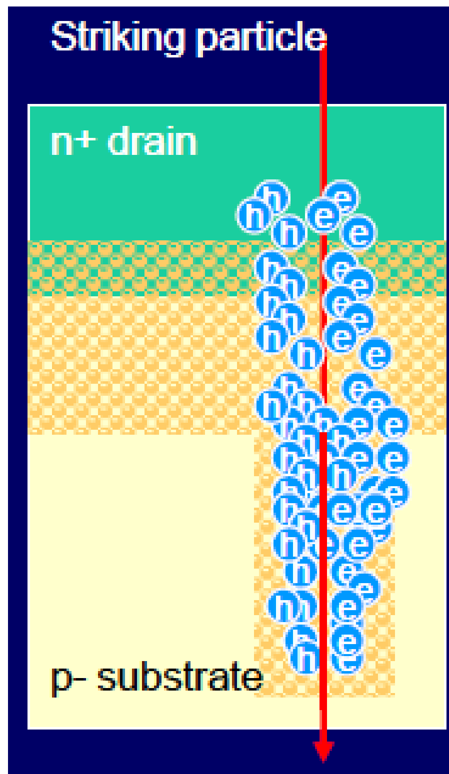
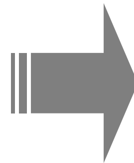
Split ADC for SEE Protection

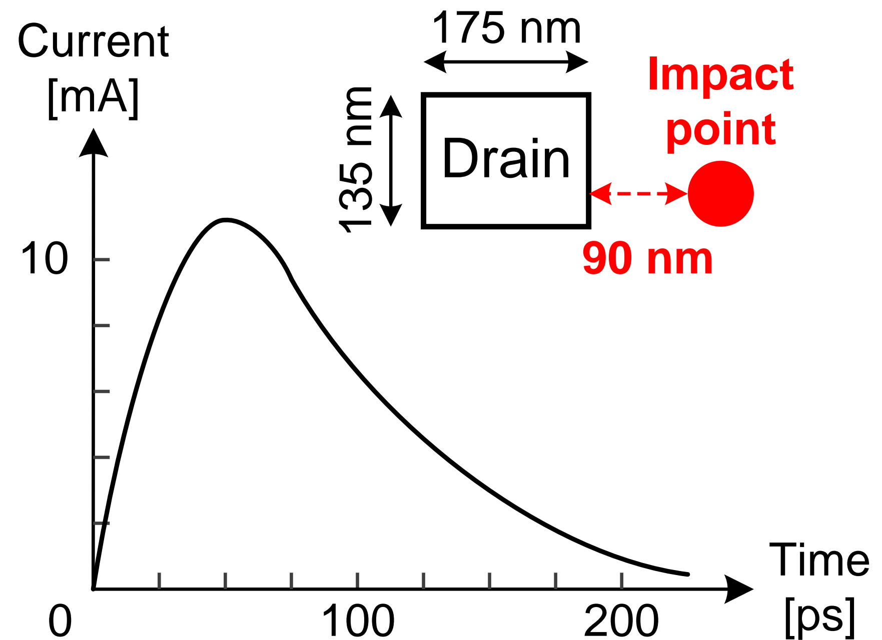


- If ΔD_o is large, chose the output of the ADC that is not hit
- A 3-dB SNR gain with normal operation (i.e., no hit)

Modeling SEE Current





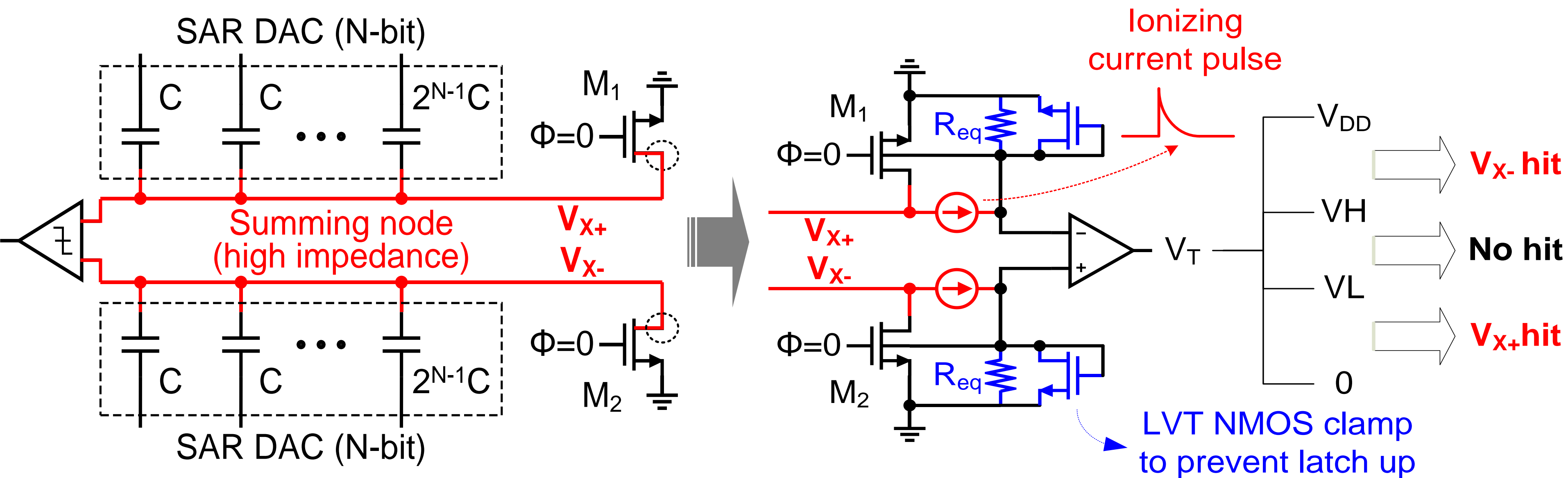


$$I(t) = \frac{Q_{tot}}{\tau_2 - \tau_1}\left(e^{-t/\tau_2} - e^{-t/\tau_1}\right)$$

Ref. Bonacini, “Redundancy methods in ASICs,” 2013

Ref. Mavis and Eaton, “SEU and SET Modeling and Mitigation in Deep Submicron Technologies,” 2007

Summing-Node Hit Detection

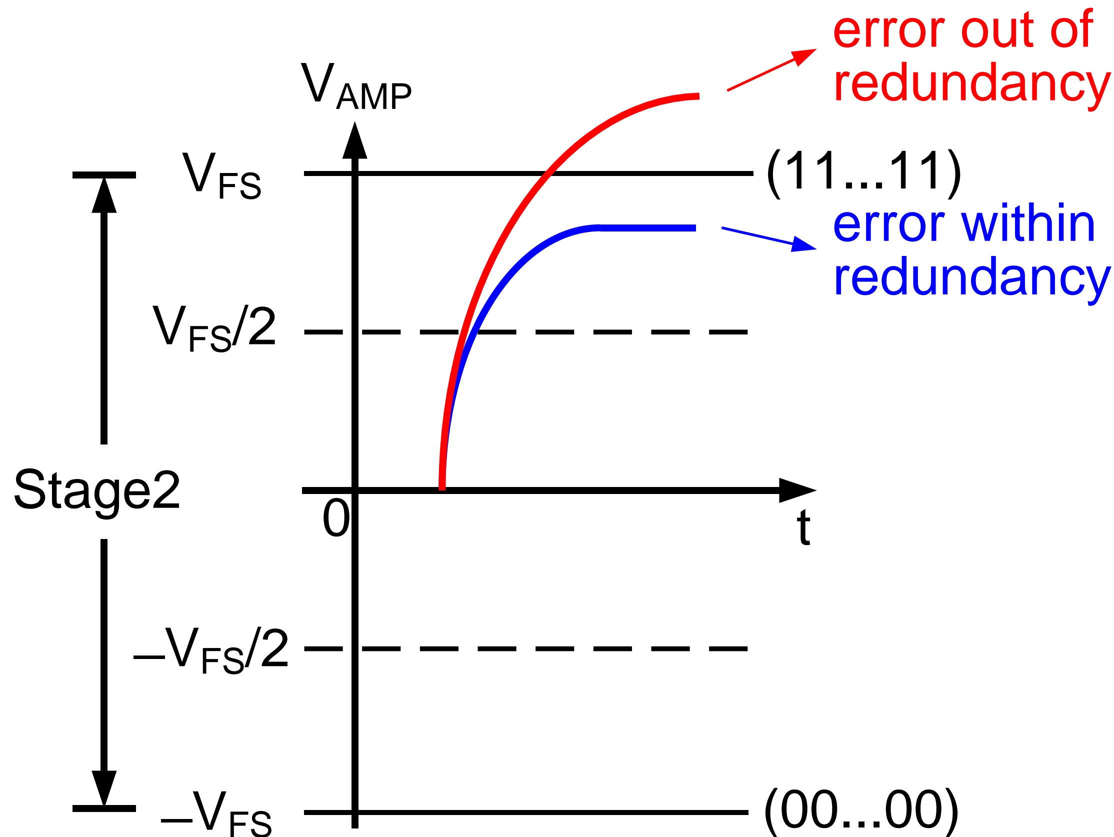


- For Q_{SEE} = 100 fC and C_{TOT} = 2 pF, V_{err} = 50 mV !
- SEE detector is formed by a pair of resistors, a “substrate-current amplifier”, and some digital logic

Summing-Node Hit Detection

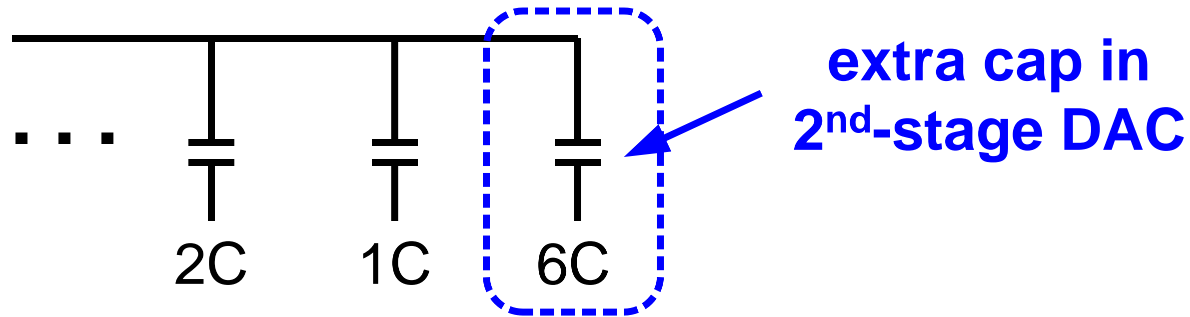
- The total charge collected due to SEE is ~5.5 fC, causing a 2.75-mV voltage error on a 2-pF DAC (~20 LSBs)
- The detector is reset at the beginning of each sample period

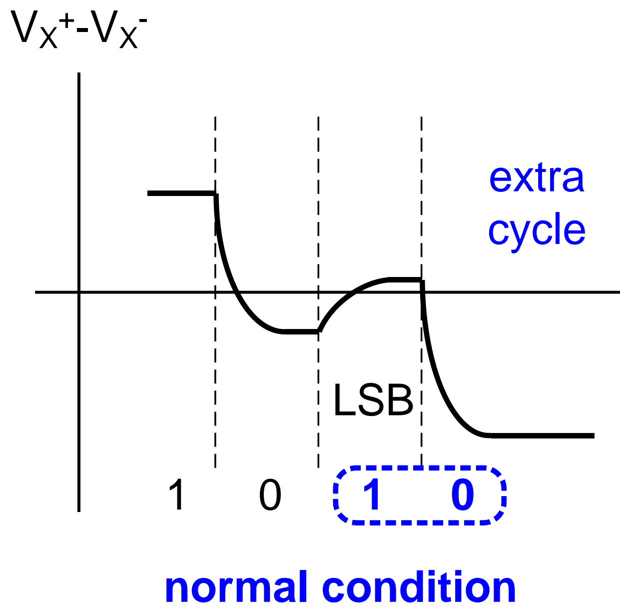
1st-Stage SAR Error Detection

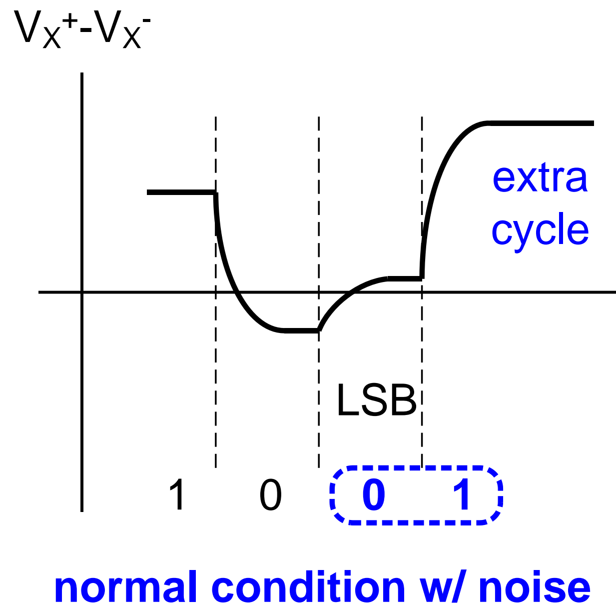


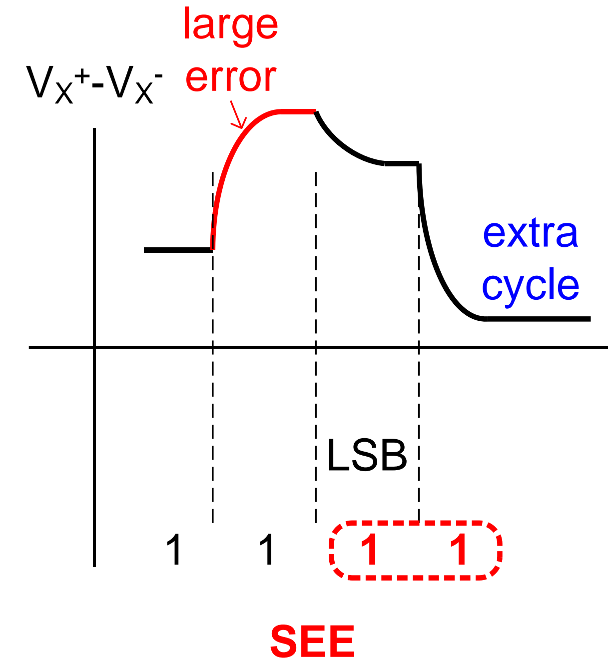
Out-of-range error can be detected by observing the code of the 2nd stage: 11…11 (overshoot) or 00…00 (undershoot)

2nd-Stage SAR Error Detection

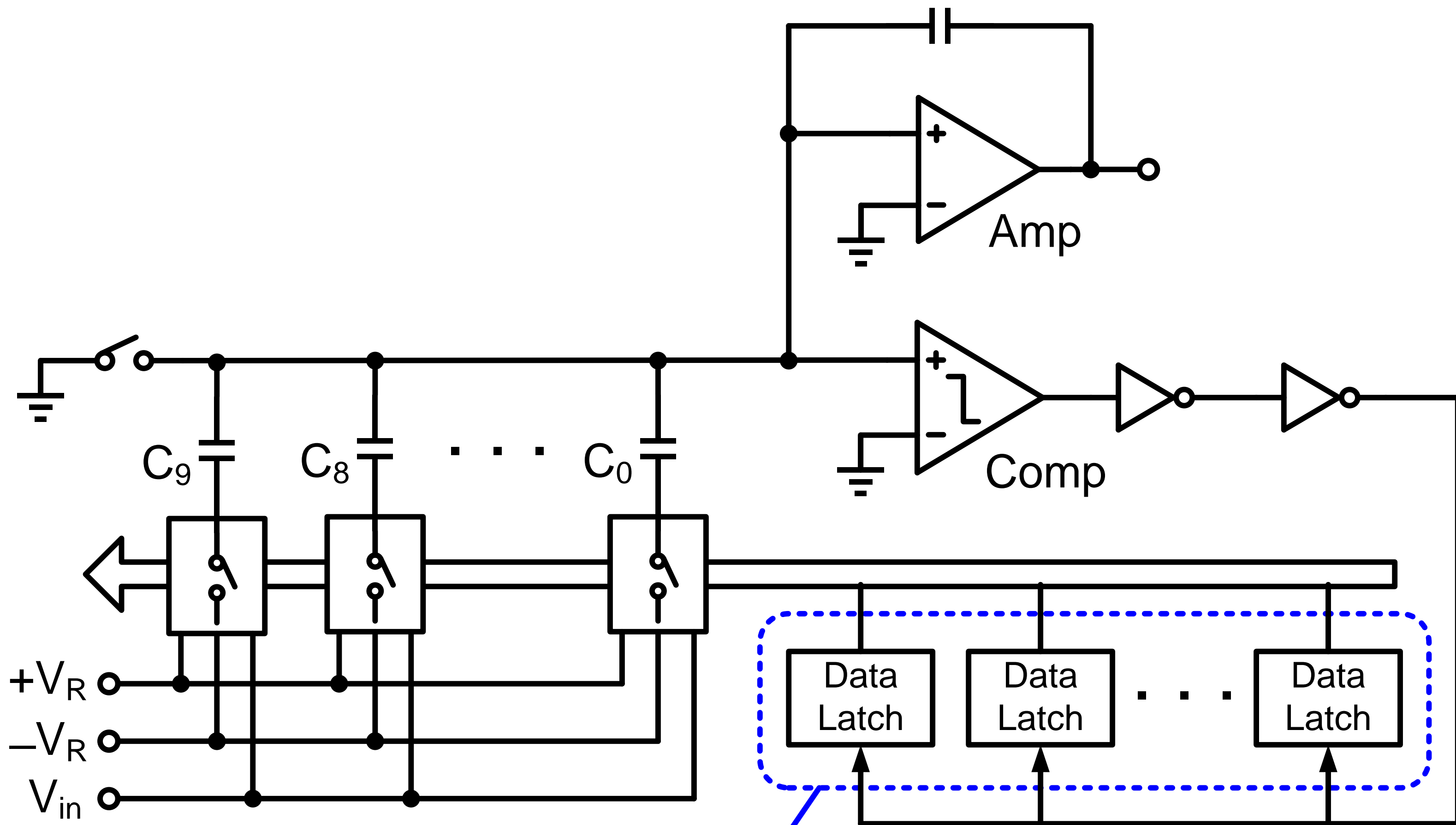






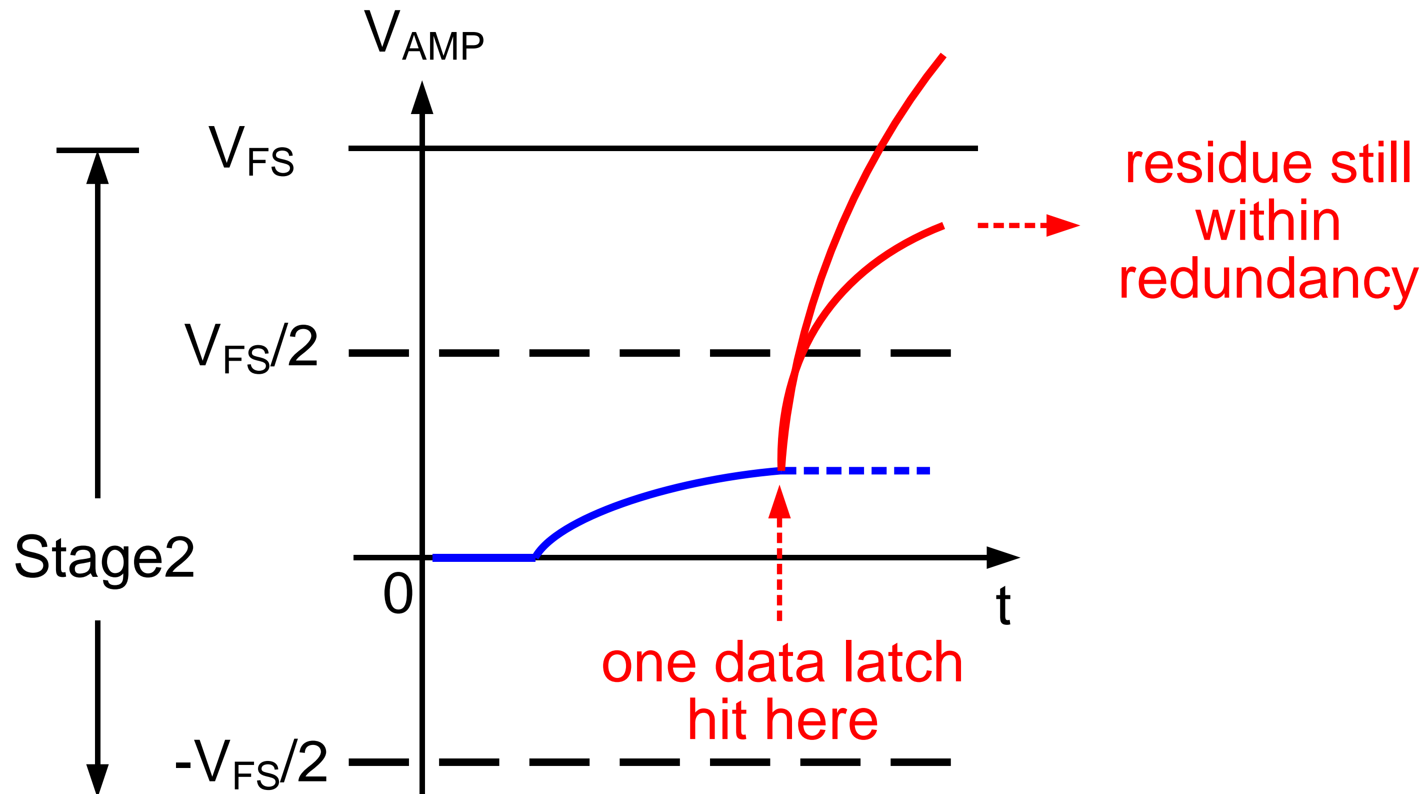


Data-Latch Error Detection



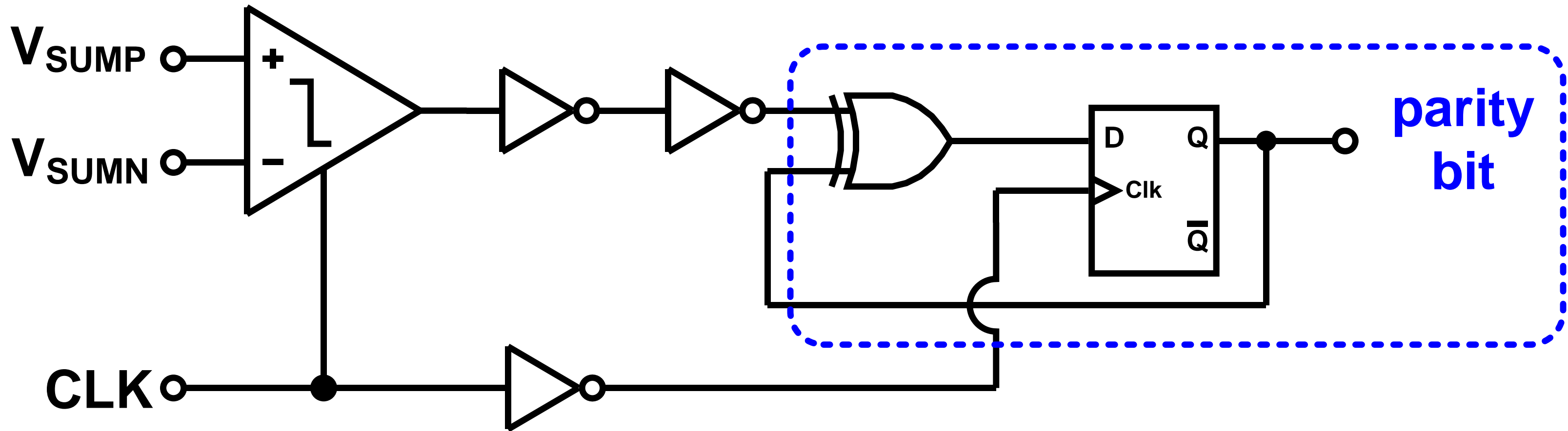
Data latch not TMR-protected to reduce the comparator loading

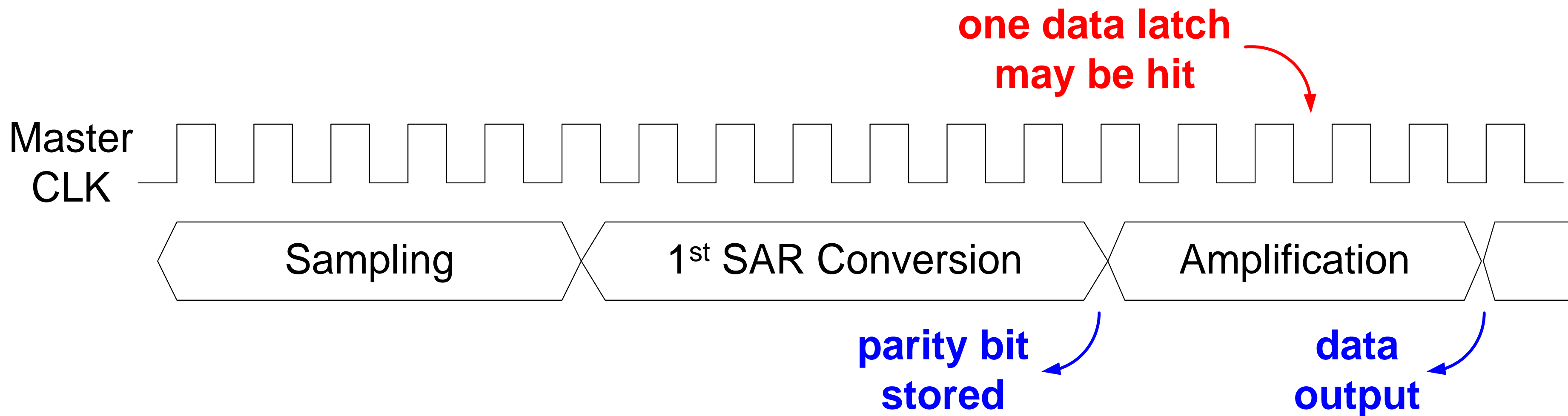
Data-Latch Error Detection



Data latches hit during residue amplification may cause error

Data-Latch Error Detection





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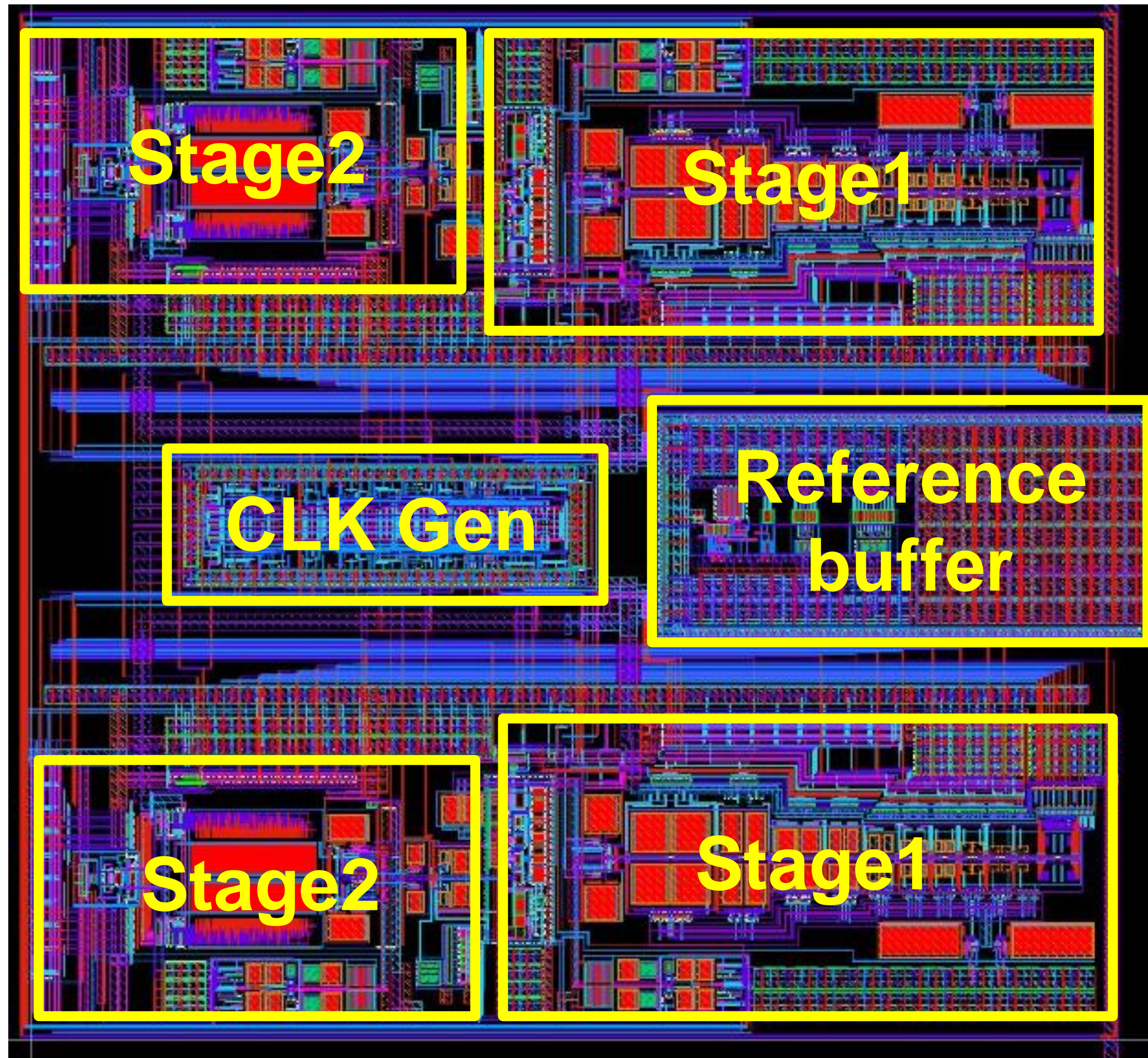
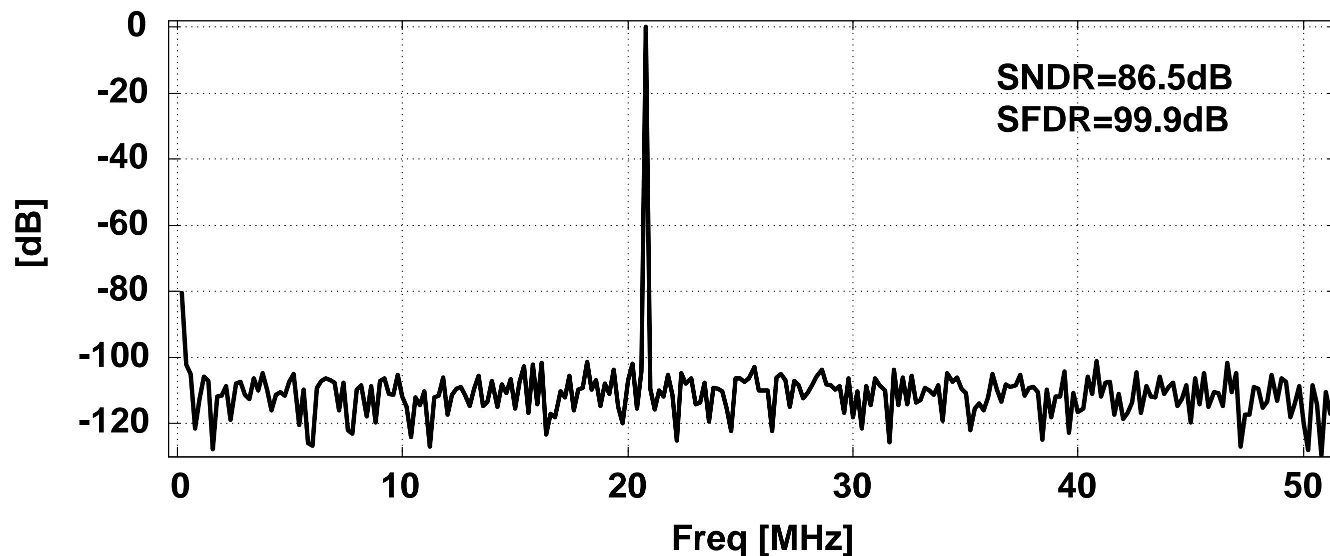
Layout Screenshot



65-nm CMOS

Preliminary Simulation Results



TT w/o circuit noise

Corner	Max. Fs [MS/s]	SNDR [dB]	SFDR [dB]
TT (w/o noise)	100	86.5	99.9
SS (w/o noise)	80	86.4	99.2
FF (w/o noise)	100	86.9	101.8
TT (w/ noise)	**100**	**76.4, single** **79.1, avg**	**93.3, single** **95.3, avg**

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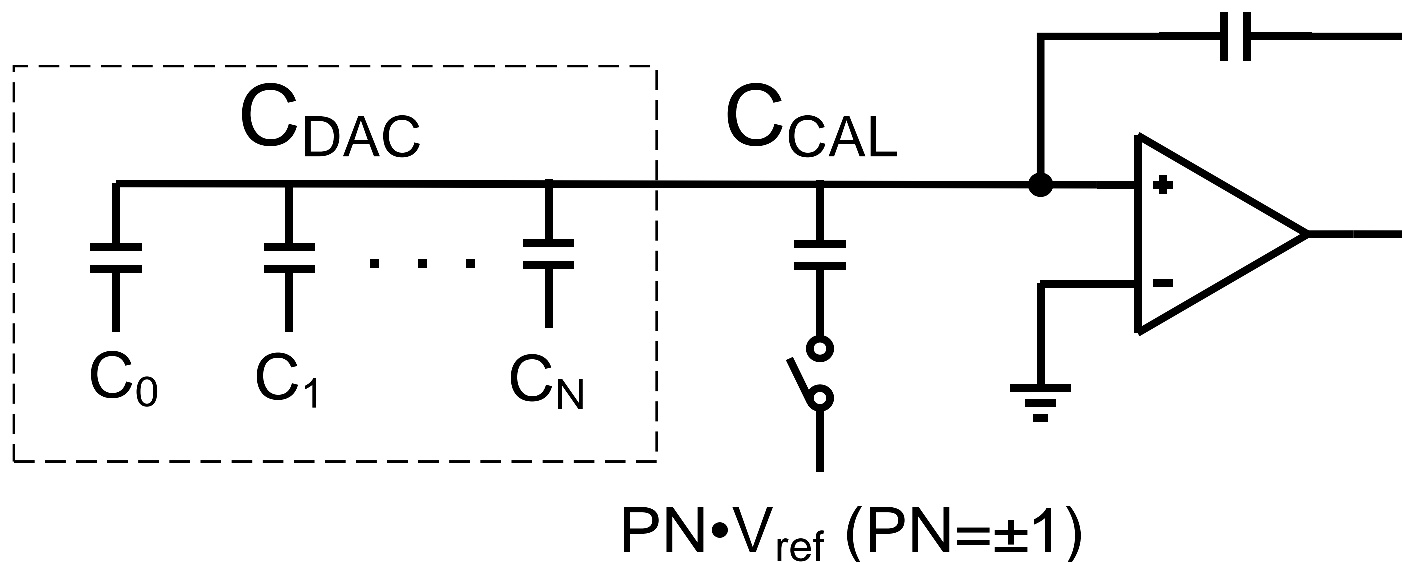
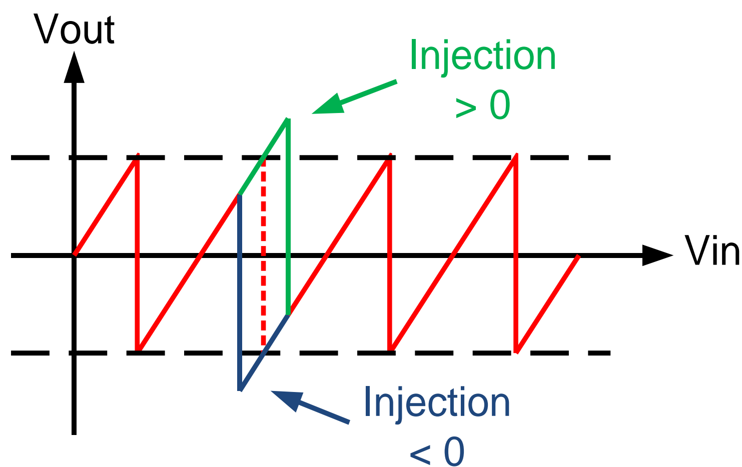
- Redundant pipelined SAR ADC is a strong candidate to meet the stringent requirements for ATLAS LAr upgrade
- Split-ADC architecture with SEE detection techniques provides a potential (architecture + analog) solution to SEE
- Various SEE-protection techniques and proven TID-tolerance will result in a fully radiation-tolerant ADC in CMOS in the near future
- Stay tuned…

Thank you for your attendance!

Backup Slides

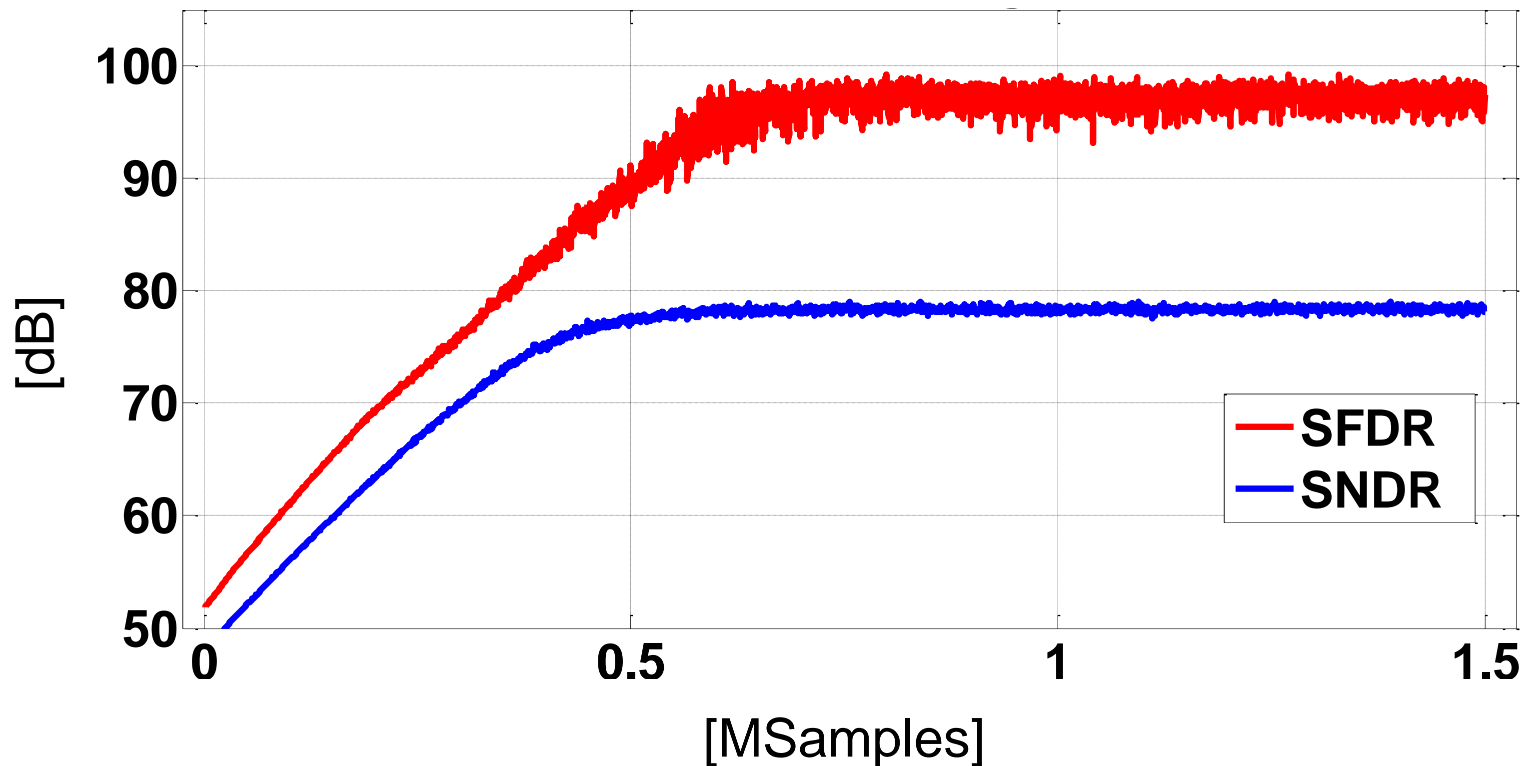
Split-ADC Bit-Weight Calibration





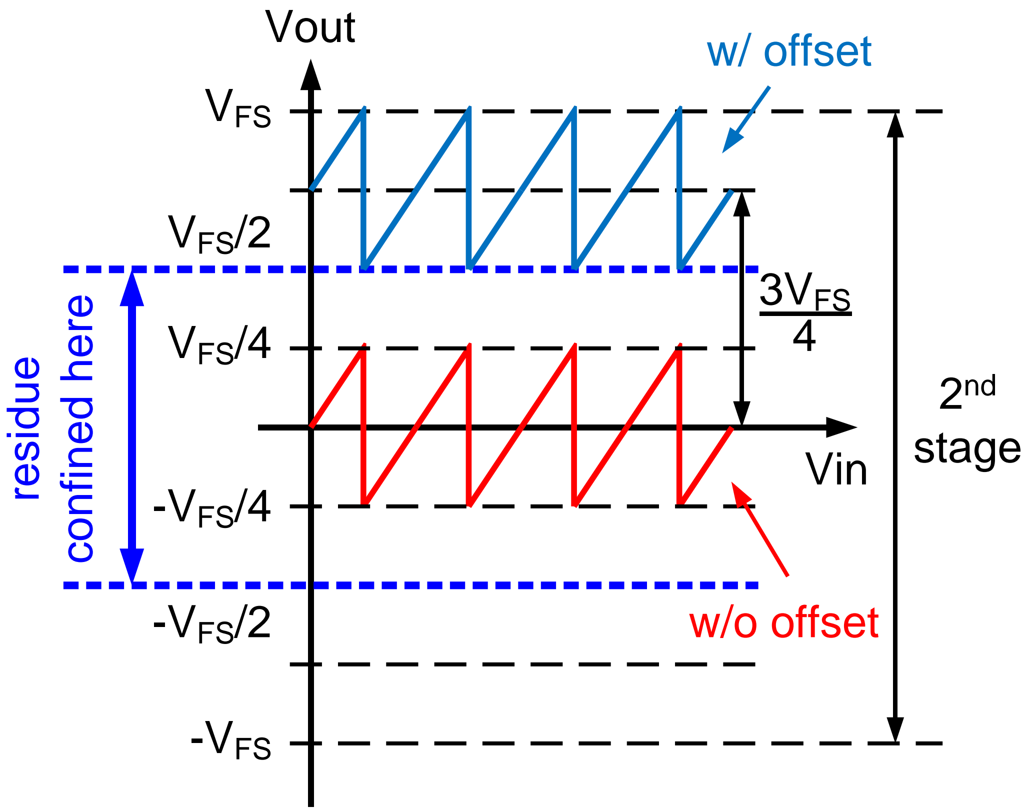
Offset injection to the SAR conversion curve to split the decision trajectory

Behavioral Simulation Results



Calibration converges within 1 million samples

Comparator-RA Offset



- 150-mV 2nd-stage full scale
- 2-bit inter-stage redundancy
- 16× inter-stage gain

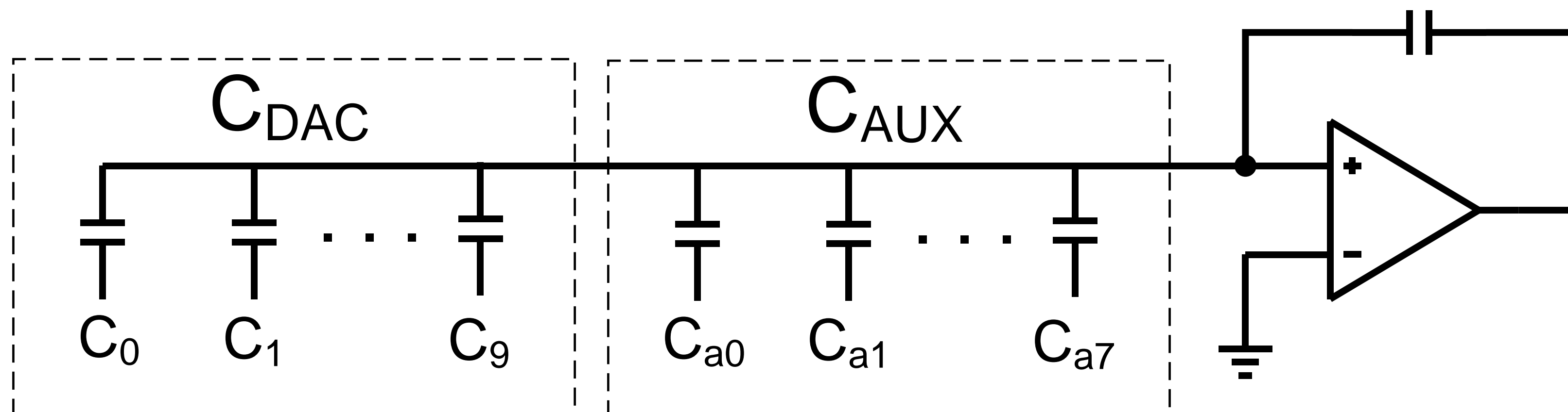
Maximum tolerable offset:

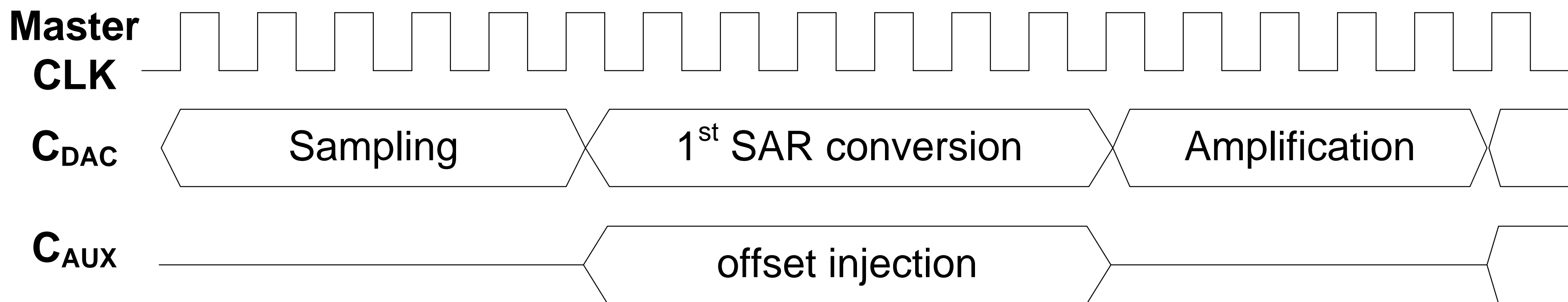
$$V_{OS,MAX} = \frac{\frac{3}{4} \times 150mV}{16} = 7mV$$

Too small !

Observing the digital code of the 2nd stage enables residue confinement

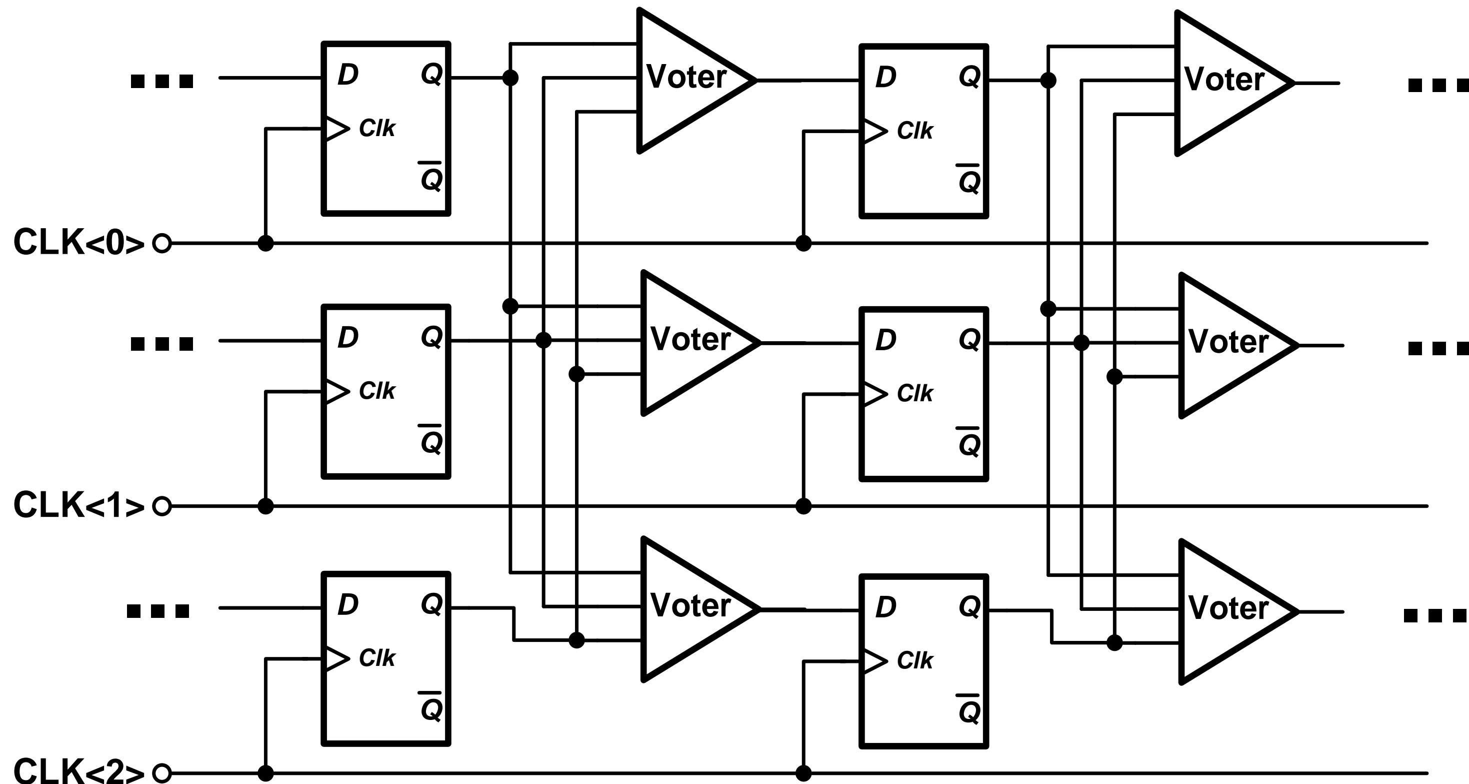
Comparator-RA Offset Calibration





Auxiliary DAC used to compensate the comparator-RA offset

TMR Protection for Logic Gates



TMR-protected shift registers are used in other parts, i.e., clock generation, parallel-to-serial conversion, etc.